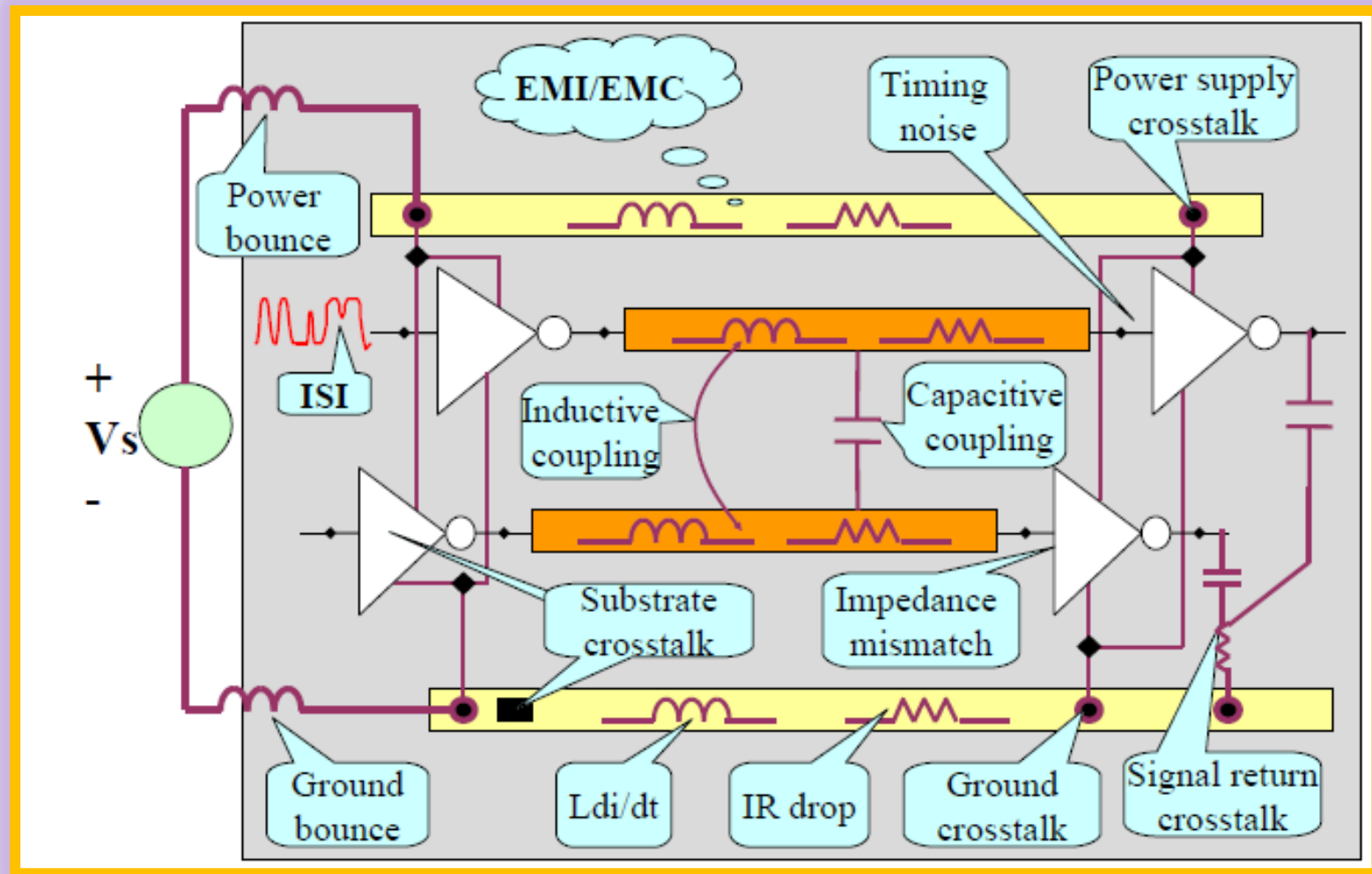


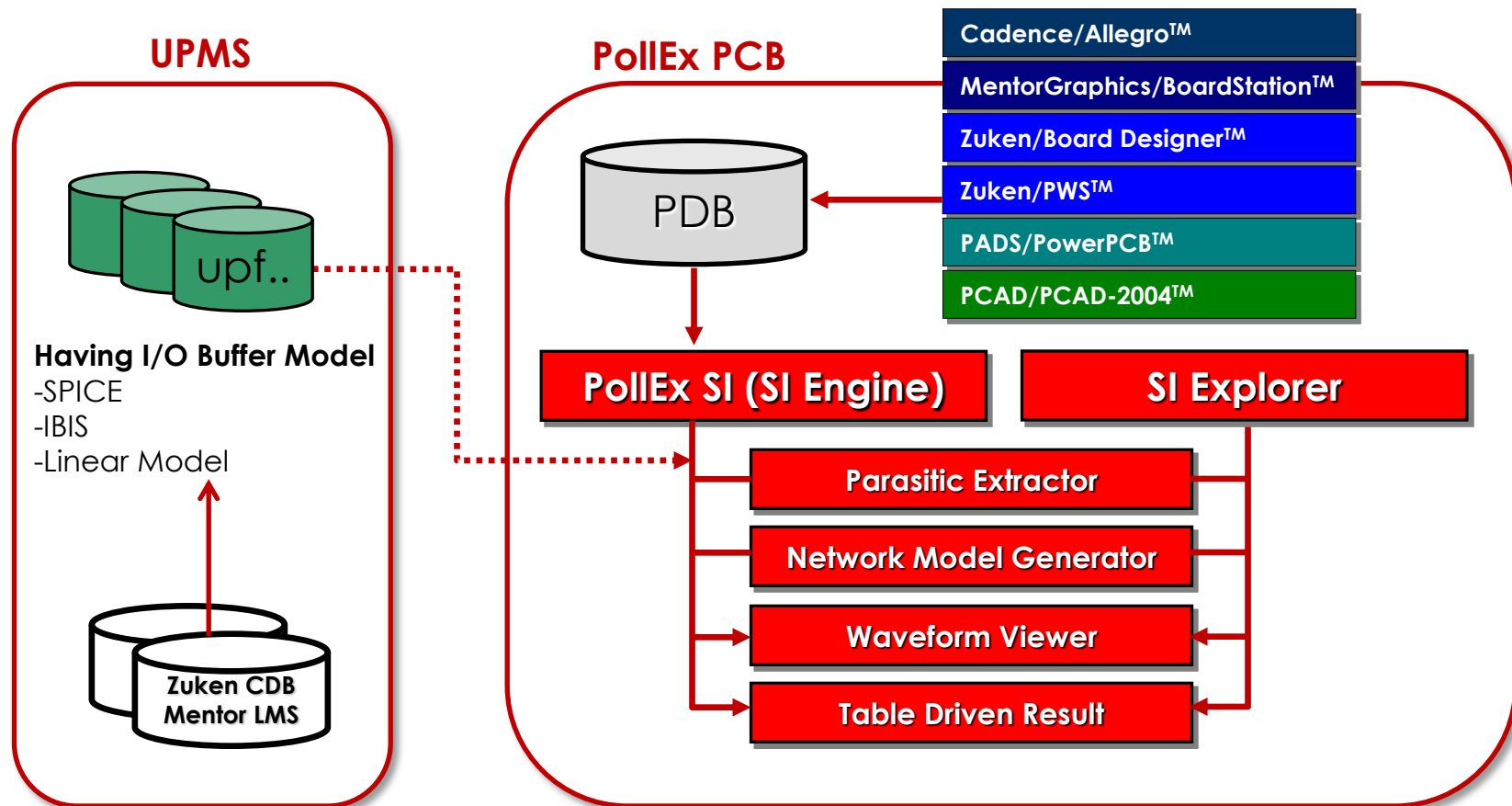
PoIIEx DFE/SI 를 활용한, SI/PI/EMC 대응 설계

- POLLIWOG Corporation.

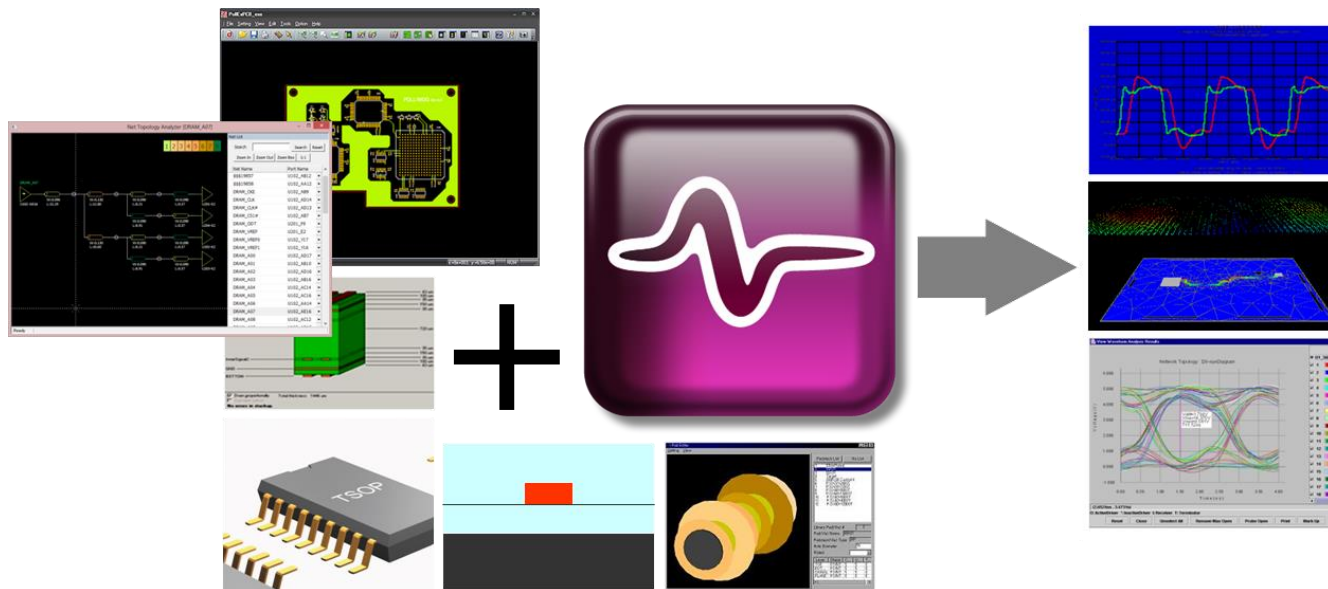
SI/PI/EMI Issue in PCB



PollEx Signal Integrity



PolIEx SI



- **Transmission Line Analysis:** Routed Net Impedance, Delay 분석, TLM Model 생성/관리
- **Network Analysis:** 신호 Eye Diagram, Setup/Hold Margin 및 Noise Analysis
- **Data Line Analysis:** DDR Data Line의 Byte별 Analysis 일괄 수행
- **ADD/CMD/CNTR Line Analysis:** DDR ADD/CMD/CNTR Line의 Byte별 Analysis 일괄 수행
- **Crosstalk Analysis:** Routed Net Coupling 분석, Odd/Even Mode Crosstalk 분석
- **Net Topology Analysis:** Net Topology 분석 및 수정/해석 기능

PolIEx SI

◆ Transmission Line Analysis

- Analysis PCB trace etching effect
- Analysis GND guard effect

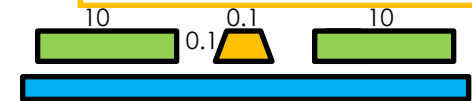
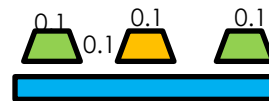
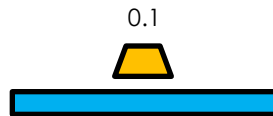
$$Z_0 = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}}$$

$$Z_0 = L/C \propto W, h, t$$

$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln \frac{4b}{0.67\pi(0.8w + t)}$$

$$t_f = 1.017 \sqrt{\epsilon_r} \quad (\text{ns/ft})$$

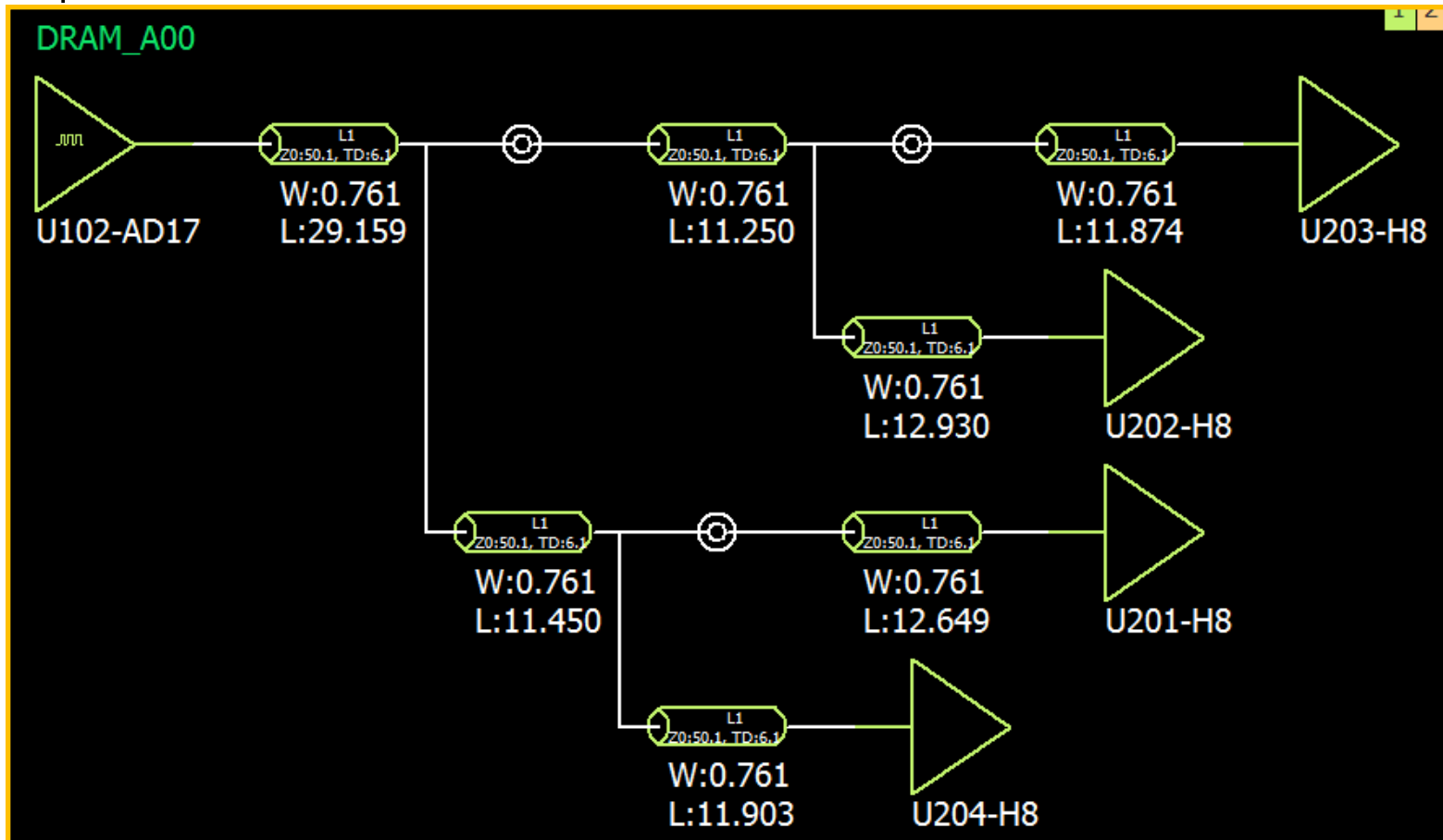
* $w/(b-t) < 0.35, t/b < 0.25$



Transmission Line Analysis-Display Results			Transmission Line Analysis-Display Results			Transmission Line Analysis-Display Results		
Model	Item	Frequency (MHz)	1_0.09	Frequency (MHz)	Z01	Frequency (MHz)	Z01	
ITEM		100	52.691, -1.789	100	49.023, -0.364	100	42.747, -0.61	
	Resistance (Ohm/cm)	111.1	52.597, -1.686	111.1	48.998, -0.34	111.1	42.656, -0.52	
	R11	144.4	52.36, -1.467	144.4	48.94, -0.289	144.4	42.431, -0.33	
	Inductance (nH/cm)	200	52.11, -1.23	200	48.874, -0.232	200	42.195, -0.123	
	L11	277.8	51.902, -1.019	277.8	48.822, -0.181	277.8	41.997, 0.063	
	Capacitance (pF/cm)	377.8	51.735, -0.857	377.8	48.778, -0.141	377.8	41.837, 0.207	
	C11	500	51.587, -0.728	500	48.741, -0.11	500	41.697, 0.32	
	Conductance (mS/cm)	644.4	51.482, -0.629	644.4	48.713, -0.085	644.4	41.598, 0.409	
	G11	811.1	51.394, -0.548	811.1	48.691, -0.065	811.1	41.51, 0.48	
	DC Resistance (Ohm/cm)	1000	51.326, -0.484	1000	48.674, -0.049	1000	41.444, 0.539	
	R01							
	Skin Depth (m)							
	SD1							
	Char-Impedance (Ohm)							
	Z01							
	Delay (sec/m)							
	TD1							
	Velocity (m/sec)							
	V1							
	Attenuation (dB/m)							
	A1							
Display Network Parameters			Display Chart	Close	Display Chart			Close

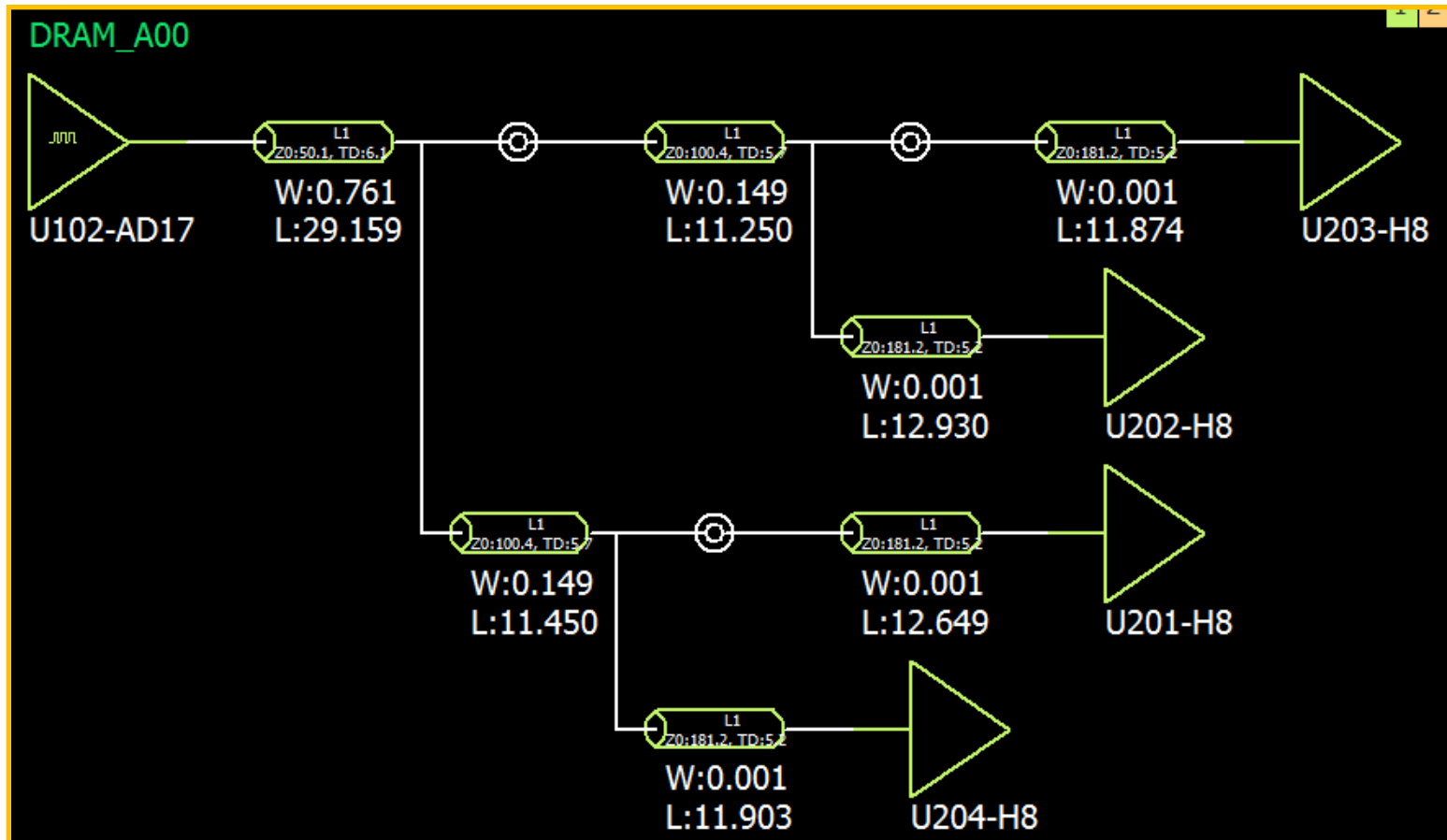
PolIEx SI

◆ Transmission Line Analysis - Impedance Mismatch



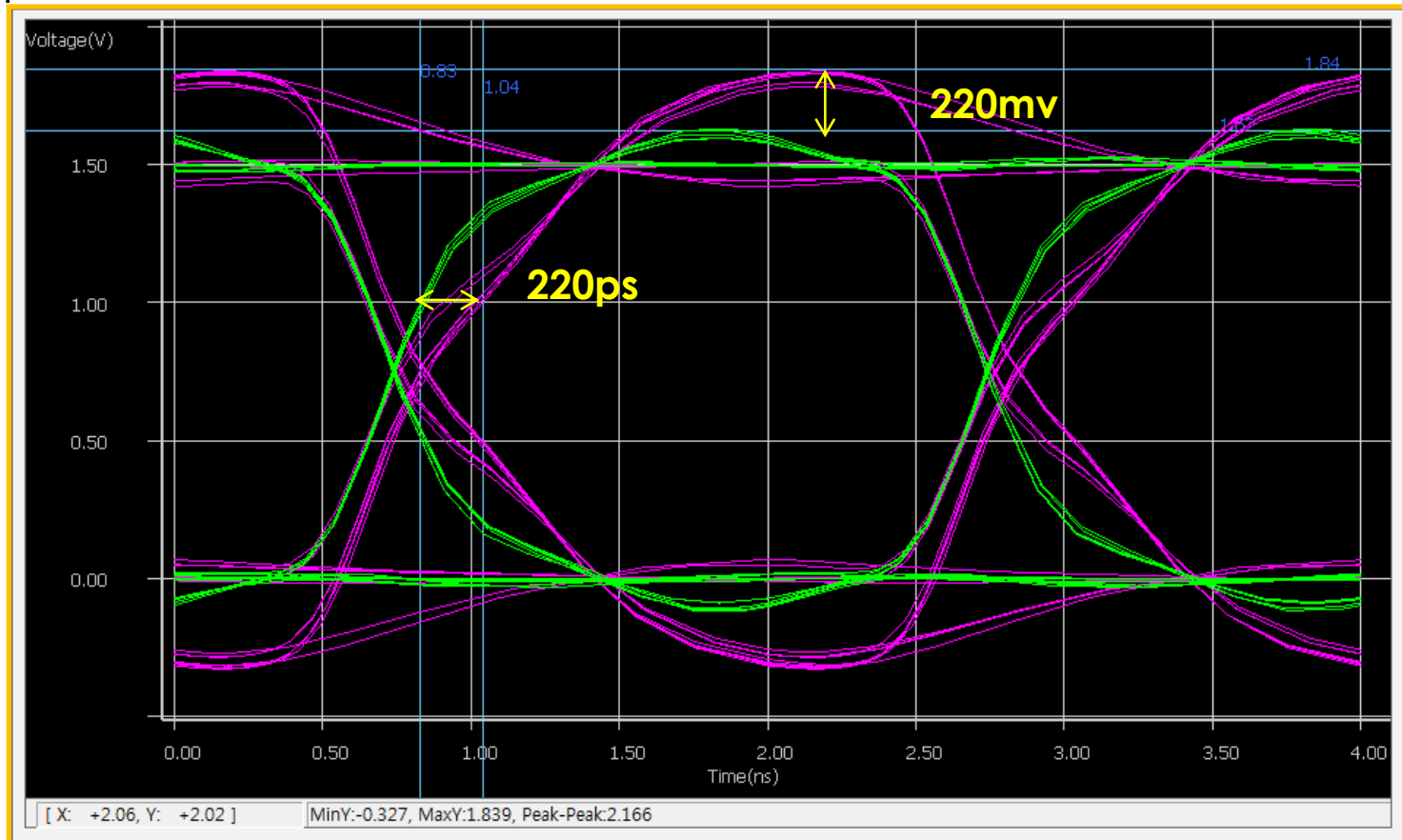
PolIEx SI

◆ Transmission Line Analysis - Impedance Match



PoIEx SI

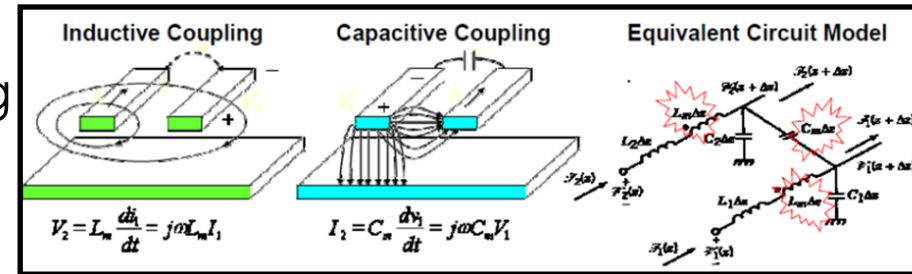
◆ Transmission Line Analysis - Impedance Mismatch



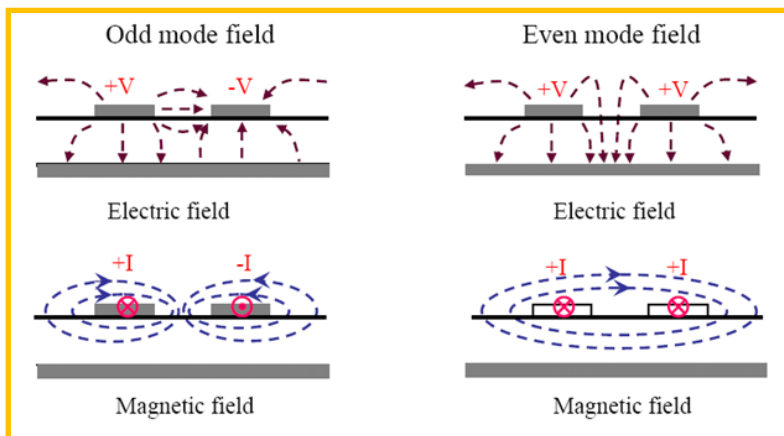
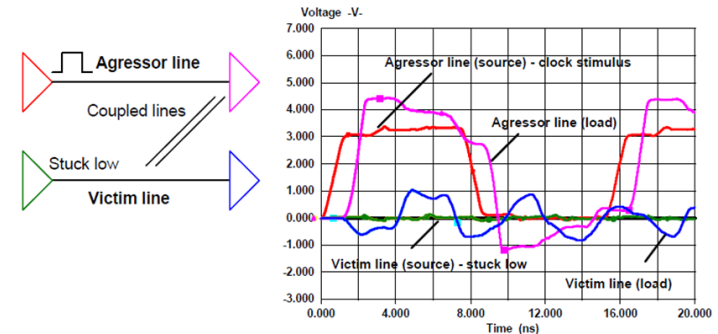
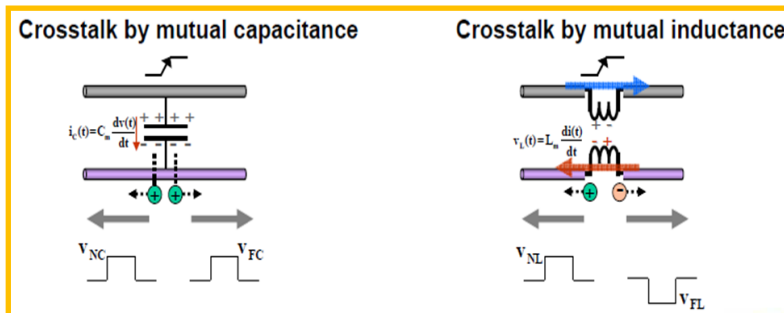
PoIEx SI

◆ Crosstalk Analysis

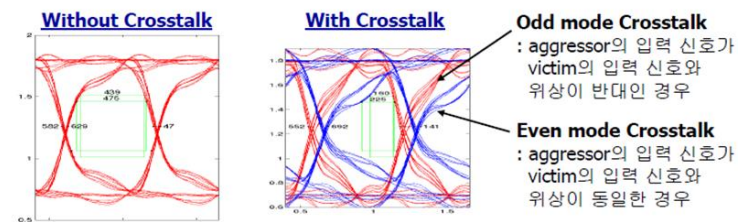
- 주변 신호선과의 Noise Coupling 현상 해석



Noise Margin Issue



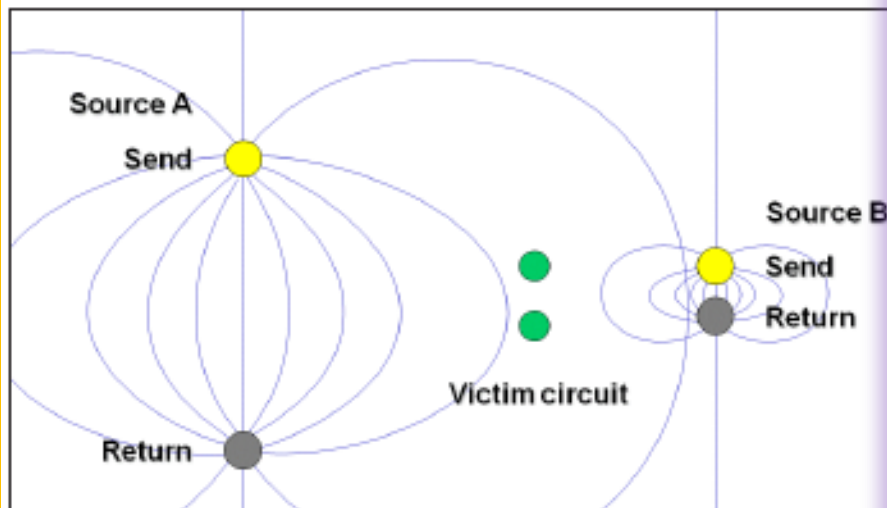
Timing/Noise Margin Issue



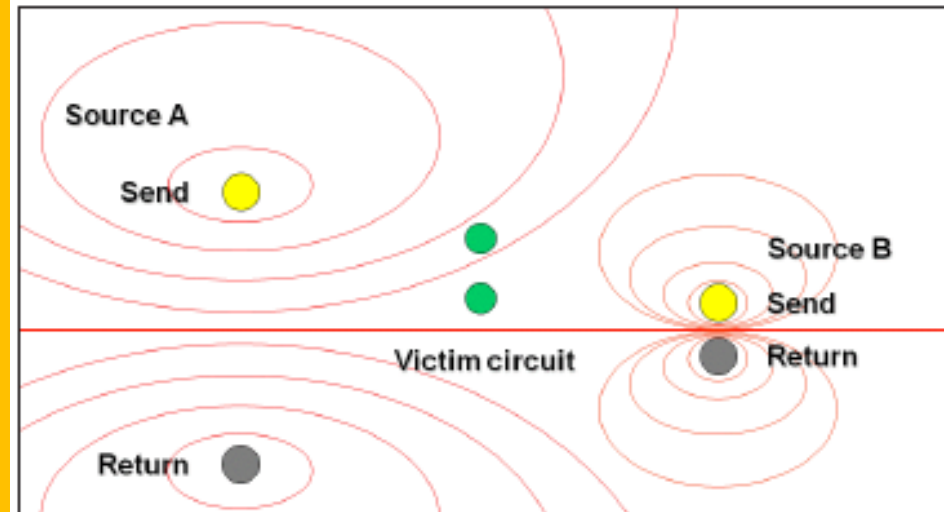
PollEx SI

◆ Crosstalk Analysis

- 3W



Source A couples to the Victim circuit more strongly than Source B, because Source B has more capacitance between its send/return conductors, so its E field is more compact and causes less stray field coupling (less stray capacitance) to the victim circuit

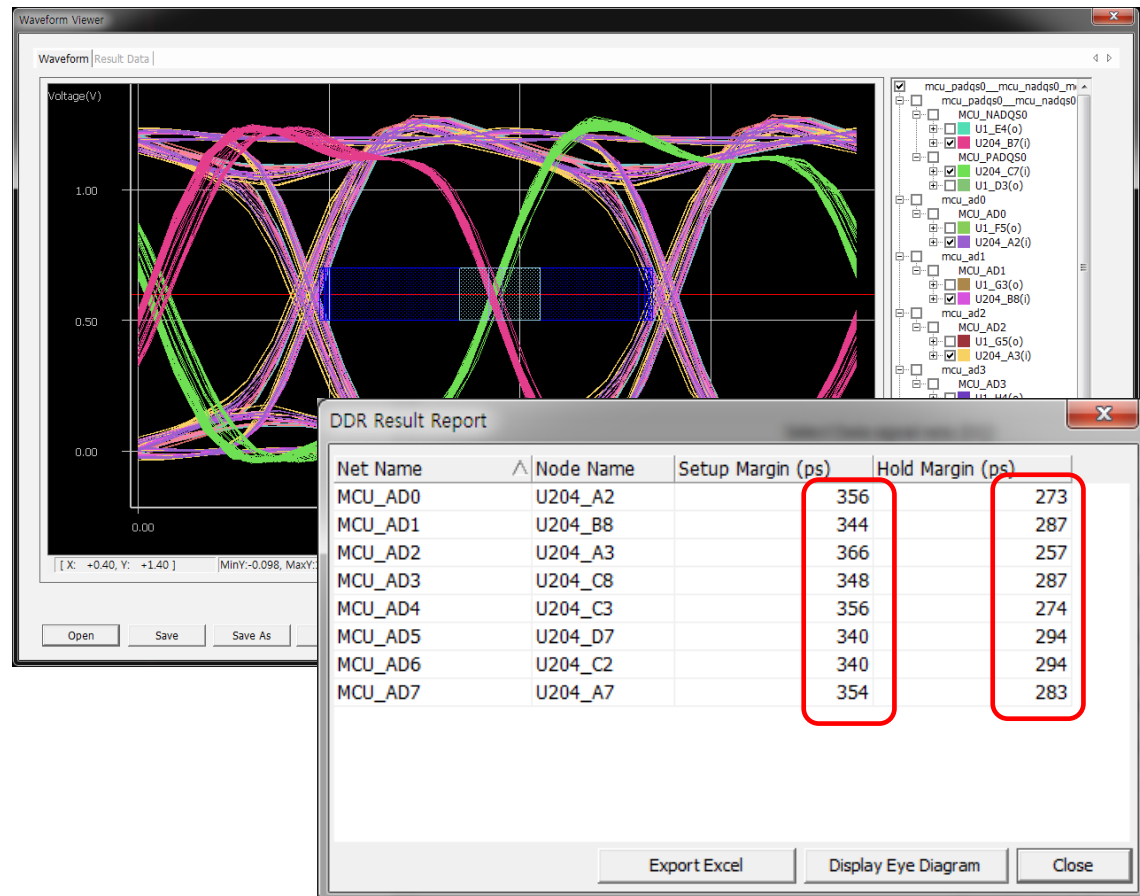
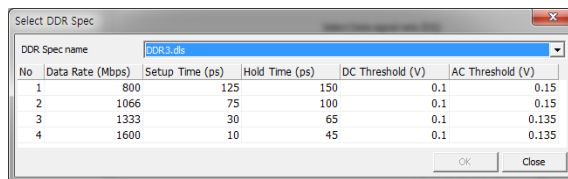
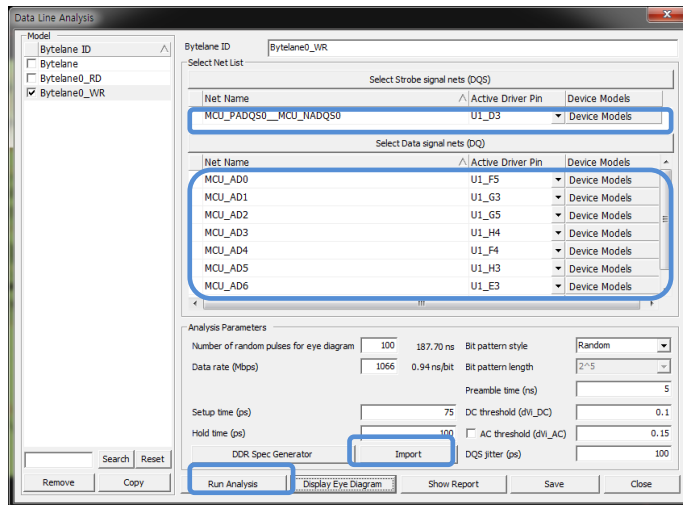


Source A couples to the Victim circuit more strongly than Source B, because Source B has more DM mutual inductance between its send/return, so its H field is more compact and causes less stray field coupling (less stray mutual inductance) to the victim circuit

PoIEx SI

◆ Data Line Analysis

- DDR Data Line의 Byte별 Analysis 일괄 수행.

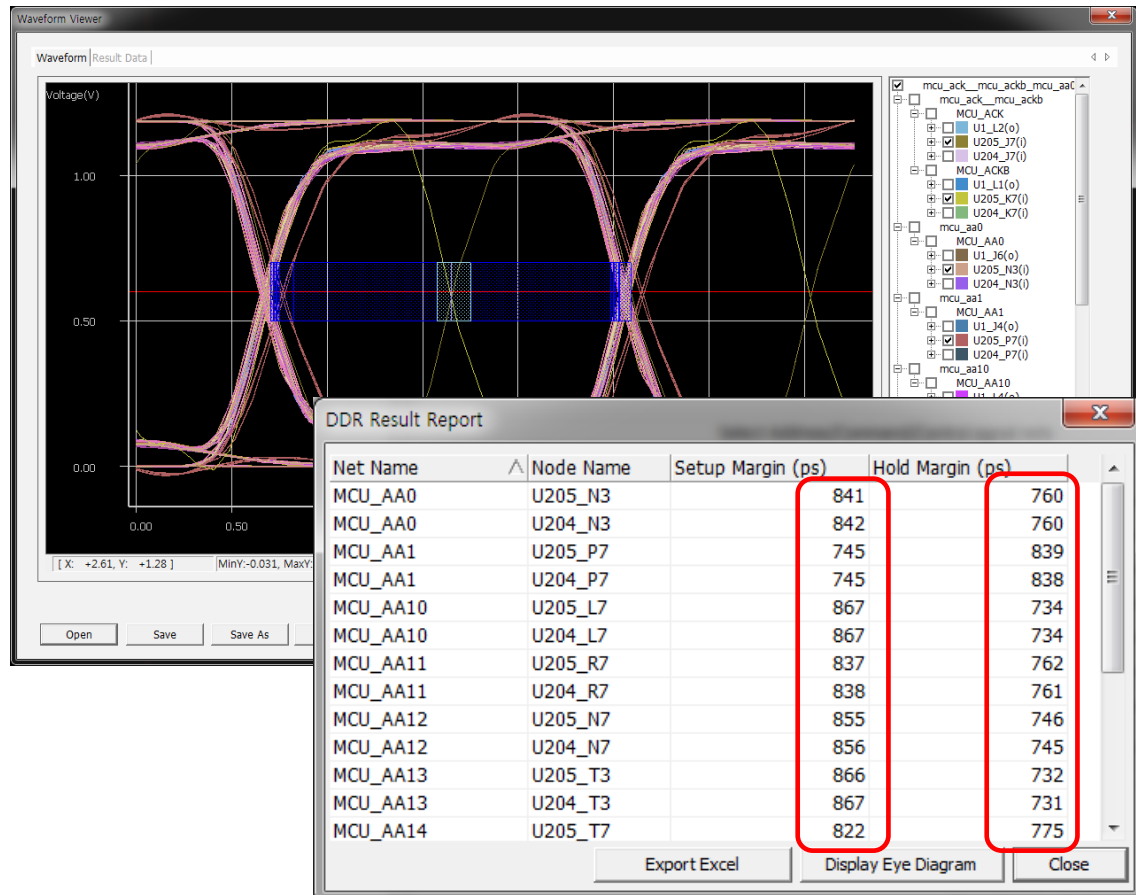
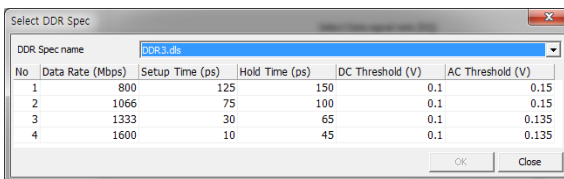
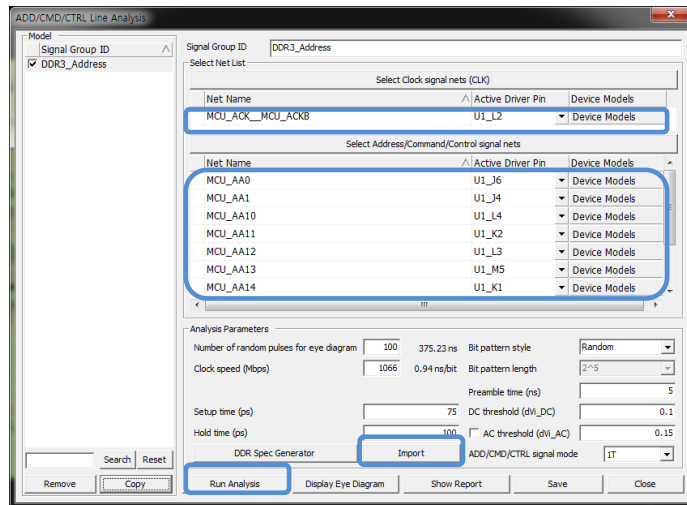


Centering을 통한 Margin 확보

PoIEx SI

◆ ADD/CMD/CNTR Line Analysis

- DDR Control Line의 Byte별 Analysis 일괄 수행.



Centering을 통한 Margin 확보

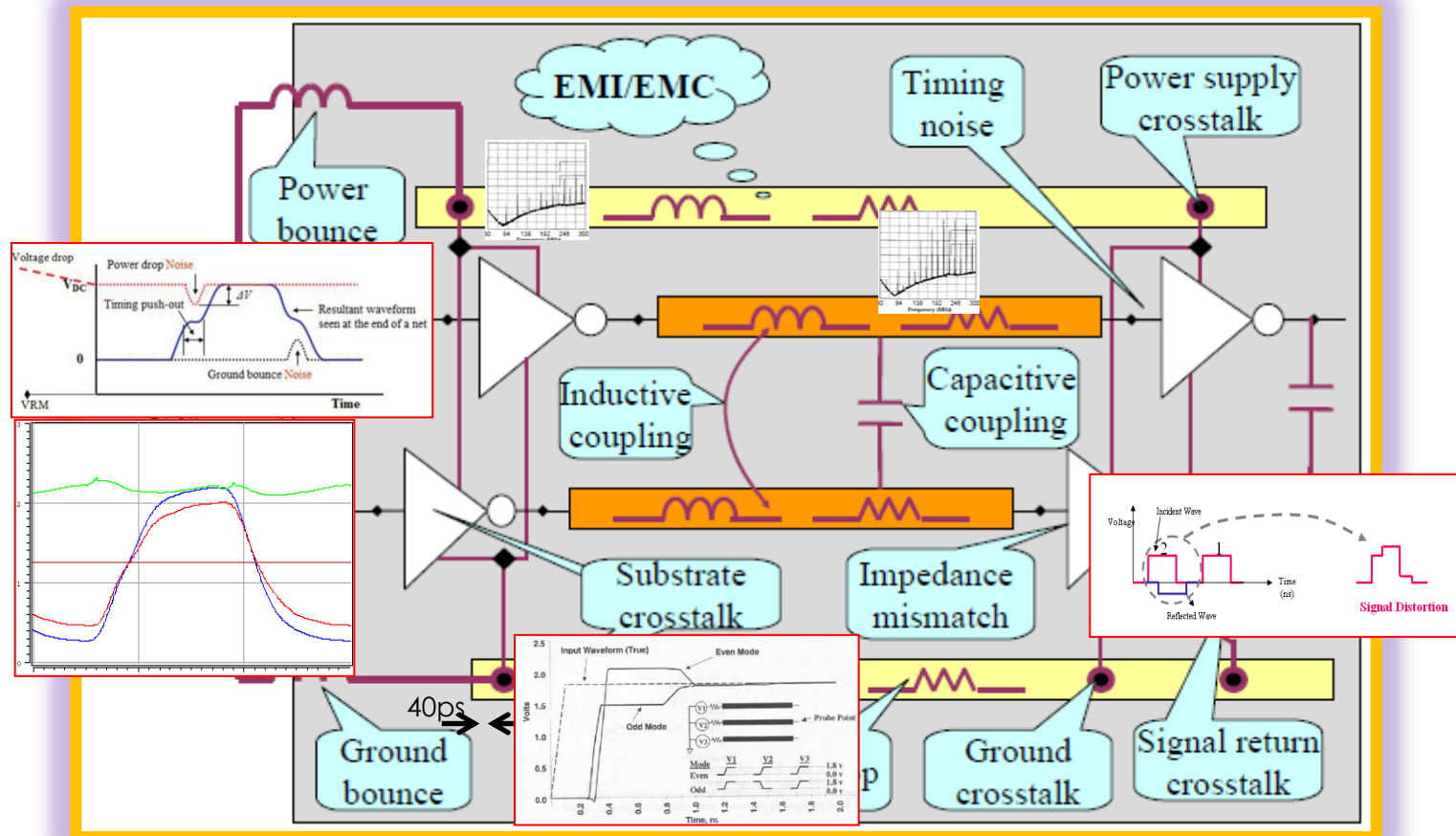
Jump Design Innovation

polliwog
corporation

Pollex SI

◆ Timing/Noise Margin Analysis

- Margin = Reflection + SSN + Crosstalk + Jitter



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◆ Read Timing Budget 예 (DDR2-667 사례)

-

PCB/Interconnect Skew Component	Setup	Hold	Units	Comments
Crosstalk	40	40	ps	-
Data Group Trace Mismatch	15	15	ps	- M/S: 7.1ps/mm, S/L:5.5ps/mm
SSN	80	80	ps	- Power Trace 구조
Termination Mismatch(V_{OH}/V_{OL})	15	15	ps	Termination mismatch error that reduces the input eye. (OCD calibration 필수)
Eye Reduction	50	50	ps	V_{REF} mismatch error, termination error, and eye reduction due to slew rate differences between DQS and DQ
Jitter	100	100	ps	온도, 전압, Corner Chip
Total Board Skew	300	300	ps	-
DRAM output skew($t_{DQSQmax}$)	240	240	ps	From DDR2-400/533/667/800 data sheet (350/300/240/200)
DDR controller input skew requirement(t_{DISKEW})	550	550	ps	Controller Spec.
Read Timing Margin	10	10	ps	Margin = Controller Requirement – DRAM – Board Skew (DRAM out + Board Skew < Controller Requirement)

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◆ Write Timing Budget 예 (DDR2-667 사례)

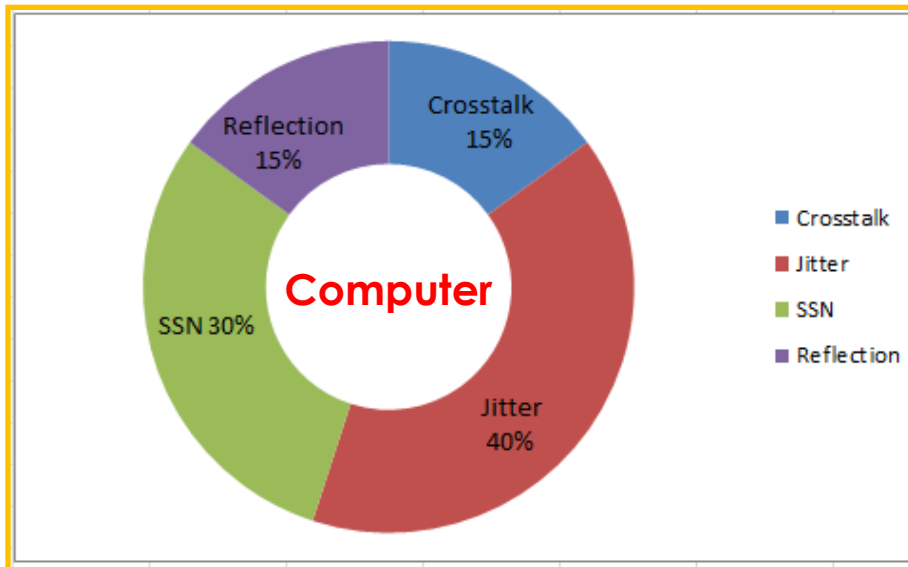
-

PCB/Interconnect Skew Component	Setup	Hold	Units	Comments
Crosstalk	40	40	ps	-
Data Group Trace Mismatch	15	15	ps	- M/S: 7.1ps/mm, S/L:5.5ps/mm
SSN	80	80	ps	- Power Trace 구조
Termination Mismatch(V_{OH}/V_{OL})	15	15	ps	Termination Mismatch Error that reduces the input eye. (OCD calibration 필수)
Eye Reduction	50	50	ps	V_{REF} mismatch error, termination error, and eye reduction due to slew rate differences between DQS and DQ
Jitter	100	100	ps	온도, 전압, Corner Chip
Total Board Skew	300	300	ps	-
DDR Controller output skew($t_{DQSQmax}$)	290	290	ps	DDR Controller Spec.
DDR controller Output setup/hold	750	750	ps	Assumes Center Align
DRAM Input setup/hold (t_{DS}/t_{DH}) Requirement	100	175	ps	From DDR2 data sheet(400/533/667/800) (150-275/100-225/100-175/50-125)
Write Timing Margin	60	-15	ps	Margin = DDR controller – DRAM Requirement – DDR controller skew - Board Skew (Controller Output - Board Skew > DRAM Requirement)

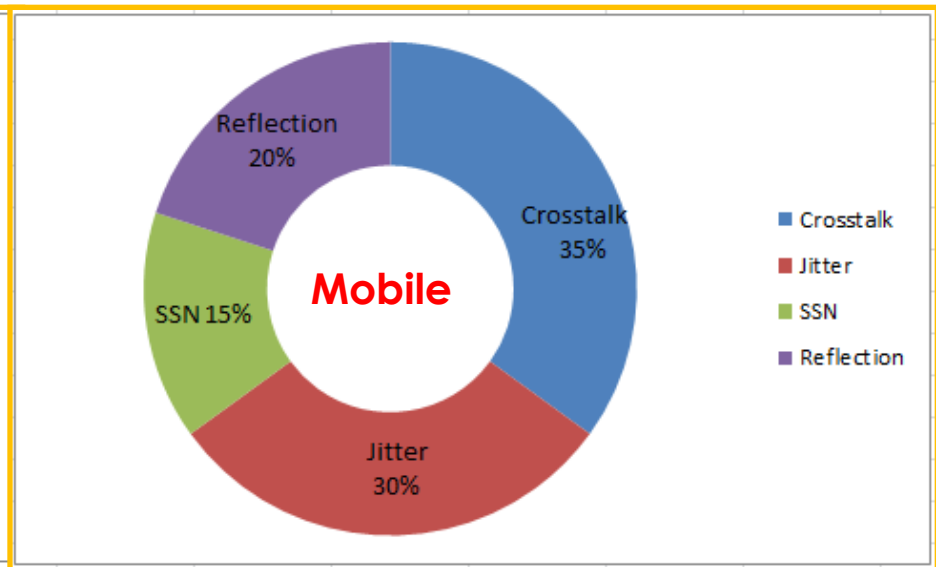
Pollex SI

◆ Margin distribution policy

- Do not have blind faith in a Design Guide from Vendor.



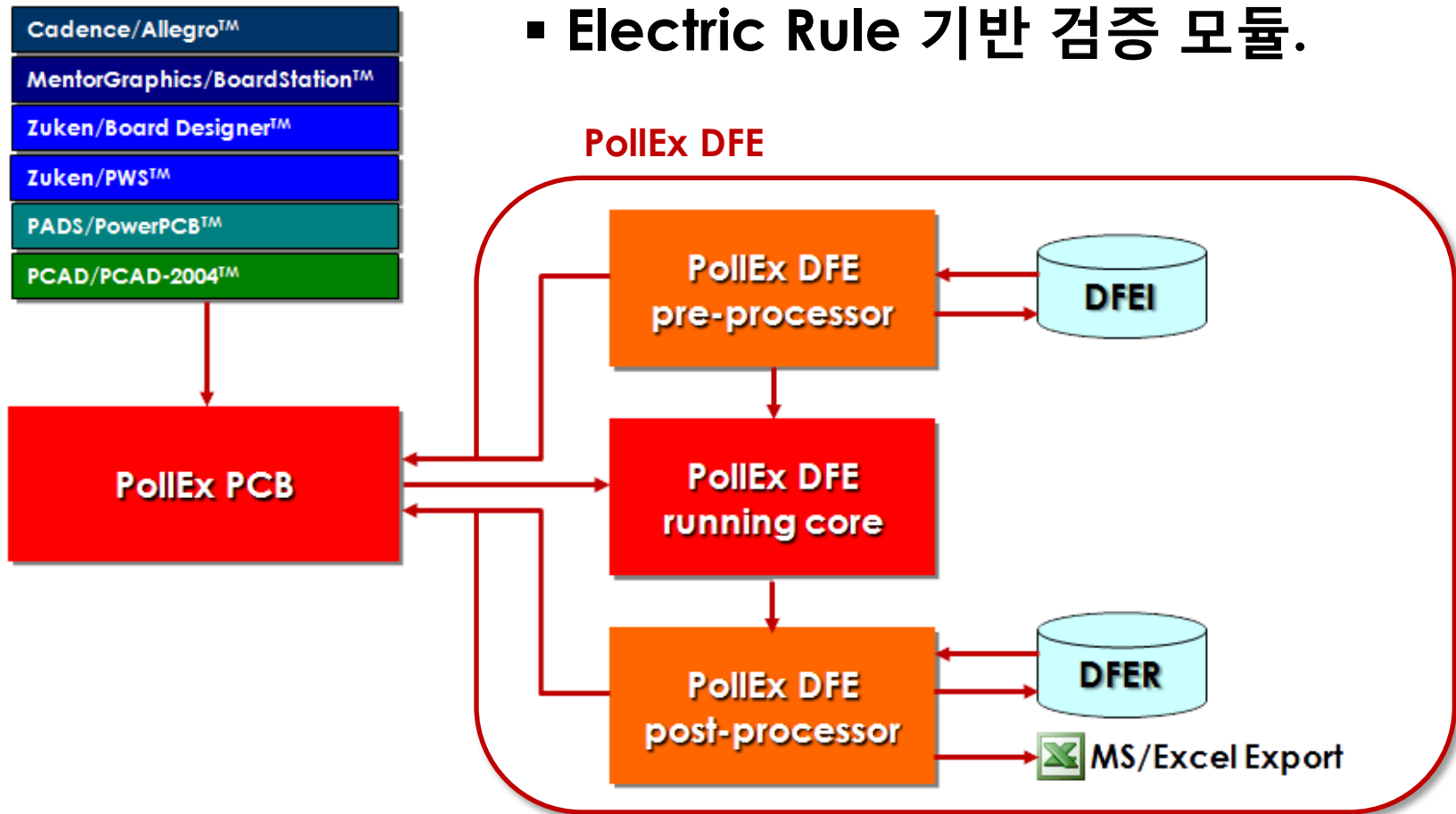
- Termination required
- Net spacing: 3W
- Appropriate Decoupling Capacitor



- No termination(Except Clock)
- Net spacing: 2W
- Tight length matching

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▪ Electric Rule 기반 검증 모듈.

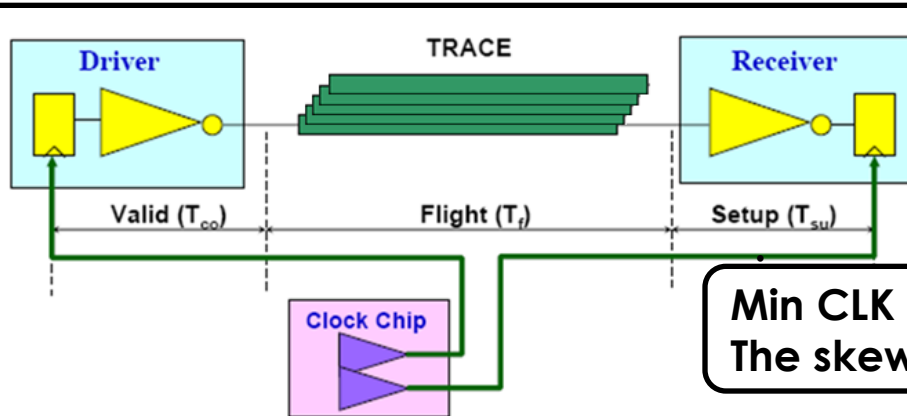


Pollex DFE

◆ Data Transfer Method

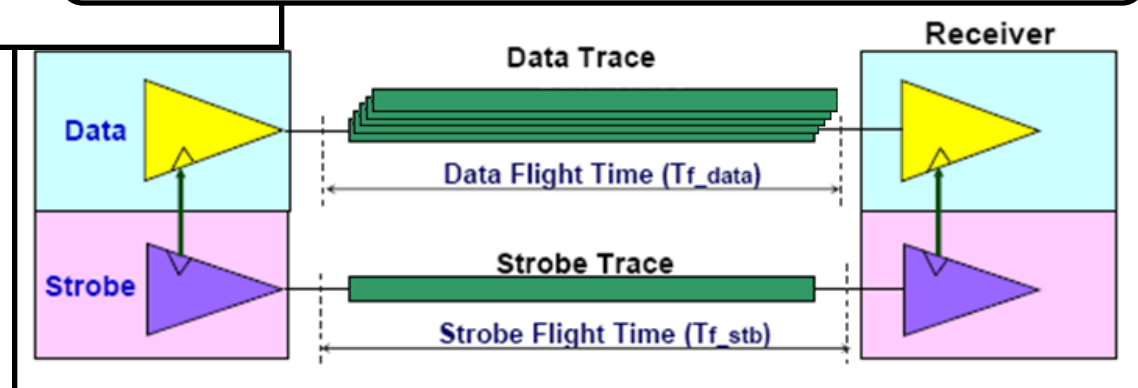
Common Clock Method

Min CLK Period = Valid + **Flight** + Setup + Jitter + Skew
Flight Time restricts Frequency of operation



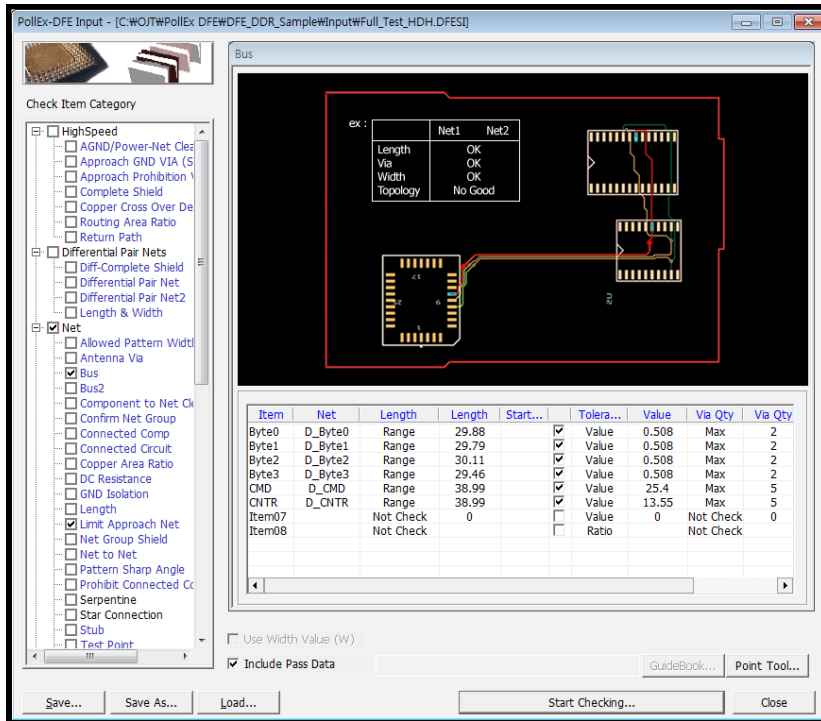
Source Sync Method

Min CLK Period = No limitation theoretically
The skew between Tf_data and Tf_stb is important



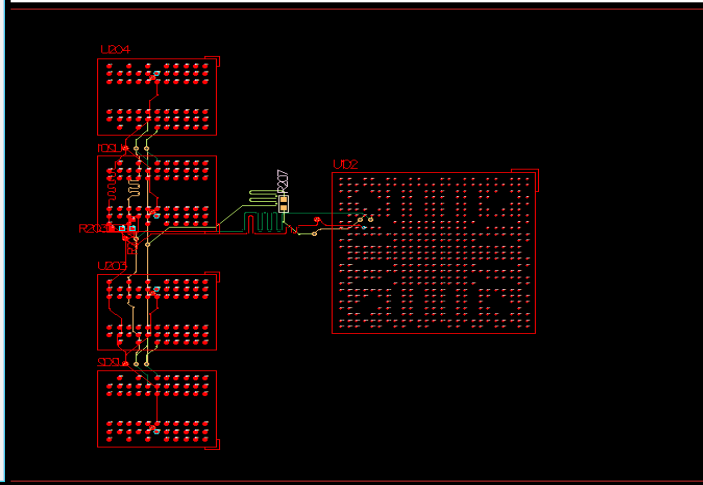
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◆ BUS



Check Items:

- Trace length matching with tolerance.
- Via quantity.
- Trace width.

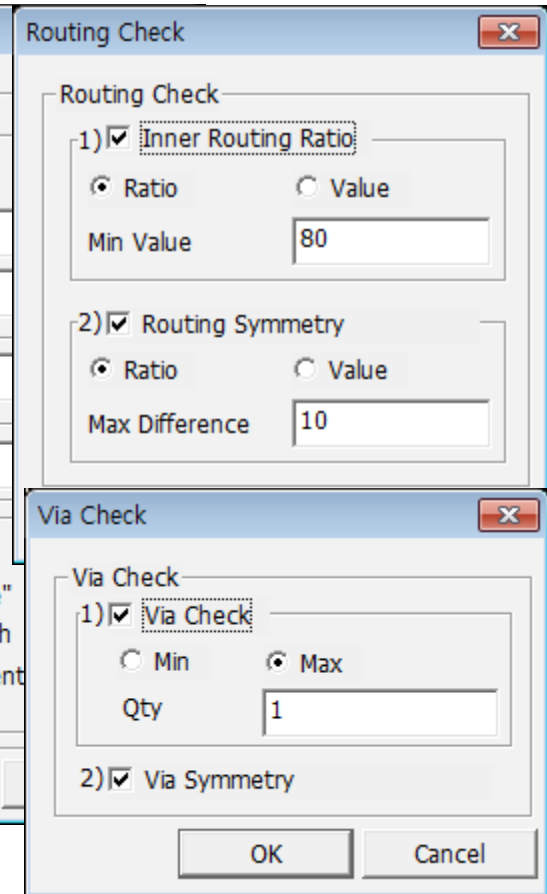
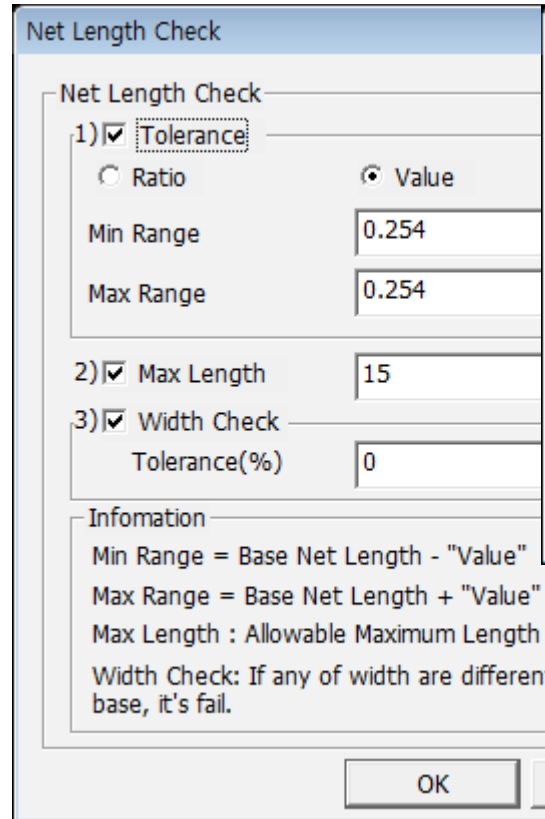
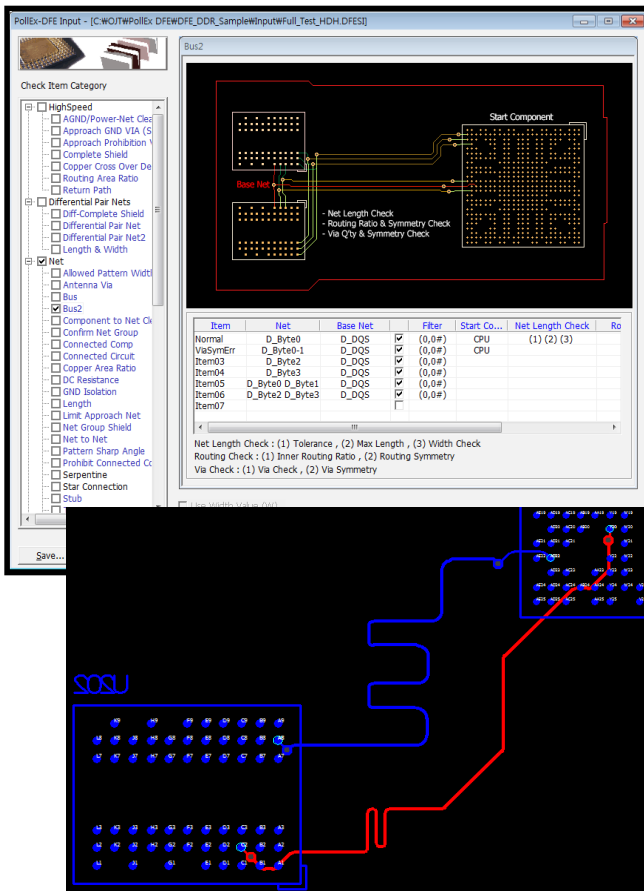


Item	Net	Length	Length	Start Component	Tolerance	Value	Via Qty	Via Qty	Width
Item01		Not Check			Ratio		Not Check		Not Check
<div> <div>Not Check</div> <div>Min</div> <div>Max</div> <div>Range</div> <div>Longest Length</div> <div>Combination Length</div> </div>									

PoIlex DFE

◆ BUS2

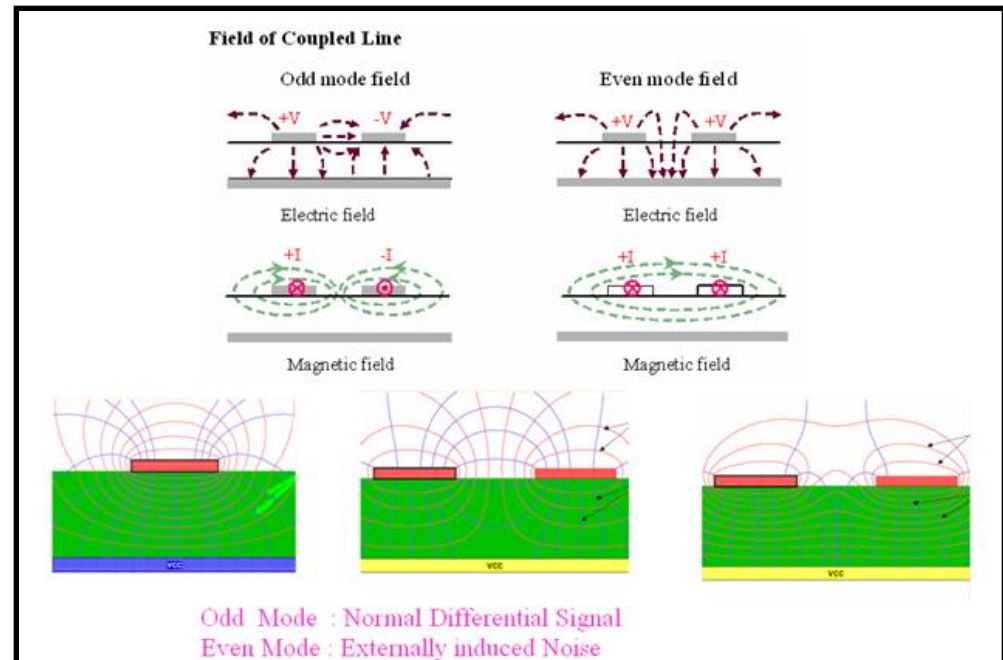
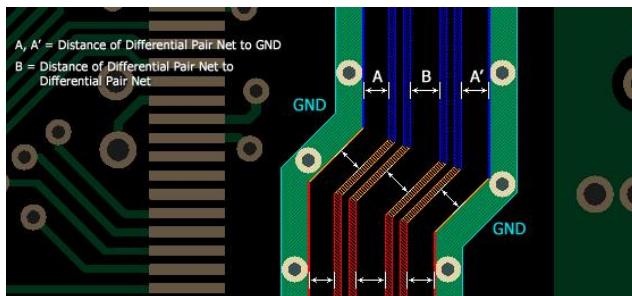
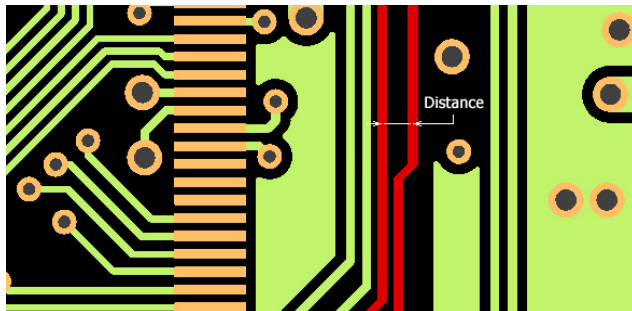
- Routing symmetry between strobe and data is Key.



Pollex DFE

◆ Differential Signalling

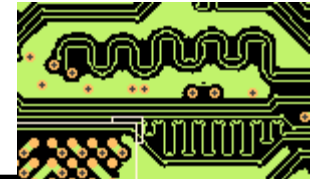
- Length matching between P/N signals.



Item	Net	Start Comp	End Comp	Filter	Toleran...	Ratio(%)	Segment Distance	Pin Escape	TP	TP Distance	Nut Shape Anti-Pad	Except Layer
Item01				<input type="checkbox"/>		80	<input type="checkbox"/> Minimum Distance	0	<input type="checkbox"/>		Not Check	

Item	Net Group	Filter	GND Net Group	Pin Escape	Via Escape	Net Clearance	Shield Distance	Tolerance(%)	Show Segment .
Item01									<input type="checkbox"/>

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◆ Serpentine

- Routing symmetry between strobe and data is Key.

PCI SIG **Trace Symmetry & Matching** Layout considerations

- No matching needed pair-to-pair
- Match each differential pair per segment
 - ✓ Match overall length ≤ 5 mils (recommended)
 - ✓ Symmetric routing for each pair

Match near mismatch

Preferred matching

≤ 45 mils

Alternative matching

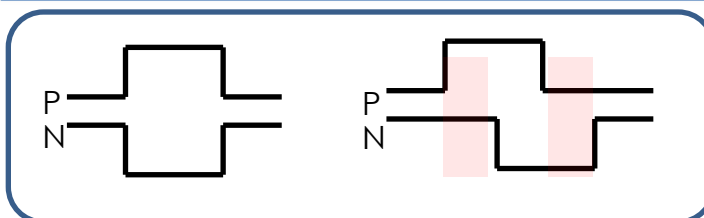
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PCI SIG **Bends and Small Serpentes** Layout considerations

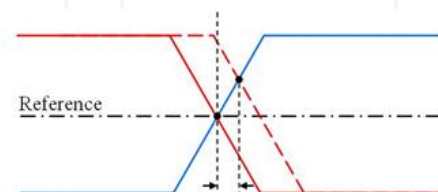
- Avoid tight bends
 - ✓ No 90° bends; impact to loss and jitter budgets
- Keep angles $\geq 135^\circ$ (a)
- Maintain adequate air gap
 - ✓ $A \geq 4x$ the trace width
- Lengths of B, C $\geq 1.5x$ the width of the trace
- Serpentines length is at least $3w$ for jog

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Item	Net	Filter	Start Component	Symmetry Check	Bending Shape Check	Serpentine Shap...
Item01				<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>



Differential
signaling
scheme



Jump > Design Innovation

polliwog
corporation

Pollex DFE

◆ Serpentine

PCI SIG **Layout considerations** **PCI EXPRESS**

AC Coupling Caps

- Size: 0402 **best**, 0603 **ok**
- No 0805 size or C-packs
- Symmetric placement best

- Cap size: 0.1uF **best**
- Same sizes for both D+/D-
- Cap location:
 - ✓ Along Tx pairs on system board
 - ✓ Along Tx pairs on add-in card

Symmetry

Symmetry Check

- ☒ Serpentine Start Position Check : 5
- ☒ Discrete Component Symmetry Check : 0.127
- ☒ Via Symmetry Check : 0.127
- ☒ Component Existence Check

OK Cancel

Bending Shape

Bending Shape Check

- ☒ Min A(W) : 3
- ☒ Min B(W) : 2
- ☒ Min C(W) : 2
- ☒ Min Angle : 135

OK Cancel

Serpentine Shape

Serpentine Shape Check

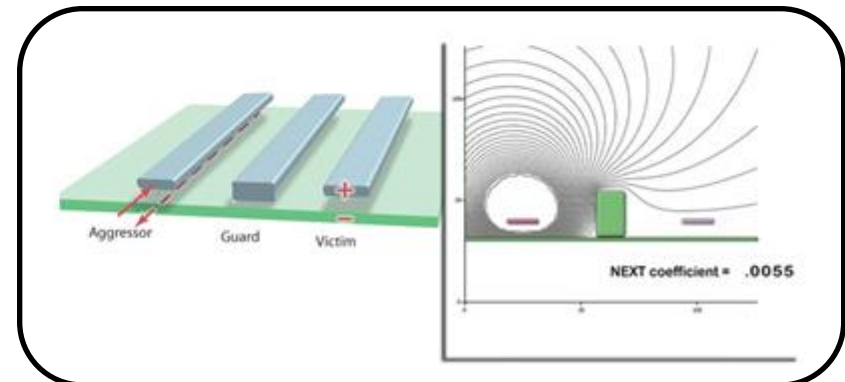
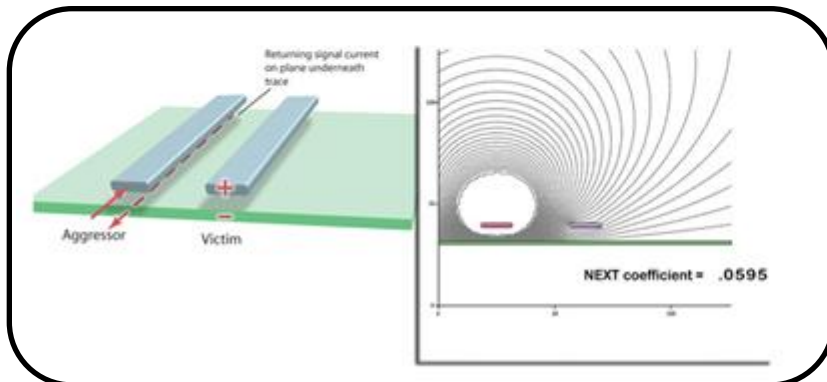
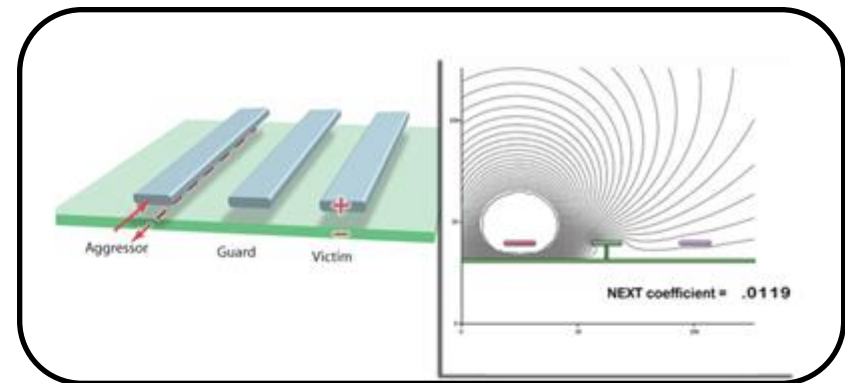
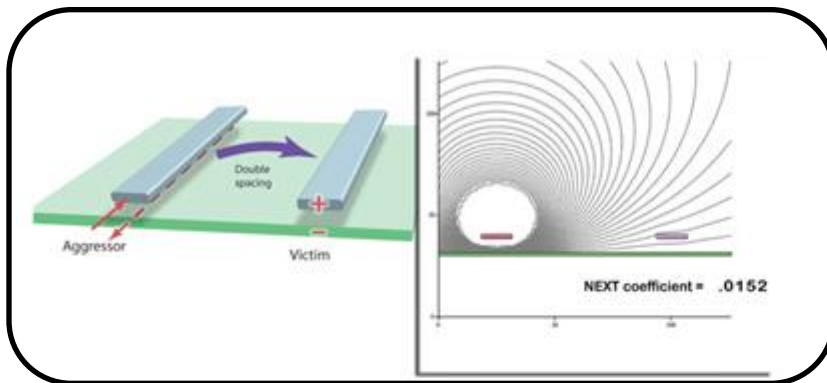
- ☒ Length1 Check : A=B=C=D(W) : 2
- ☒ Length2 Check : E=F=G(W) : 3
- ☒ Max Serpentine Height : H(W) : 1
- ☒ Max Serpentine Length Check : 2.54
- ☒ Max Serpentine Spacing : S1(S) : 2
- ☒ Serpentine Angle Check : 135

OK Cancel

Pollex DFE

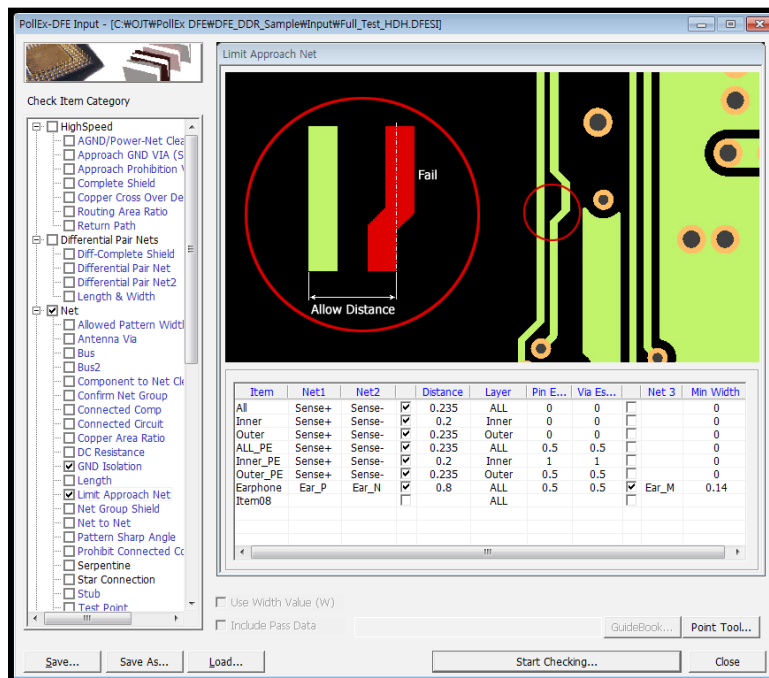
◆ Ground Barrier Effect

- Audio signal needs ground barrier in order to prevent noise coupling



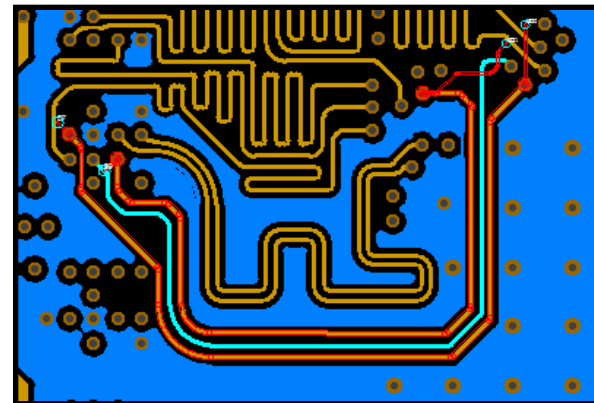
PoIEx DFE

◆ Limit Approach Net



Check Items:

- Separation between Net1 and Net2.
- Ground barrier existence.
- Ground barrier minimum width.

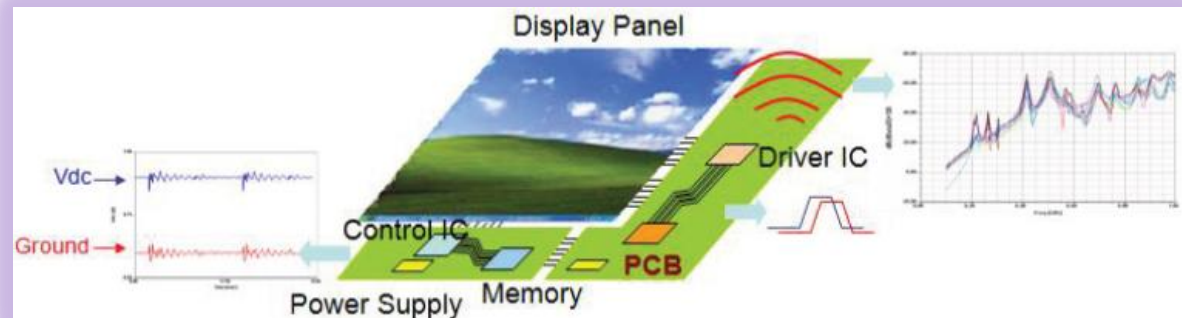
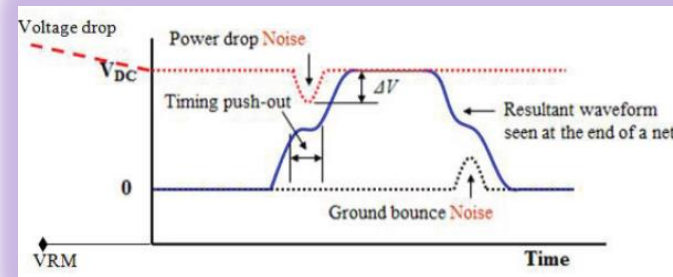
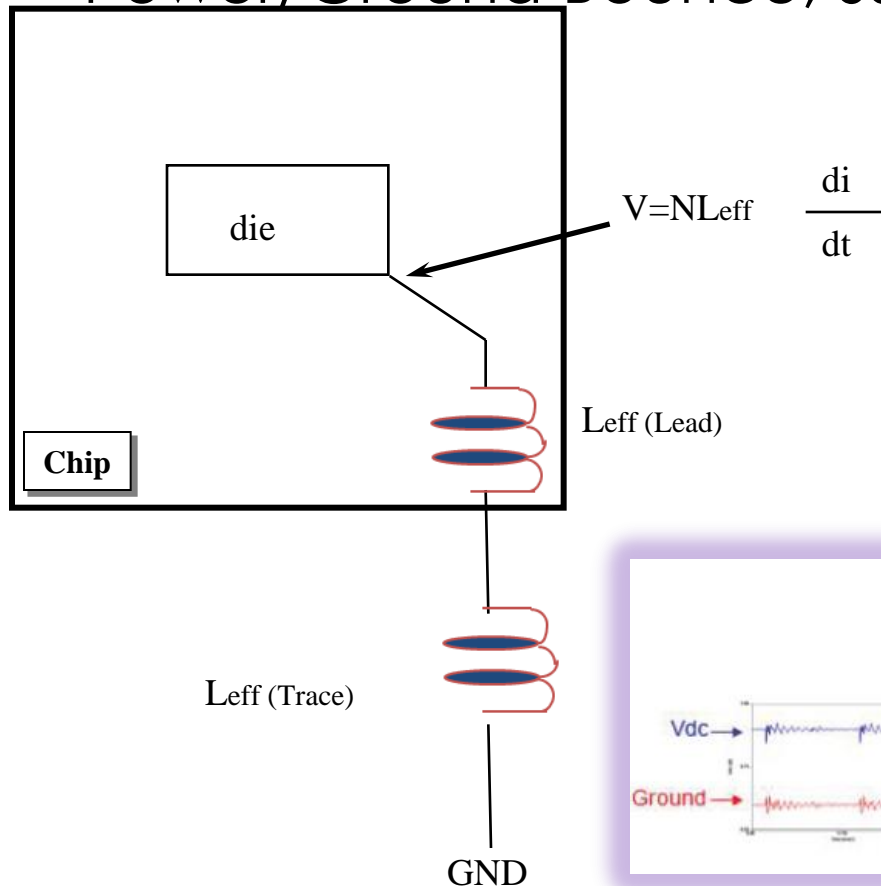


Item	Net1	Net2	Distance	Layer	Pin Escape	Via Escape	Net 3	Min Width
Item01		<input type="checkbox"/>		ALL			<input type="checkbox"/>	

Pollex DFE

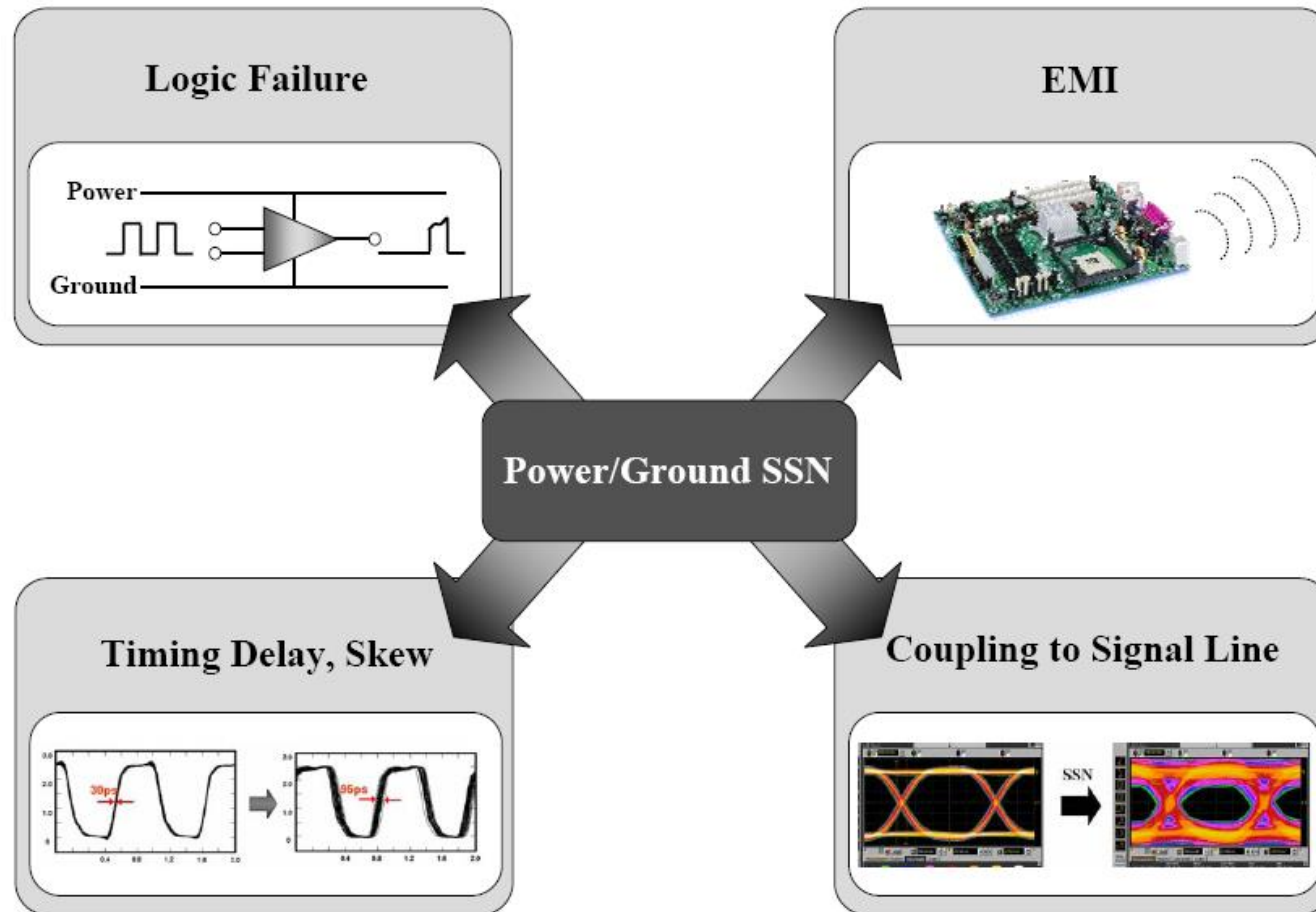
◆ Power Integrity

- Power/Ground Bounce, SSN/SSO



Pollex DFE

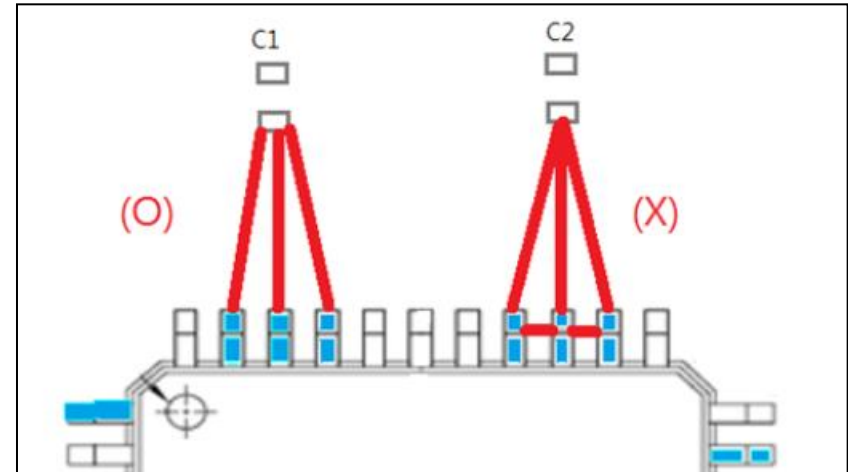
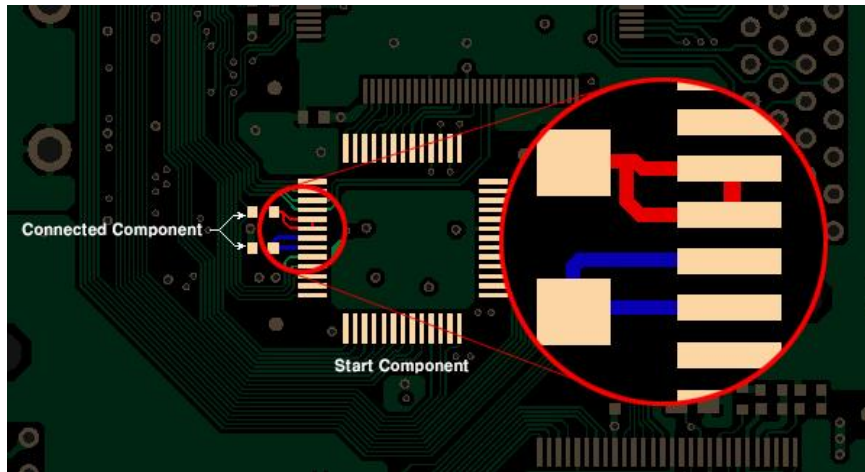
◆ Problems by Power/Ground SSN



Pollex DFE

◆ Star Connection

- In case of sharing one capacitor, connection should be isolated .

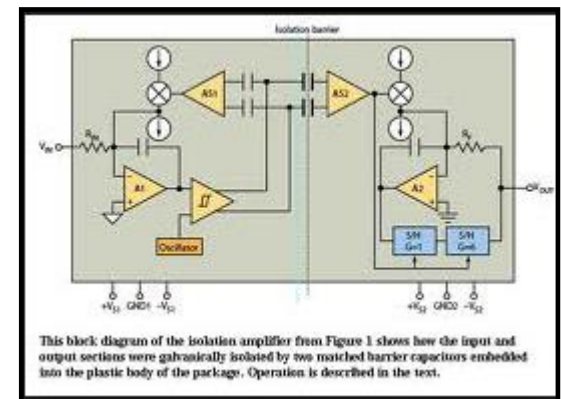
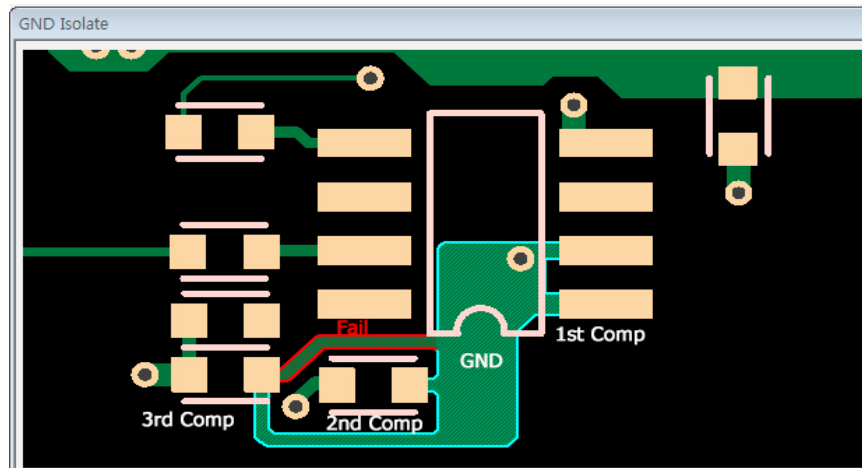
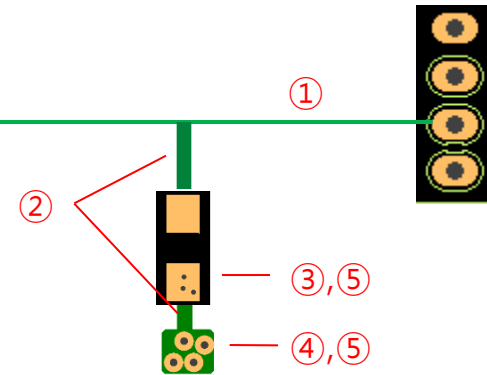


Item	Star Component	Connected Component	Check Net
Item01			

Pollex DFE

◆ GND Isolation

- ESD discharge path should be isolated and direct connect to main ground.

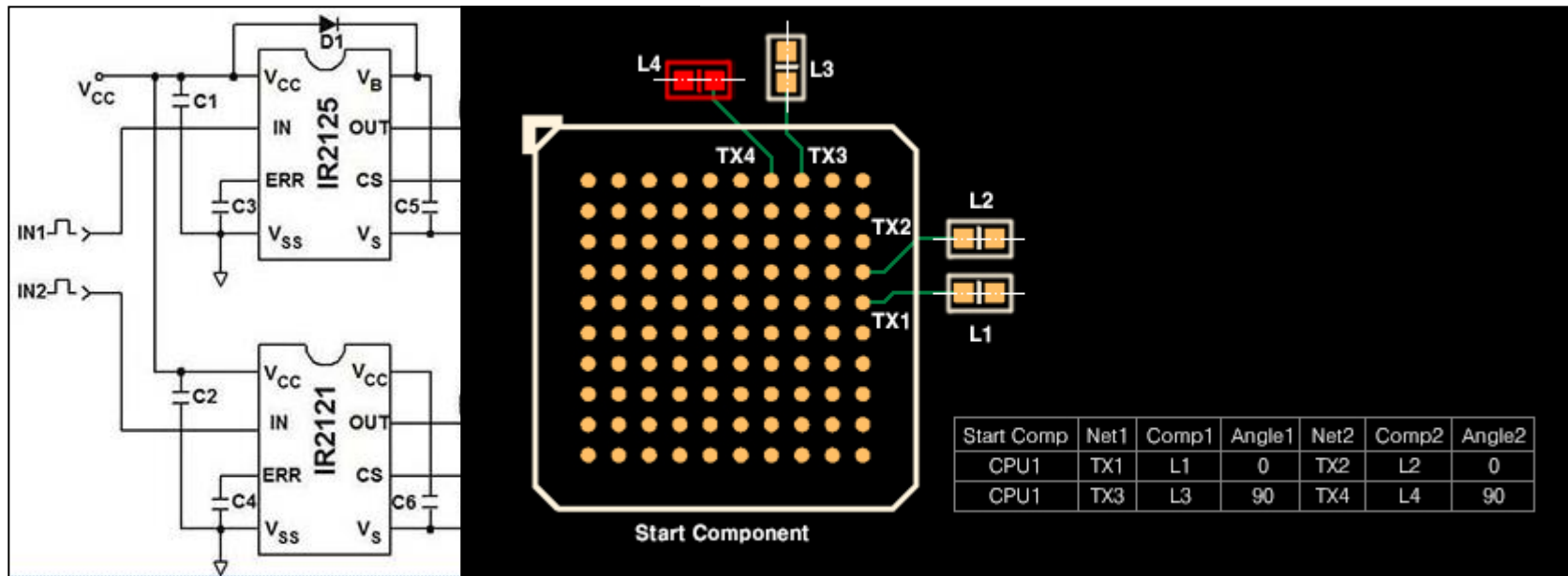


Item	Check Pins	MGND-Count	GND Isolation	Via Location	Distance
Item01			<input type="checkbox"/>	<input type="checkbox"/>	

PoIlex DFE

◆ Component Direction

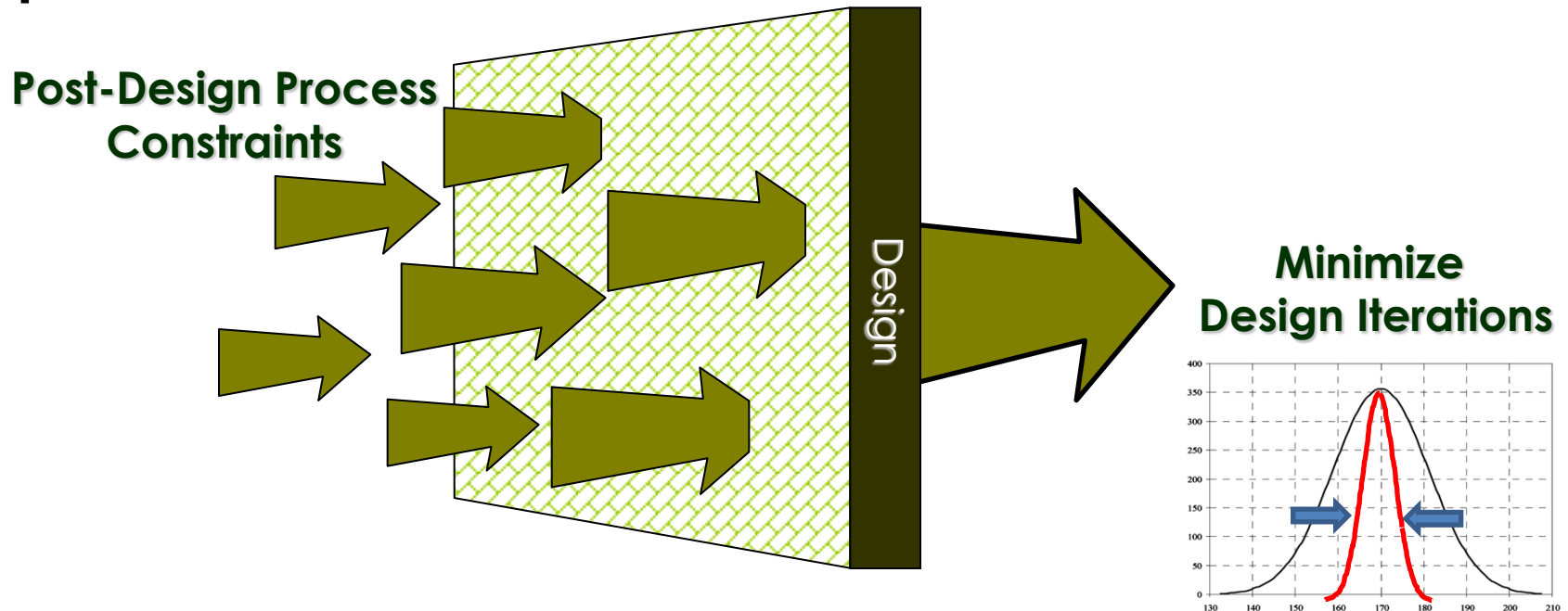
- Check passive devices' placement angles.



Item	Start Component	Angle	Net1	Comp1	Net2	Comp2
Item01						

PollEx DFE

◆ Expectation for PollEx DFE



Consider engineering faults in early design stages.

- Accumulate Knowledge for Engineering.
- Save Time-Consuming Cost. (Time to Market)
- **Get Superior Competitive Power to Competitors.**

Thank You !

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