

Accelerate Your FPGA-Based DSP Designs

Agenda

- Different DSP systems have different requirements
- 'TOTAL' 28-nm DSP solutions
 - Variable-precision DSP architecture
 - DSP Builder Advanced Blockset
 - Video design framework
 - Comprehensive floating-point IP
- Summary



FPGA DSP Designs

Span Performance, Precision, IP, Tools Requirements

9-Bit Precision

100 GMACS

Floating-Point Precision

TERAFLOPs



**Video
Surveillance**



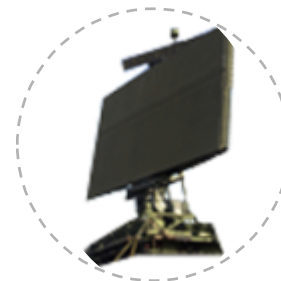
**Broadcast
Systems**



**Wireless
Basestations**



**Medical
Imaging**



**Military
Radar**



**High-Performance
Computing**

HDL

Video IP

FIR, FFT, NCOs

MATLAB/SIMULINK

Floating-Point Functions

Total DSP Portfolio at 28 nm

Variable-Precision
DSP

DSP Builder
Timing-Driven
Simulink Synthesis

Total
DSP Portfolio
at 28 nm

Video Design
Framework

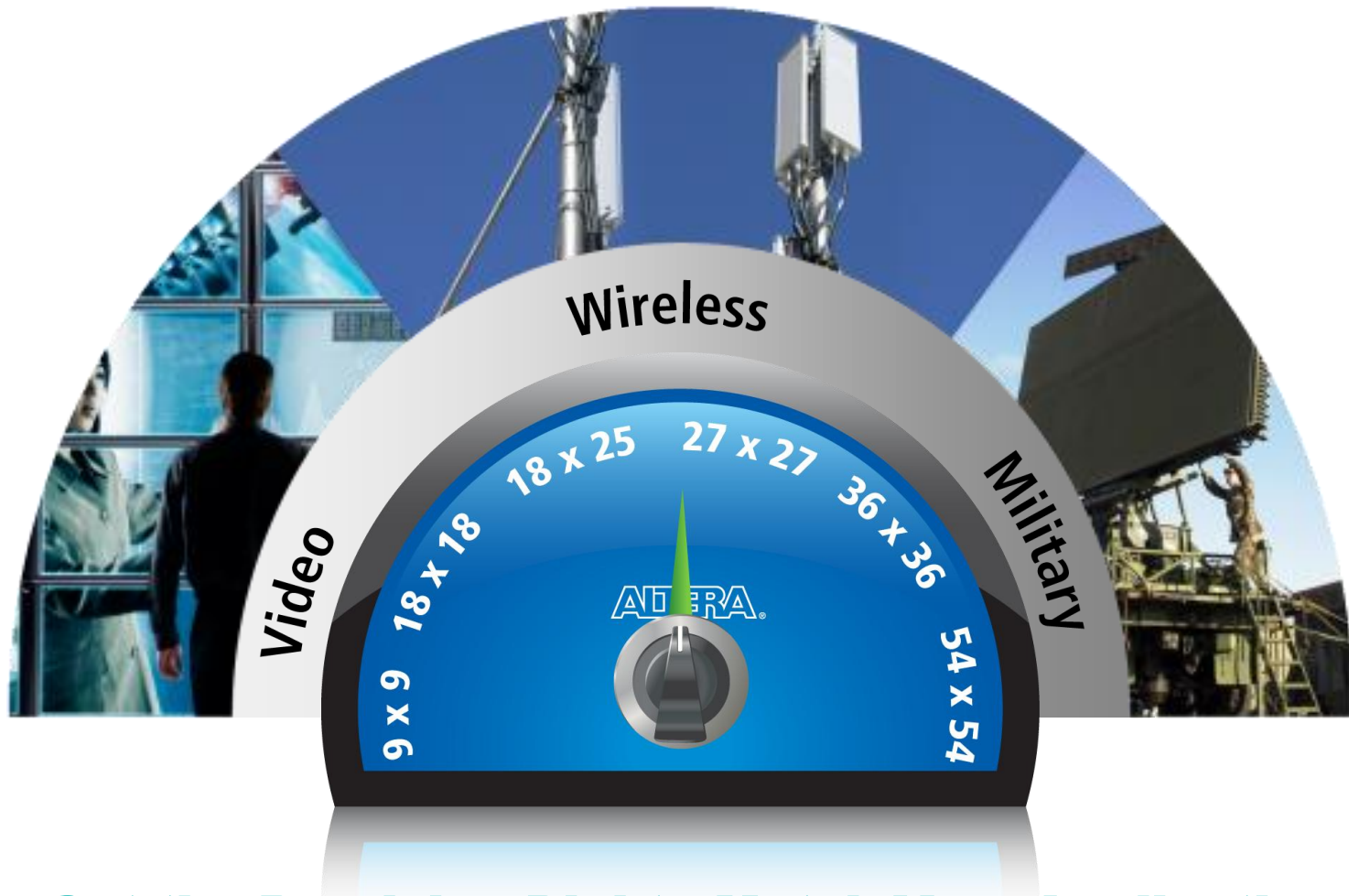
Comprehensive
Floating-Point IP

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Industry's First Variable-Precision DSP Block



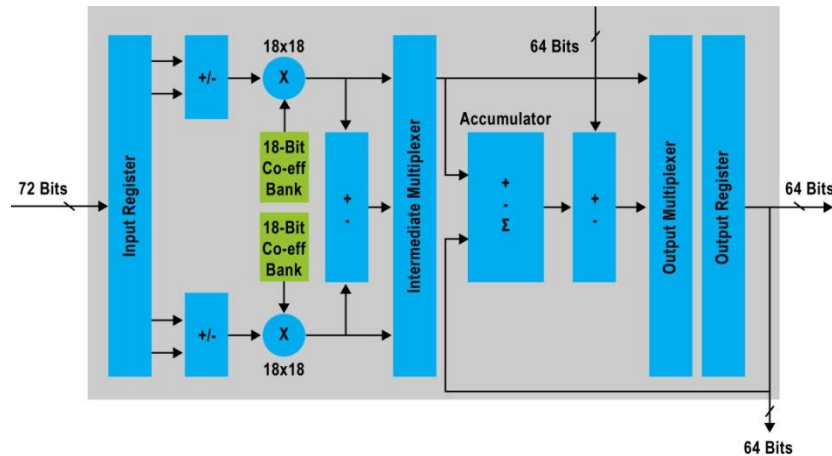
Set the Precision Dial to Match Your Application

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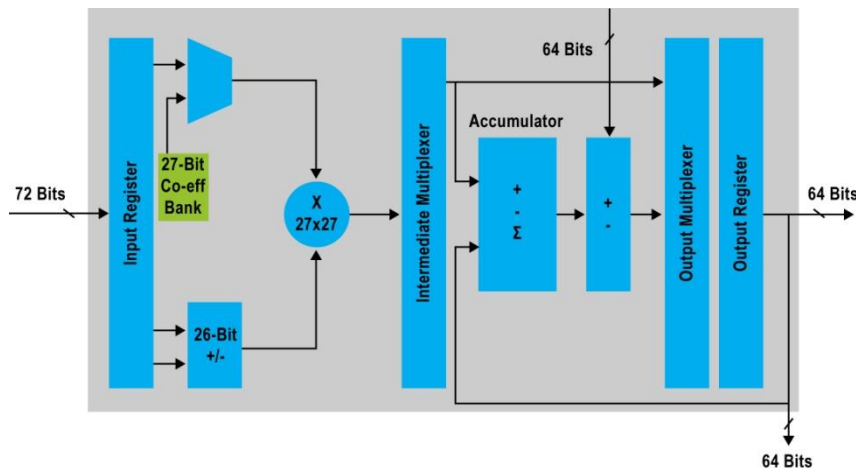
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First Variable-Precision DSP Block



**18-Bit
Precision
Mode**



**High-
Precision
Mode**

First DSP Architecture With Two Native Precision Modes

Widest Range of DSP Precision

Single Variable-Precision DSP Block	Single Competing 18x25 DSP Block
Three independent 9x9	x
Two 18x18 in the sum mode	x
Two 18x18 – independent 32-bit resolution	x
One independent 18x25 or 18x36	18x25 ONLY
One independent 27x27	x

Cascade Mode	Variable-Precision DSP Block Count	Competing 18x25 DSP Block Count
One independent 36x36	2	4
One independent 54x54	4	9
18x18 complex multiply	2	4
18x25 complex multiply	3	4
18x36 complex multiply	4	8
27x27 complex multiply	4	8



Variable-Precision DSP Block: Advantages

Altera's 28-nm DSP block:

- Allows user-programmable variable-precision signal processing
- Provides for the most efficient implementation of FIR and FFT structures across various bit widths
- Efficiently supports floating point

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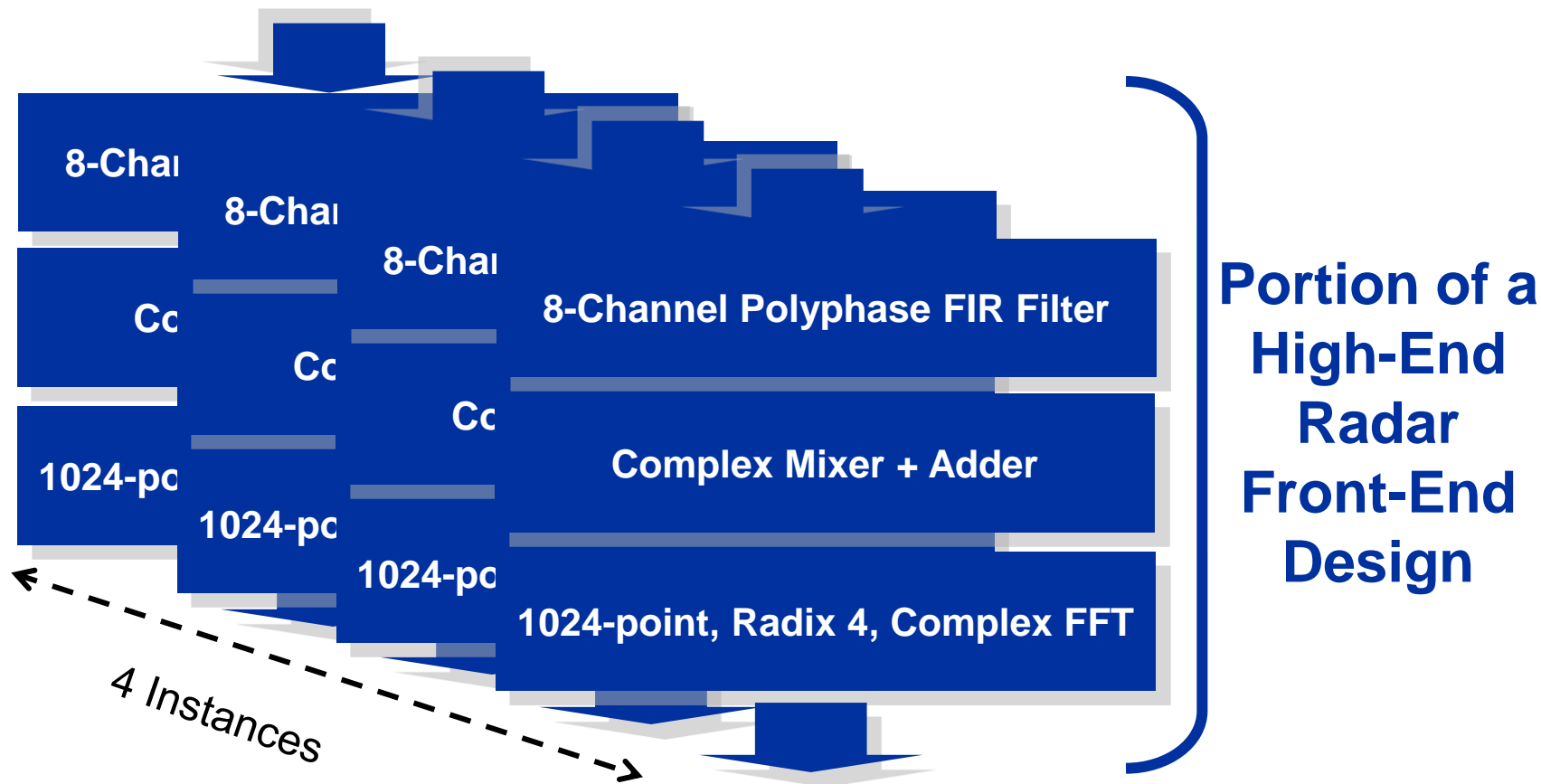
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DSP Builder Advanced Blockset Advantage

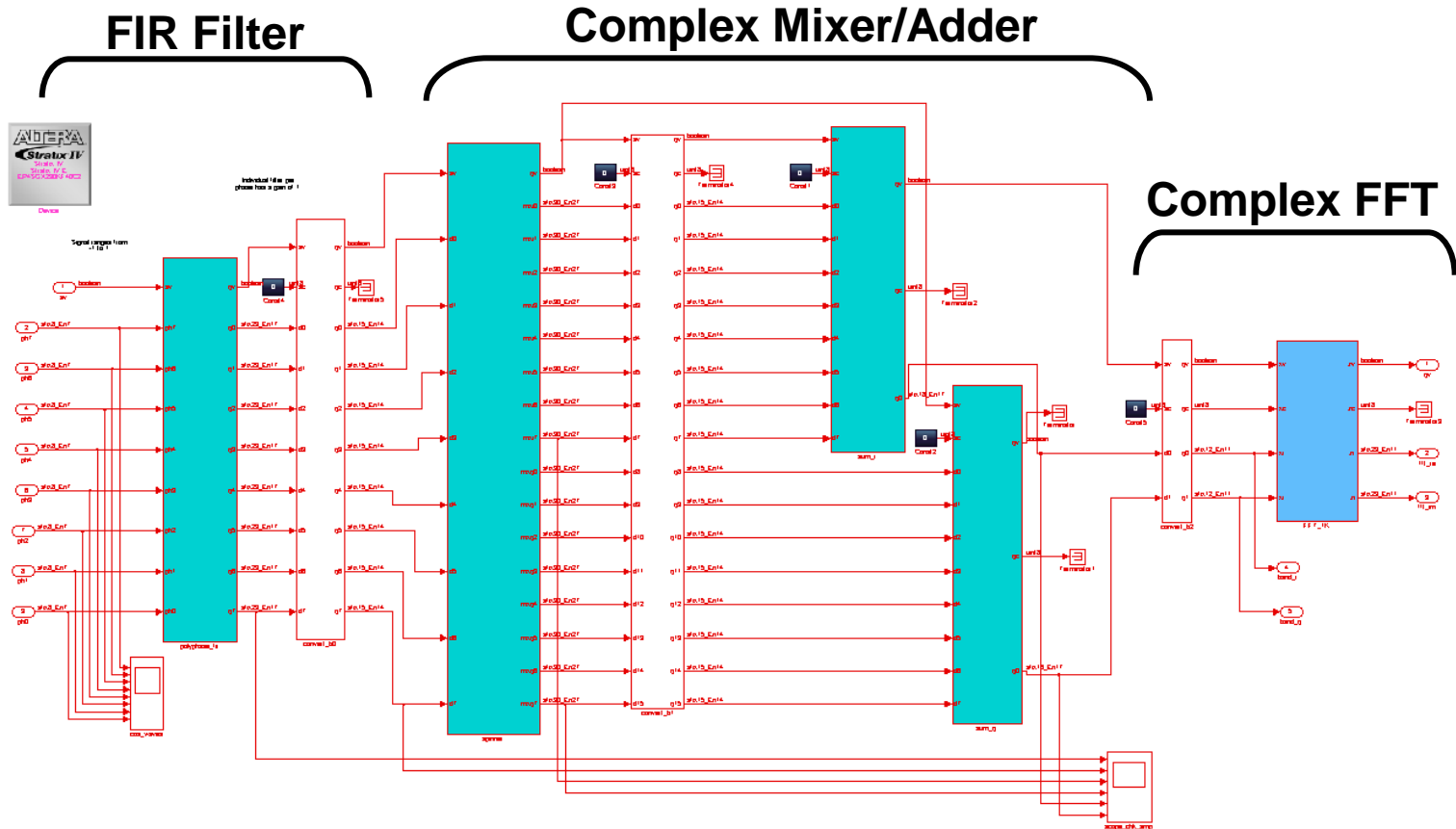
Building a High-Performance DSP Datapath



This Design Needs to Close Timing at 350 MHz.

DSP Builder Advanced Blockset Design Flow

Build the Design in MATLAB/Simulink



High-Level Simulink Design Description

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DSP Builder Advanced Blockset Design Flow

Set the Desired f_{MAX} Within Simulink

```
clear variables      % Using clear variables instead of clear all avoids the annoying but
                    % unharmedful 'mip_sfnc_common.dll was not found' error message.

close all

%% User and Test parameters

% Design parameters
DS_factor = 8;      % downsampling factor
SampleRate = 350;   % per phase, aggregated sampling rate is DS_factor * SampleRate,

bw_source = 8;
bw_coeff = 11;     % 11 bits provides a min 55dB SNR which is needed due to oversampling ga
bw_polyph_DR = 1+ bw_coeff + log2(DS_factor) ;      % Polyphase filter dynamic range, one

bw_mixer_coeff = bw_polyph_DR;    %16
bw_mixer_out = bw_polyph_DR;
bw_adder_out = bw_mixer_out+ log2(DS_factor);

bw_fft_input = 1+ bw_coeff;
bw_output = 23;

% User/test parameters
```



Set f_{MAX} Constraints Within the High-level Simulink Design Description

DSP Builder Advanced Blockset Design Flow

Push-Button Implementation

The image shows a screenshot of the Quartus II software interface. On the left, the 'Compilation Report - Fitter Summary' window is open, displaying the following information:

- Fitter Status: Successful - Wed Jan 27 20:19:31 2010
- Quartus II Version: 9.0 Build 132 02/25/2009 SJ Full Version
- Revision Name: Radar_x4_350
- Top-level Entity Name: Radar_top
- Family: Stratix IV
- Device: EP4SGX230FF35C2X
- Timing Models: Preliminary
- Logic utilization: 26 %
- Combinational ALUTs: 29,225 / 182,400 (16 %)
- Memory ALUTs: 1,080 / 91,200 (1 %)
- Dedicated logic registers: 52,619 / 182,400 (29 %)

On the right, the 'Compilation Report - Slow 900mV 85C Model...' window is open, showing a table titled 'Slow 900mV 85C Model Fmax Summary':

Fmax	Restricted Fmax	Clock Name	Note
1	304.79 MHz	bus_clk	
2	374.11 MHz	clk	

The value '374.11 MHz' in the second row of the table is circled in blue. The '5C Model...' window is also visible in the background.

Large (60K LE) Design Achieves >350 MHz Without HDL Design Tweaking

DSP Builder Advanced Blockset: Advantages

You can:

- Change the design parameters (i.e. number of channels)
- Increase the desired f_{MAX} for the entire datapath
- Target a different silicon architecture, i.e. Stratix IV FPGA to Cyclone III FPGA
- Set the datapath latency
- Trade-off between f_{MAX} and latency

...All By Editing a Top-Level Parameter File in Simulink

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**Video Design
Framework**

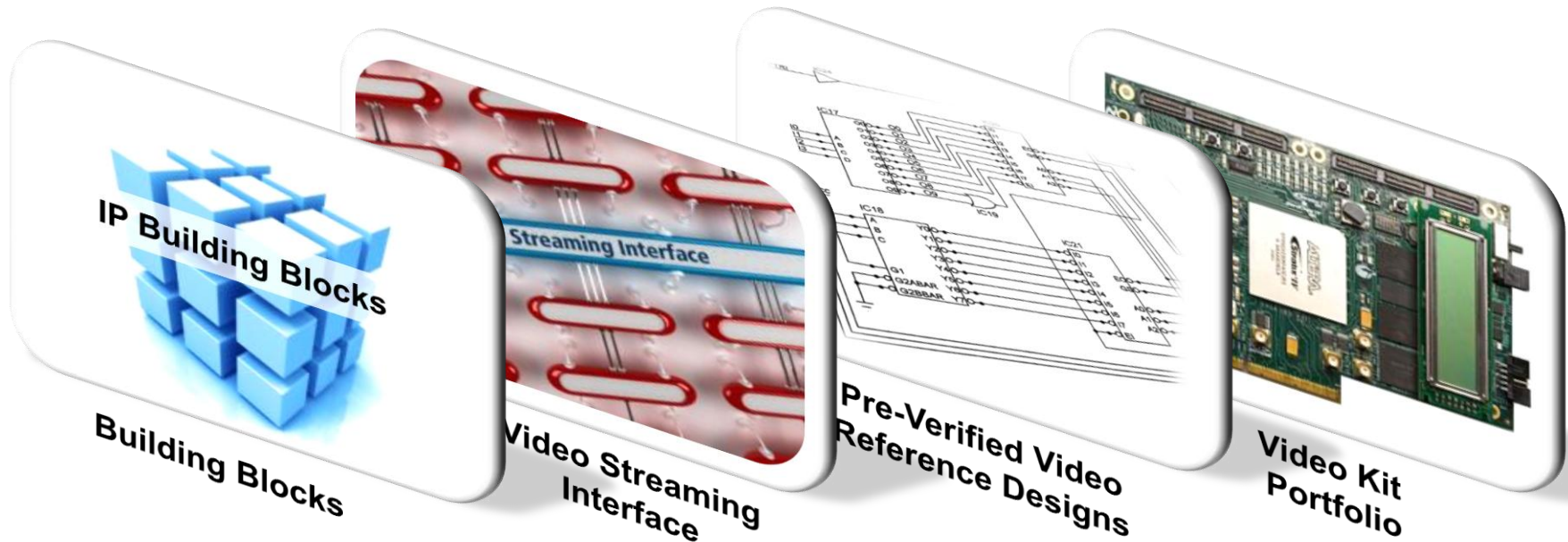
**Comprehensive
Floating-Point IP**

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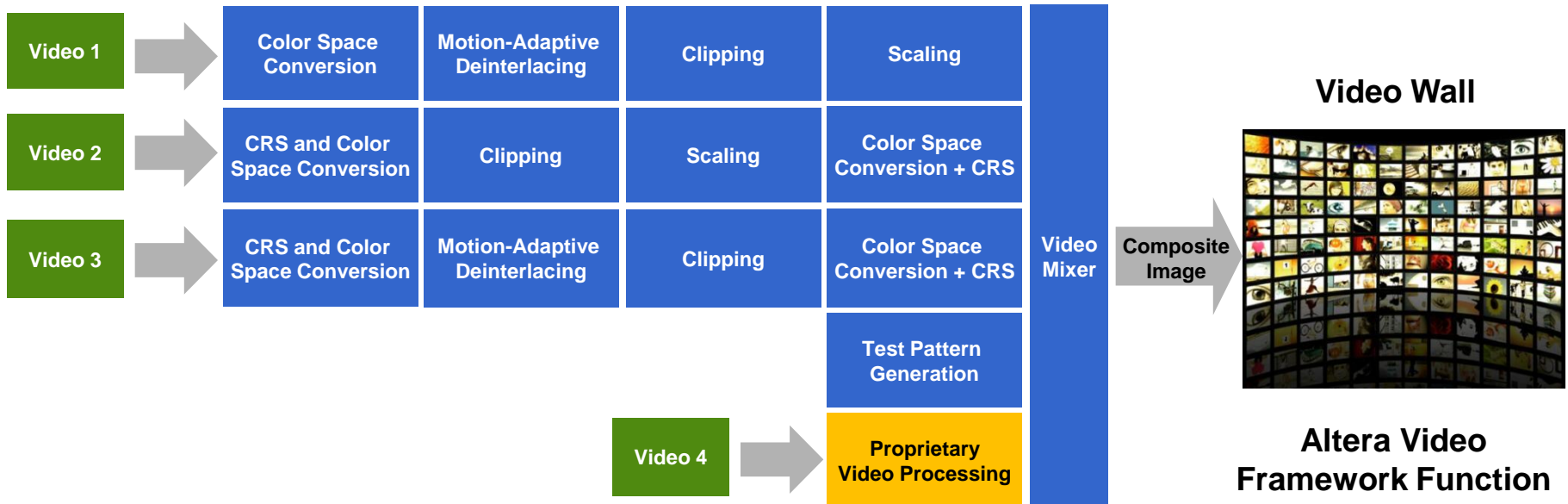
Altera Video Design Framework



Higher Designer Productivity = Faster Time To Market

Altera Video Design Framework

Customer Application



Over 100 Active Customers to Date

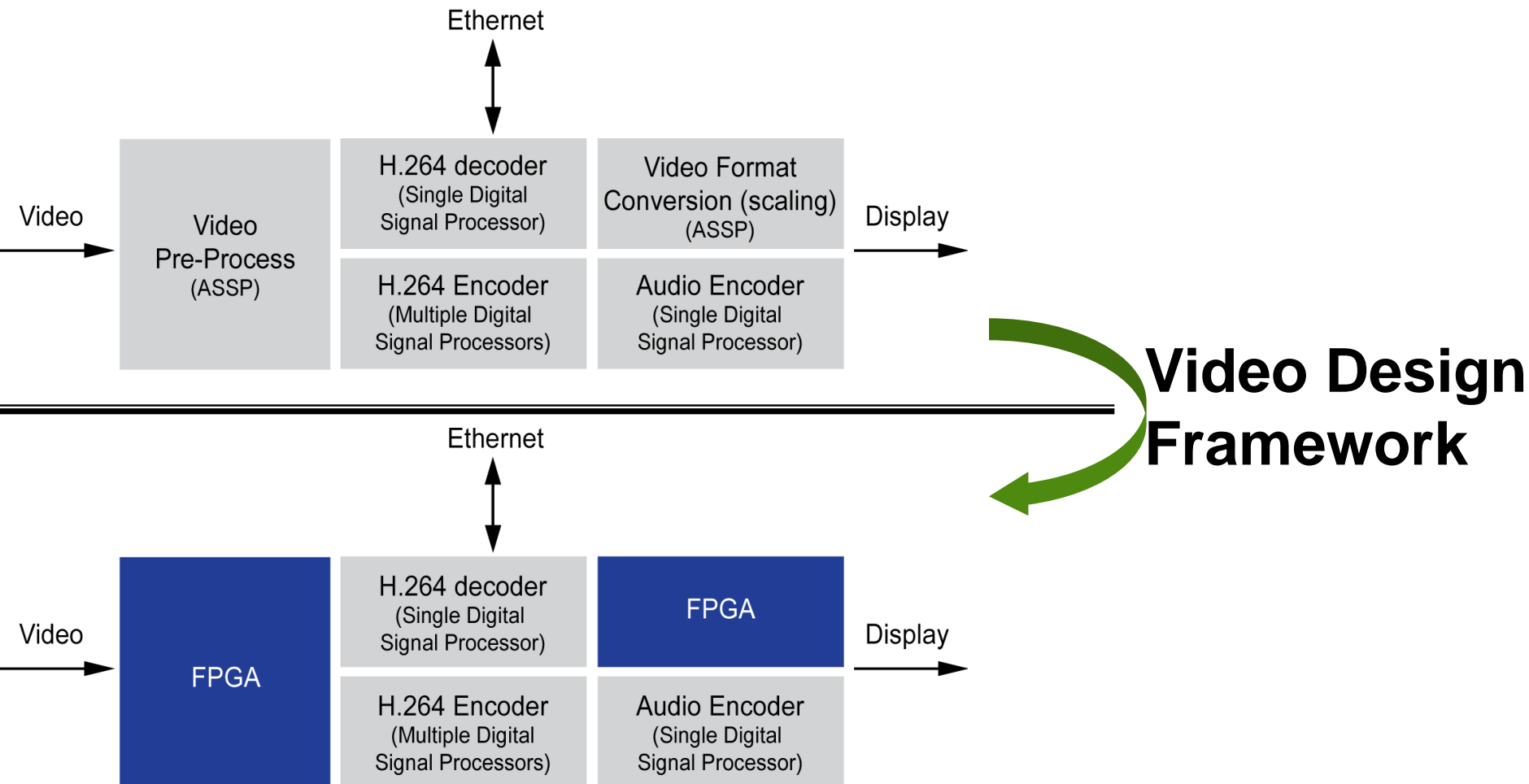
Image: Apantac LLC.

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Altera Video Design Framework

Replace ASSPs in Video Conferencing Systems



Video Design Framework

Competitive Summary

	Xilinx	Altera at 28 nm
Video processing IP portfolio	5	18
Video processing reference design portfolio		6+
Run-time control of the video datapath		✓
Open streaming interface standard for video data		✓
Motion-adaptive deinterlacer		✓
Infrastructure IP: clocked video conversion, crossbar, test pattern generation		✓
Multi-tap scaling engine with programmable taps		✓
Multi-tap scaling engine	✓	✓
Color space converter	✓	✓

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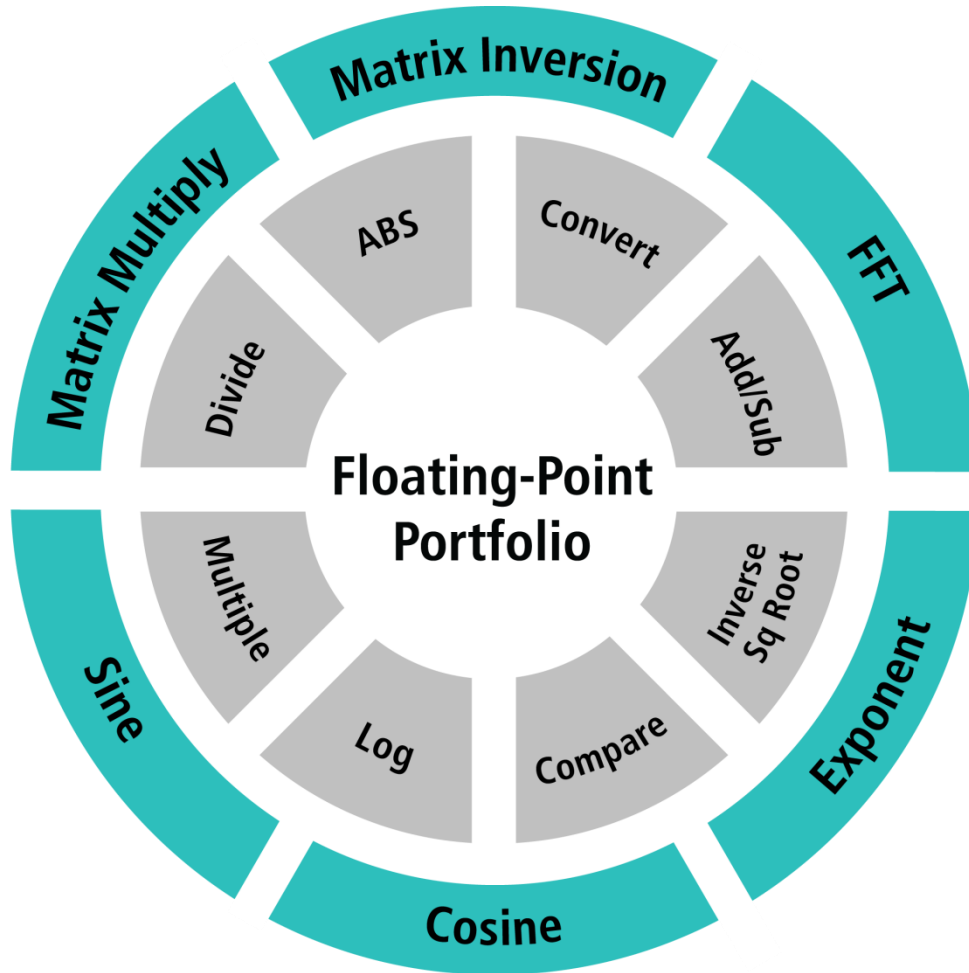
**Video Design
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Altera's Floating-Point Portfolio



Largest Portfolio of Floating-Point Cores

FFT MegaCore offers floating-point option

Sine and cosine: Scheduled for Quartus software v10.1

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Highest Push-Button Performance

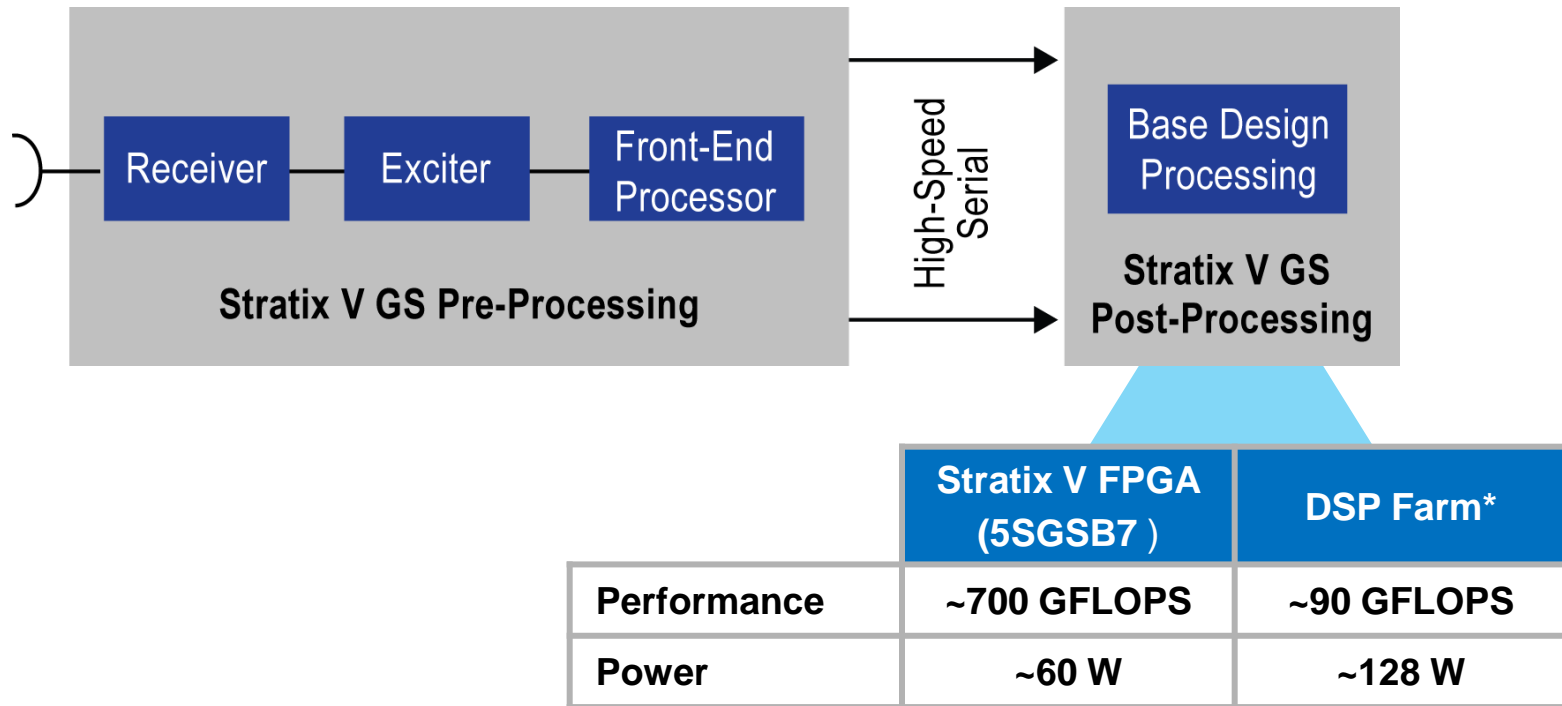
Floating-Point Function	GFLOPs	f_{MAX}	Latency
Matrix multiply – single precision (64x64) x (64x64)	24	380 MHz	8,353 clock cycles
Matrix multiply – double precision (64x64) x (64x64)	18	284 MHz	8,359 clock cycles
Exponent – single precision	-	284 MHz	17 clock cycles
Logarithm – single precision	-	385 MHz	21 clock cycles
Matrix inversion – single precision (64x64) x (64x64)	83	218 MHz	281,505 clock cycles

Benchmarked with Stratix IV FPGA

***Achieve High f_{max} for Large and Complex
Floating-Point Functions***

Altera's Floating-Point Portfolio

Replacing Floating-Point DSP Devices in Radar Systems



Industry's Highest Floating-Point Processing at the Lowest Power

* 32 floating-point DSP devices—2.7 GFLOPS , 4 W each

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Altera Floating-Point Portfolio

Competitive Summary

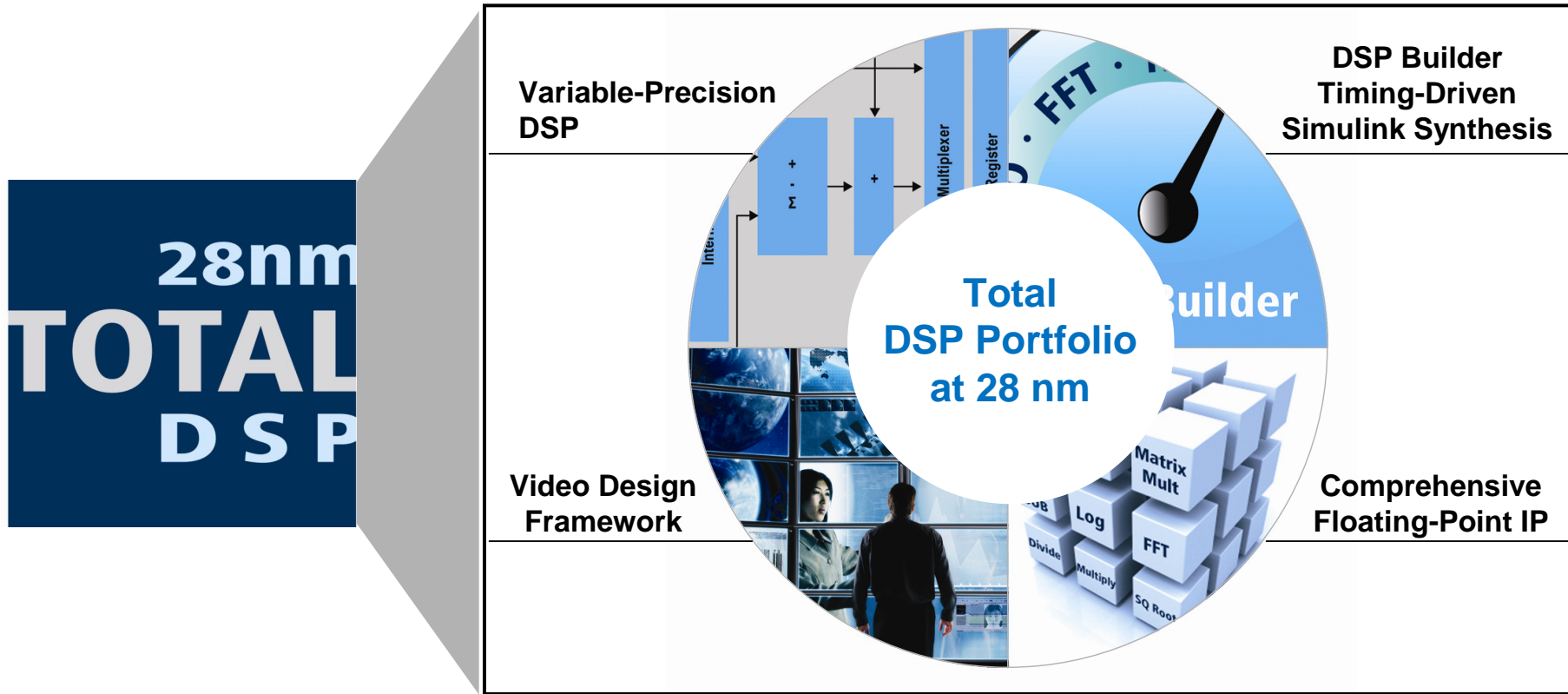
	Xilinx	Altera
Floating-point COSINE	Not Available	✓*
Floating-point SIN	Not Available	✓*
Floating-point matrix INVERSE	Not Available	✓
Floating-point matrix MULT	Not Available	✓
Floating-point ABS	Not Available	✓
Floating-point LOG	Not Available	✓
Floating-point inverse SQRT	Not Available	✓
Floating-point inverse	Not Available	✓
Floating-point exponent	Not Available	✓
Floating-point FFT	Partner IP	✓
Floating-point compare	Partner IP	✓
Floating-point SQRT	Partner IP	✓
Floating-point divider	Partner IP	✓
Floating-point multiplier	Partner IP	✓
Floating-point adder	Partner IP	✓

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Summary



For More Information

- Download our total 28-nm DSP portfolio white paper
 - Accelerating DSP Designs with the Total 28-nm DSP Portfolio
- Download the Stratix V handbook
- Download our DSP architecture whitepaper
 - Enabling High-Precision DSP Applications with the FPGA Industry's First Variable-Precision Architecture
- Download our Stratix V white paper
 - Introducing Innovations at 28nm to Move Beyond Moore's Law