PCI Express Link Equalization Testing

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Application Engineer

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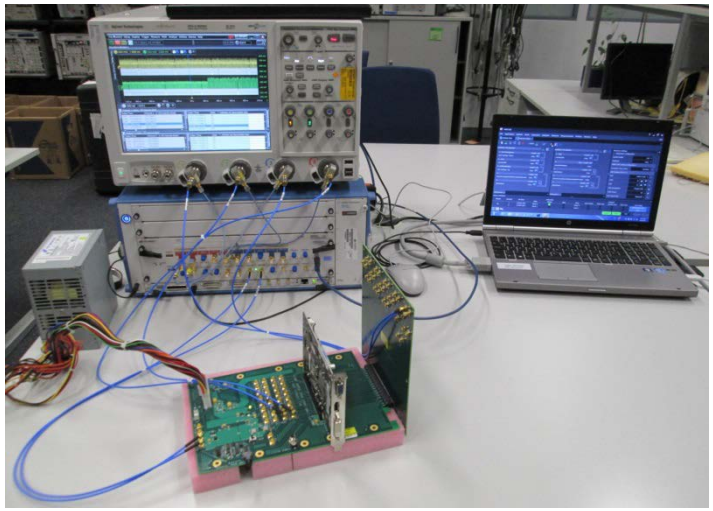

KEYSIGHT TECHNOLOGIES

Agenda

- Introduction
- Dynamic Link Equalization
- TX/RX Link Equalization Tests
- Test Automation
- RX Stress Signal Calibration
- Summary

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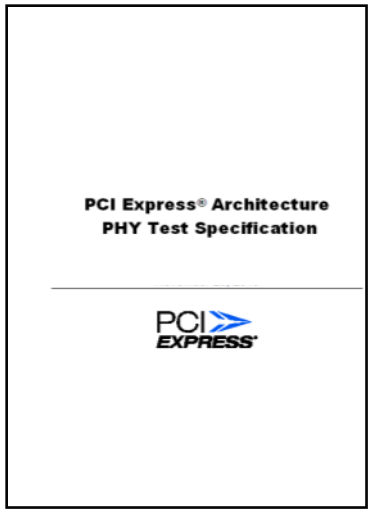
Sequential Development of PCIe Specs and Scope



Base Specification

- Contains all the system knowledge
- Can directly be applied to Chip Test

Card Electromechanical (CEM) Spec

- Applies to Add-In Cards and Mother Boards
- Mitigates card manufacturer's need to study the base specification
- Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)

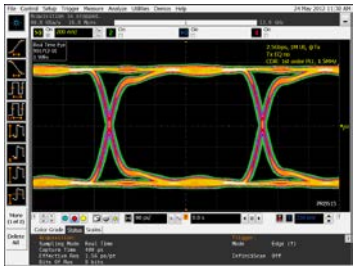
Phy Test Specification

- Defines compliance tests of CEM spec in detail

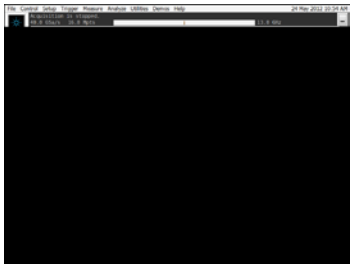
Differences on PHY-layer between PCIe2 and PCIe3

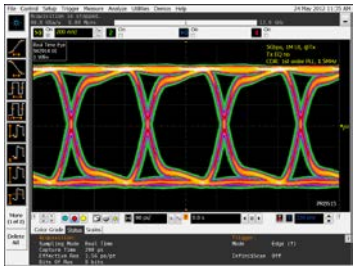
	PCIe2	PCIe3 / PCIe4
transfer rate	5GT/s	8GT/s / 16GT/s
coding	8B/10B	128B/130B
overhead	25%	1.5625%
symbol / block alignment	K28.5 for symbol alignment	EIEOS for block alignment
scrambling	optional with PRBS 2^{16}-1; scrambler reset through K28.5	control: no (partially), data: always PRBS 2^{23}-1; scrambler reset through EIEOS
Adaptable TX link equalization	no	yes
RX-test	**informative**	**normative**

Why Test Receivers

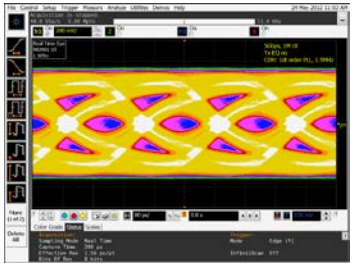


2.5Gbps





5Gbps



8Gbps

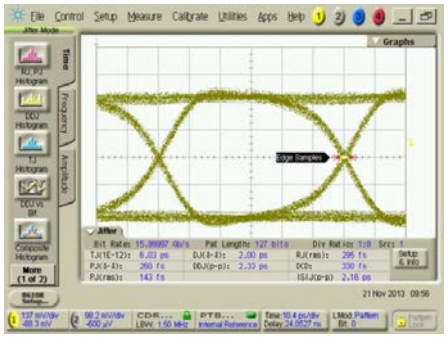
16 Gbps

PCIe 4.0 Outlook and Test Challenges

- New data rate will be added **16GT/s**
  - Requires an output stages capable of providing pre-shoot and de-emphasis with fast enough rise-times.
- **Link Equalization** protocol will be similar
  - TxEQ P0-P10
  - RxEQ CTLE + 2tap DFE
  - Max Channel Length (shorter) – more needs for Re-timers and Re-drivers
  - RX needs to be more sensitive
- RX clocking architectures: CC, DC and IR
  - CC ➔ Common RefClock ➔ synchronous RX and TX
  - IR ➔ Independent RefClock ➔ asynchronous RX and TX
  - SKP OS filtering is required!
- 2.5GT/s ➔ 8GT/s with link equalization, if successful ➔ 16GT/s with link equalization

Integration at 16Gbps

>16Gbps BERT



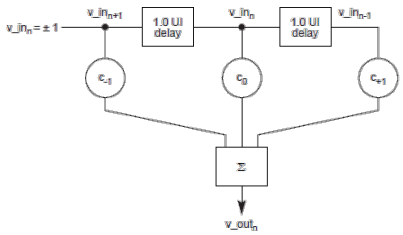
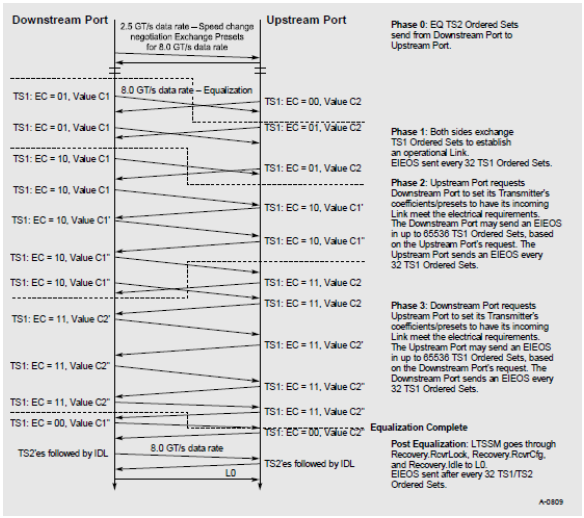


Figure 4-41: Tx Equalization FIR Representation

Link Equalization



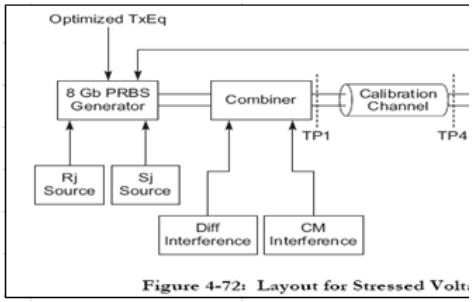
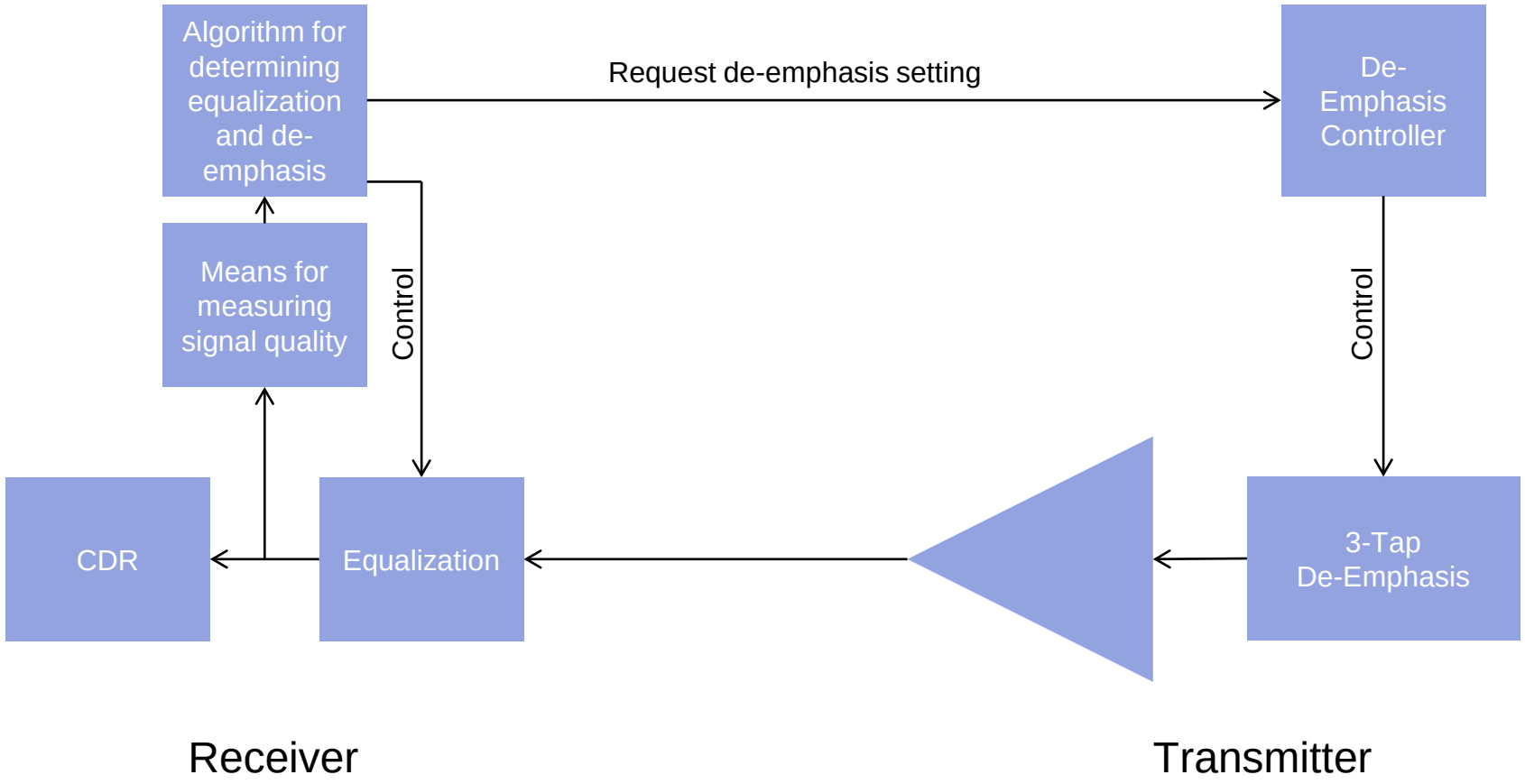


Figure 4-72: Layout for Stressed Volt

Jitter and De-emphasis

Tx/Rx Link for PCIe 3.0

Block Diagram of Transmitter and Receiver Architecture



TxEQ vs RxEQ

RxEQ - CTLE

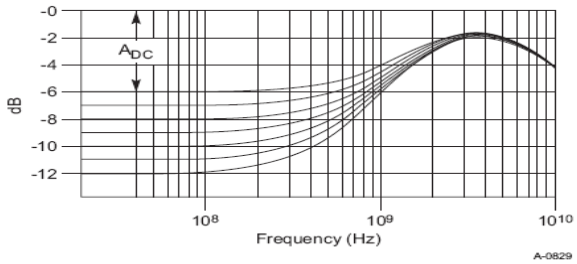
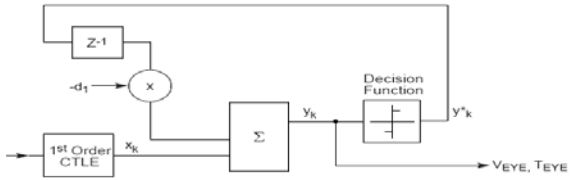


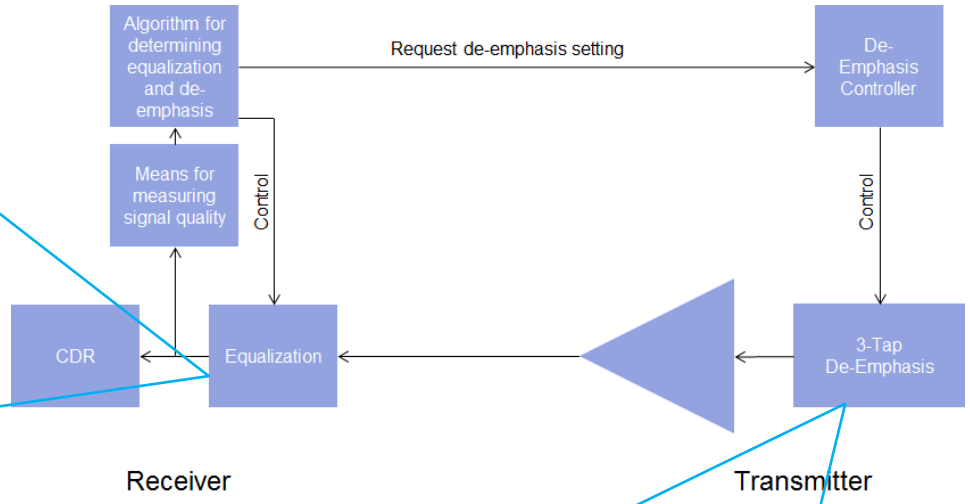
Figure 4-69: Loss Curves for Behavioral CTLE

RxEQ – DFE

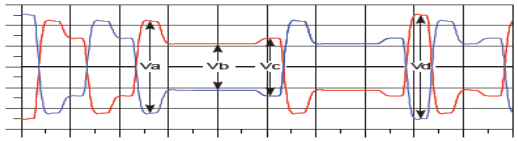


$y_k = x_k - d_1 \mathrm{sgn}(y_{k-1})$
y_k = DFE summer differential output voltage.
y^*_k = decision function output voltage. $|y^*_k| = 1$
x_k = DFE differential input voltage
d_1 = feedback coefficient
k = sample index in UI

Figure 4-70: Equation and Flow Diagram for 1-tap DFE



TxEQ – De-emphasis and Pre-shoot



Preset Number	Preshoot (dB)	De-emphasis (dB)
P4	0.0	0.0
P1	0.0	-3.5 ± 1 dB
P0	0.0	-6.0 ± 1.5 dB
P9	3.5 ± 1 dB	0.0
P8	3.5 ± 1 dB	-3.5 ± 1 dB
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB
P5	1.9 ± 1 dB	0.0
P6	2.5 ± 1 dB	0.0
P3	0.0	-2.5 ± 1 dB
P2	0.0	-4.4 ± 1.5 dB
P10	0.0	See Note 2.

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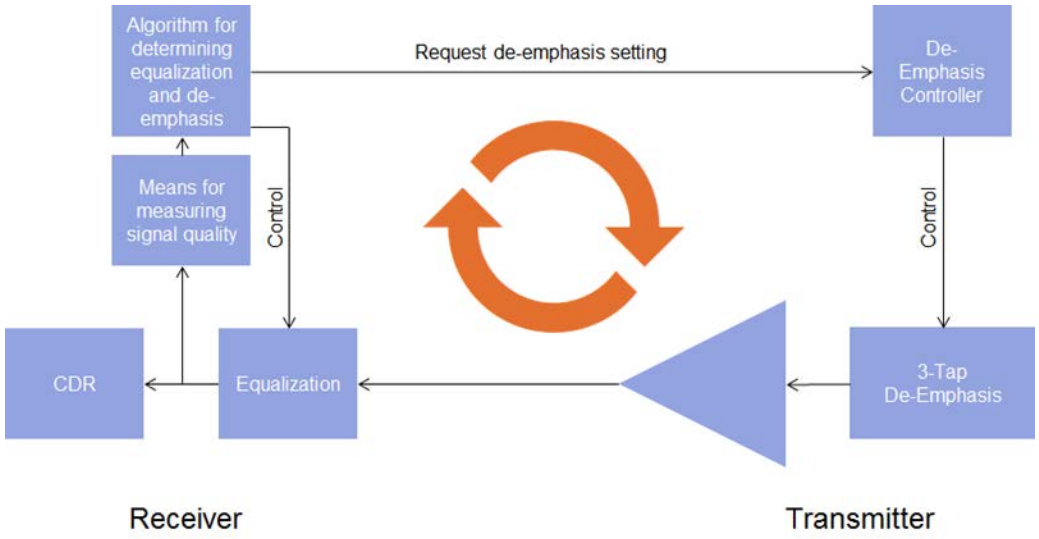
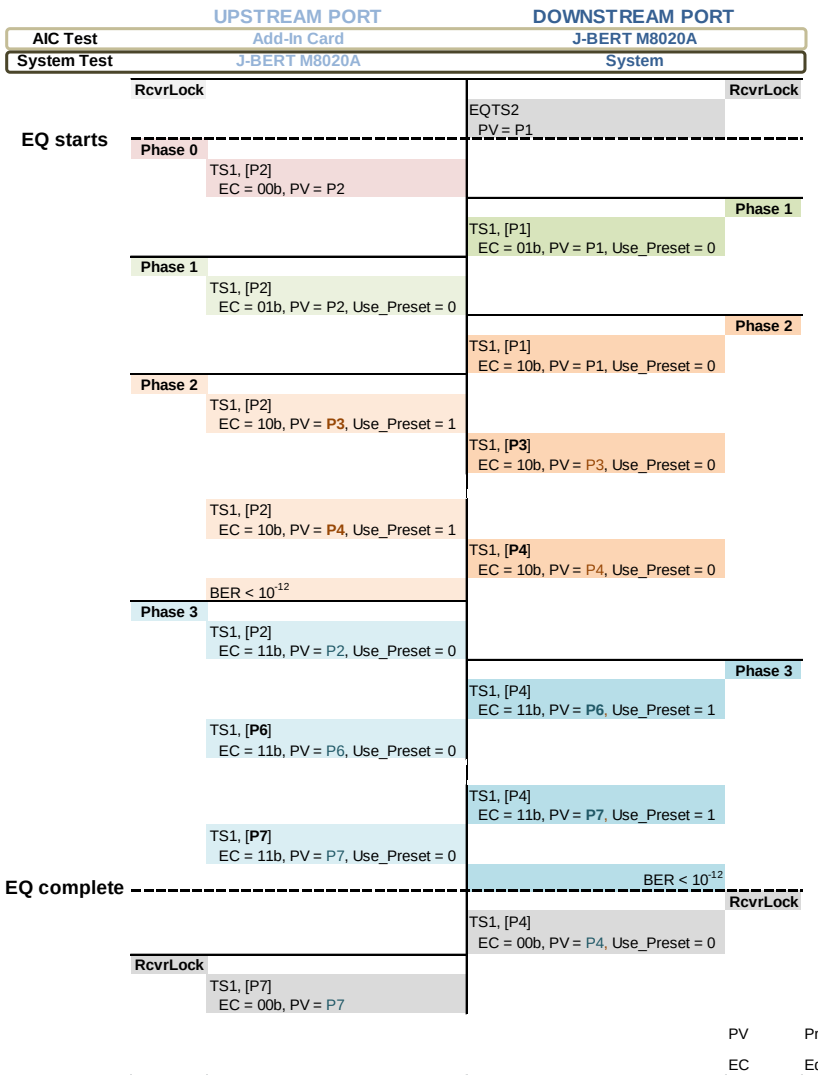
Dynamic Equalization

Root Complex and End Point will negotiate the optimized EQ Setting



Dynamic Link Equalization Handshake

The four phases of the Link Equalization Protocol



Phase 0:
- 2.5Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:
- 8Gb/s
- Link partners settle on 8GT/s speed.
- Exchange FS/LF values.

Phase 2:
- 8Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:
- 8Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

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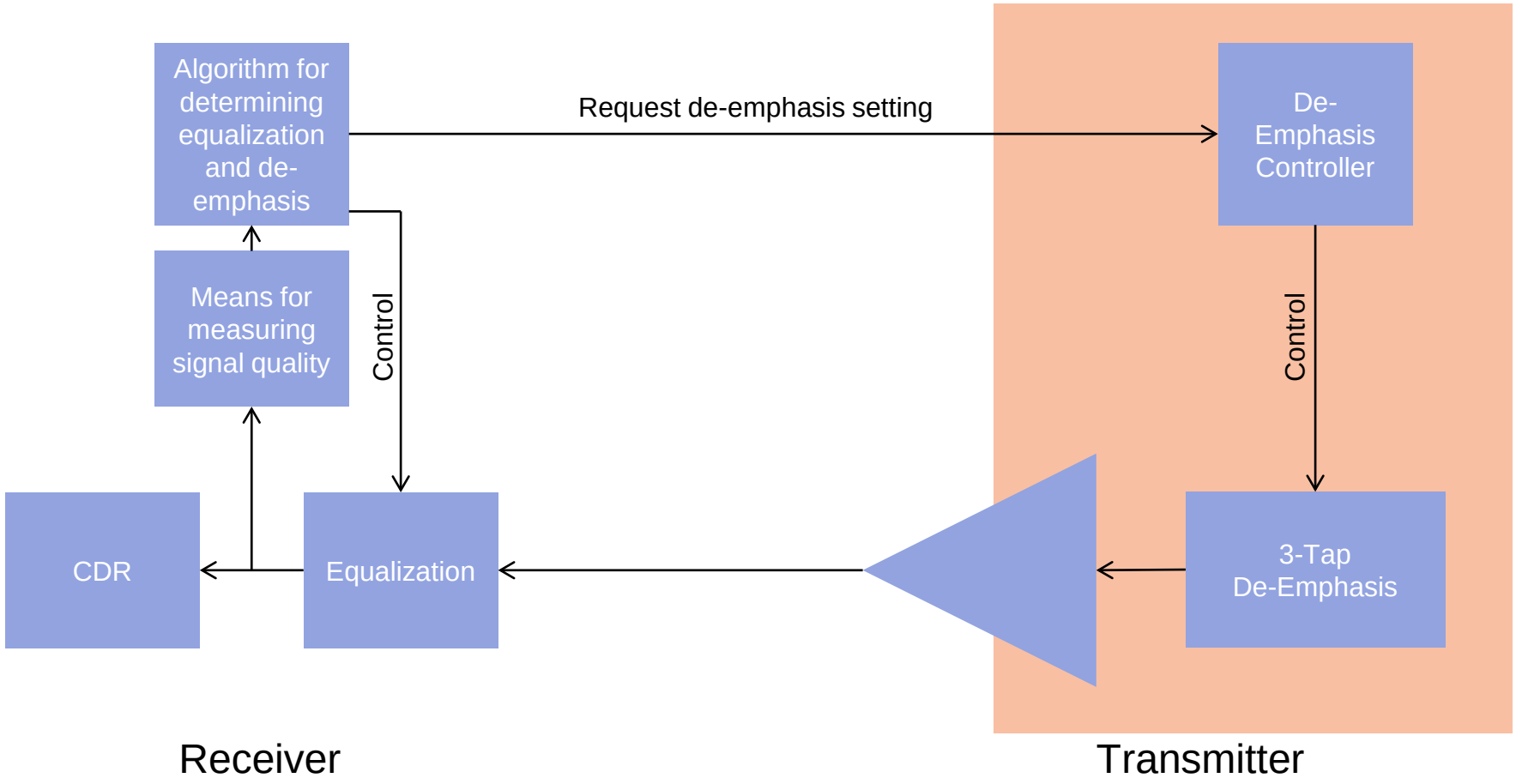
Tx/Rx Link Equalization Testing for PCIe 3.0

According to PCI Express Electrical PHY Test Specification

Test Number	Test Name
2.3	Add-in Card Transmitter Initial Tx EQ Test for 8.0GT/s
2.4	Add-in Card Transmitter Link Equalization Response Test for 8GT/s
2.7	System Board Transmitter Link Equalization Response Test for 8GT/s
2.10	Add-in Card Receiver Link Equalization Test for 8GT/s
2.11	System Board Receiver Link Equalization Test for 8GT/s

Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.3, 2.4, and 2.7 focus on the transmitter

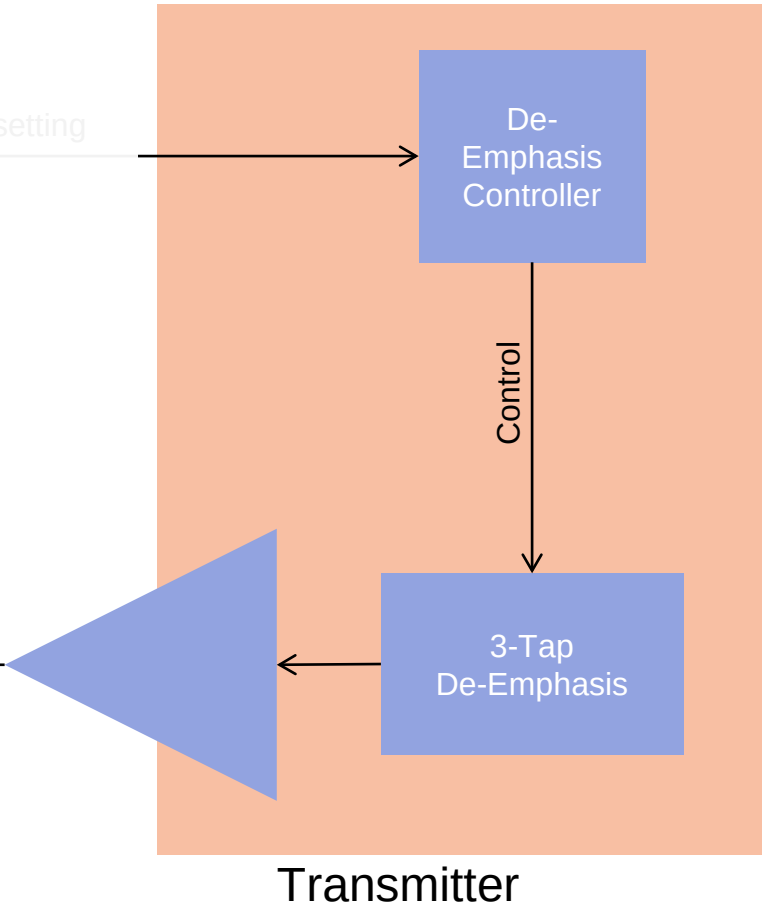


Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.3, 2.4, and 2.7 focus on the transmitter

The PCIe 3.0 Transmitter Link Equalization Tests specified in 2.3 and 2.4 and 2.7 provide insight to TxEQ issues and corner case situations

- Requires the DUT to negotiate using both Presets and Cursors values
- Determines if DUT responds to Preset/Cursor requests in the specified amount of time
- Troubleshoot the issues between protocol communication vs PHY layer performance



Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.3 – Link EQ TX Test for AICs

What does the test do?

This tests checks if the AIC starts 8G transmission with the preset requested by the system in phase 0.

How does the test work?

The test system simulates the downstream port and trains the link up through recovery. Phase 2 and phase 3 of the link equalization are bypassed and thus the AIC is not changing its TX eq. The loopback pattern is the 8G compliance pattern. Once in loopback the waveform of the looped pattern is captured on the scope and analyzed using SIGTEST. The test is repeated for presets 0 through 9.

What are the requirements on the AIC to be able to perform this test?

The AIC must be able to be trained into loopback through recovery. The AIC must accept that phase 2 and phase 3 are bypassed.

Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.3 – Example Test Result Report

KEYSIGHT TECHNOLOGIES

BitifEye Digital Test Solutions

Show all results

Show only selected

Print

- L0_Cal_8GTps_EQ_Cust_Preset
- L0_Cal_8GTps_RJ
- L0_Cal_8GTps_SJ
- L0_Cal_8GTps_CBB3_DM_SI
- L0_Cal_8GTps_CBB3_Eye_Height
- L0_Cal_8GTps_CBB3_Eye_Width
- L0_Cal_8GTps_CBB3_Comp_Eye
- L0_Rx_8GTps_CBB3_DeEmph_Scan
- L0_Rx_8GTps_CBB3_PreSh_Scan
- L0_Rx_8GTps_CBB3_PreComp_2.8
- L0_Rx_8GTps_CBB3_Comp_2.8
- L0_EqRx_8GTps_CBB3_Com_2.10
- L0_Tx_8GTps_EQ_2_3
- L0_Tx_8GTps_EQ_Comp_2_4

L0_Tx_8GTps_EQ_2_3

for PCI Express 3.0 Add-In Card

Offline	False
Data Rate Deviation	0 ppm
Generator Start Preset	P7
Link EQ Tx Test Script File	C:\Documents and Settings\All Users\Application Data\Bitifeye\Valiframe\Settings\PCIExpress3\Pcie3_8G_M8020A_EqTx_Loopback.txt
Suppress Loopback Training Messages	False
Use CDR	True
CDR Loop Bandwidth	12 MHz
Peaking	1 dB
Analyzer Equalization	6dB
Capture and Compare Mode	False
EQ Preset Measurement	SigTest
Scope Sampling Rate	40 GSa/s
Use Power Switch Automation	True
Power Switch Channel Number	2
Power Cycle Off On Duration	7 s
Power Cycle Settling Time	8 s
Power Cycle max. Retries for LB Training	3

Result	DUT Initial Preset	Pre-Shoot [dB]	Min Spec PS [dB]	Max Spec PS [dB]	De-Emphasis [dB]	Min Spec DE [dB]	Max Spec DE [dB]	Comment
pass	P0	0.00	0.00	0.00	-6.03	-7.50	-4.50	
pass	P1	0.00	0.00	0.00	-3.53	-4.50	-2.50	
pass	P2	0.00	0.00	0.00	-4.45	-5.90	-2.90	
pass	P3	0.00	0.00	0.00	-2.70	-3.50	-1.50	
pass	P4	0.00	0.00	0.00	0.00	0.00	0.00	
pass	P5	1.92	0.90	2.90	0.00	0.00	0.00	
pass	P6	2.68	1.50	3.50	0.00	0.00	0.00	
pass	P7	3.49	2.50	4.50	-6.02	-7.50	-4.50	
pass	P8	3.90	2.50	4.50	-3.92	-4.50	-2.50	
pass	P9	3.50	2.50	4.50	0.00	0.00	0.00	

Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.4 – Link EQ TX Test for AICs

What does the test do?

This tests checks if the AIC is reacting to preset and cursor requests of the system in phase 3. Next to the waveform, protocol as well as electrical response times are checked to be within 1µs.

How does the test work?

The test system simulates the downstream port and trains the link up through recovery. Phase 2 and phase 3 of the link equalization are performed. The AIC TX signal as well as the test system TX signal are captured for phase 3. The captured data is analyzed and decoded to find the initial TX eq change request of the test system as well as to find the acknowledgement of the AIC and physical waveform change. Once in loopback the waveform of the looped pattern is captured on the scope and analyzed using SIGTEST. The test is repeated for presets 0 through 9 as well as for the cursors reported by the AIC for each preset.

What are the requirements on the AIC to be able to perform this test?

The AIC must be able to be trained into loopback through recovery. The AIC must be able to perform phase 2 and phase 3 and be able to react on cursor requests.

Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.4 / 2.7 – Relevant Symbols of TS1

Symbol 6:

- Bit 0 – 1: EC – current phase
- Bit 2: reserved
- Bit 3 – 6: Transmitter Preset
- Bit 7: Use_Preset

Symbol 7:

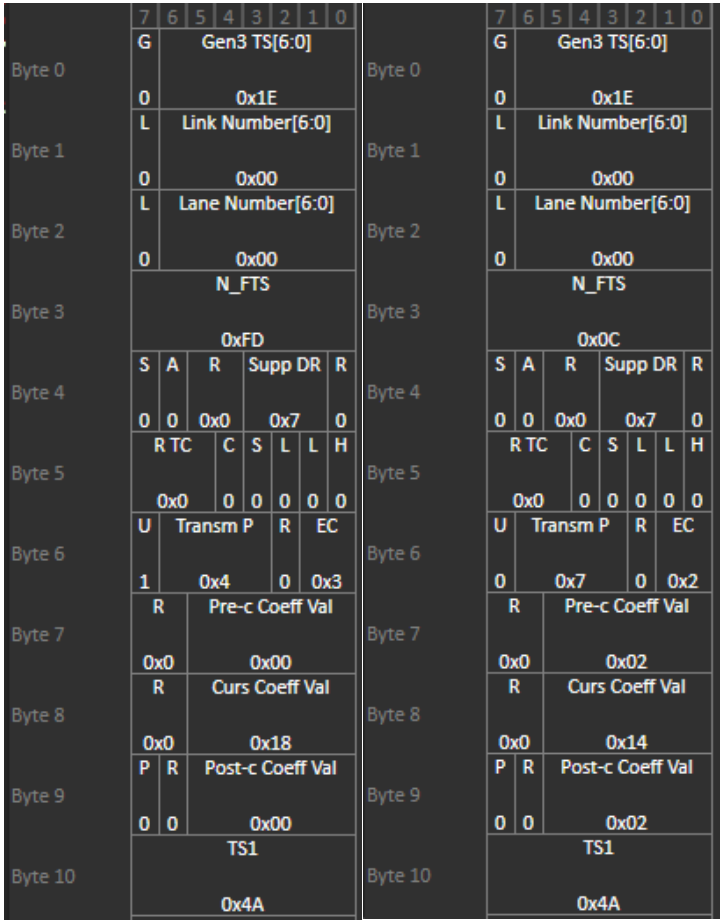
- Bit 0 – 5: Pre-cursor coefficient
- Bit 6 – 7: reserved

Symbol 8:

- Bit 0 – 5: Main cursor coefficient
- Bit 6 – 7: reserved

Symbol 9:

- Bit 0 – 5: Post-cursor coefficient
- Bit 6 – 7: reserved



Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.4 / 2.7 – EQ Change Request & Acknowledgement

How to identify the first EQ change request for the timing measurement?

The J-BERT M8070A TX signal is checked for EC bits indicating the phase change and the Use_Preset bits are checked for a change from 0 to 1

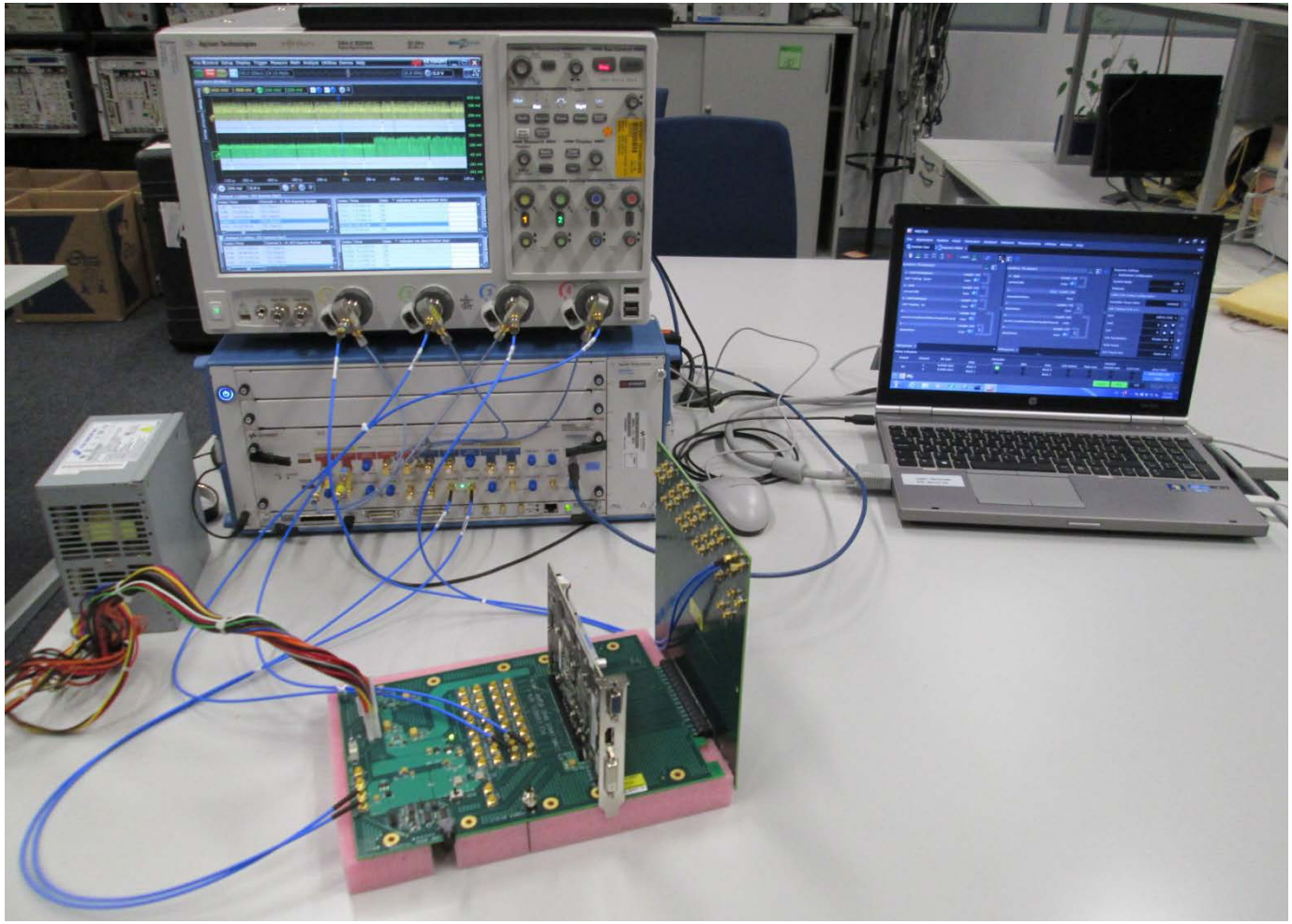
- Test 2.7: EC changes from 01b to 10b and Use_Preset from 0b to 1b
- Test 2.4: EC changes from 10b to 11b and Use_Preset from 0b to 1b

How to identify the protocol acknowledgement for the EQ request?

The DUT TX signal is checked for a change in the preset value in the respective phase. E.g. initial preset P7 to requested preset of P4.

Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.3 and 2.4 – Test Setup



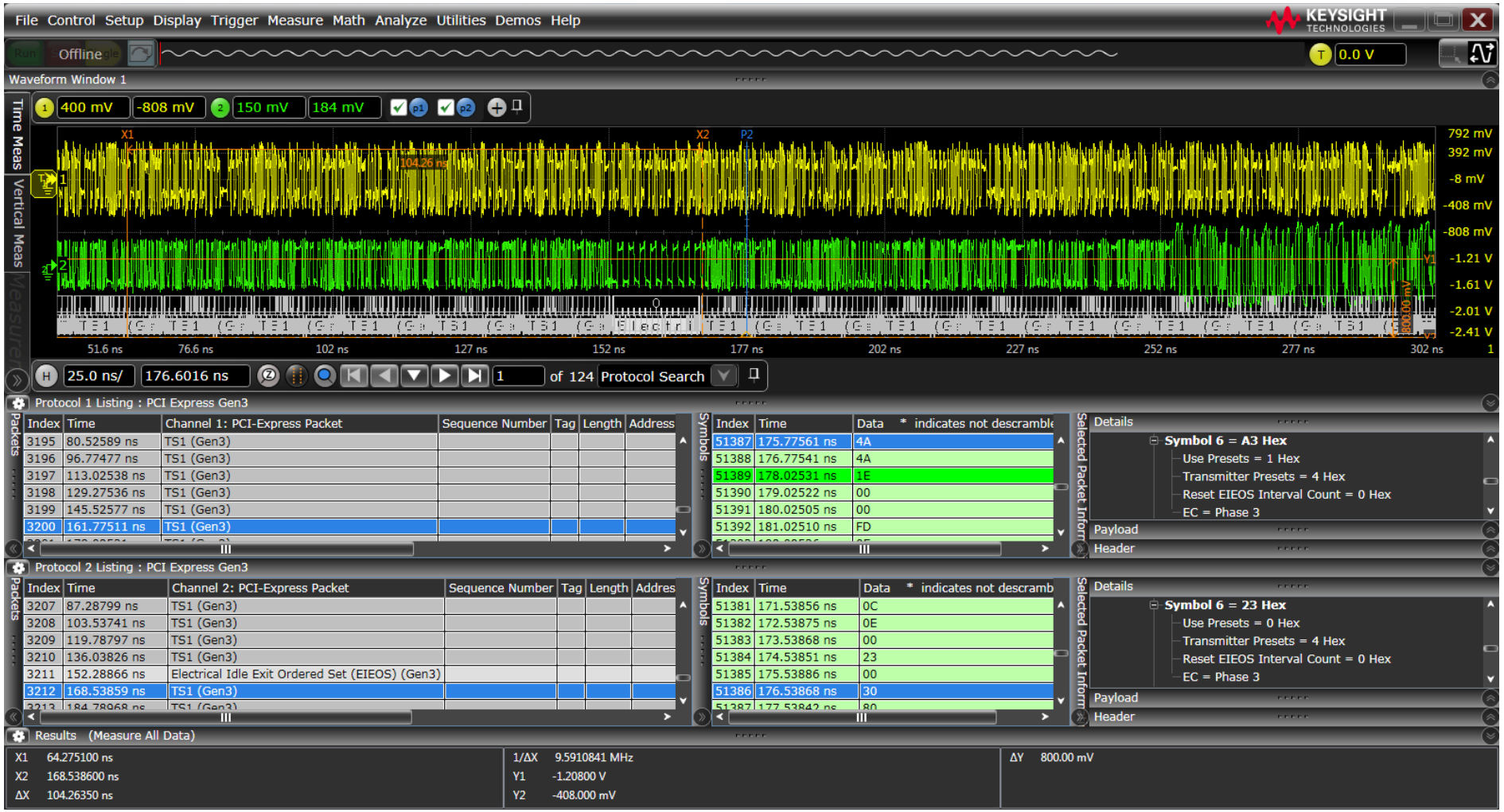
J-BERT M8020A is used to train the device and issue a trigger to the scope allowing to capture phase 3

J-BERT TX signal as well as DUT TX signals are split and captured by the scope

The common timing reference allows for timing measurements on the captured and decoded waveforms

Tx/Rx Link Equalization Testing for PCIe 3.0

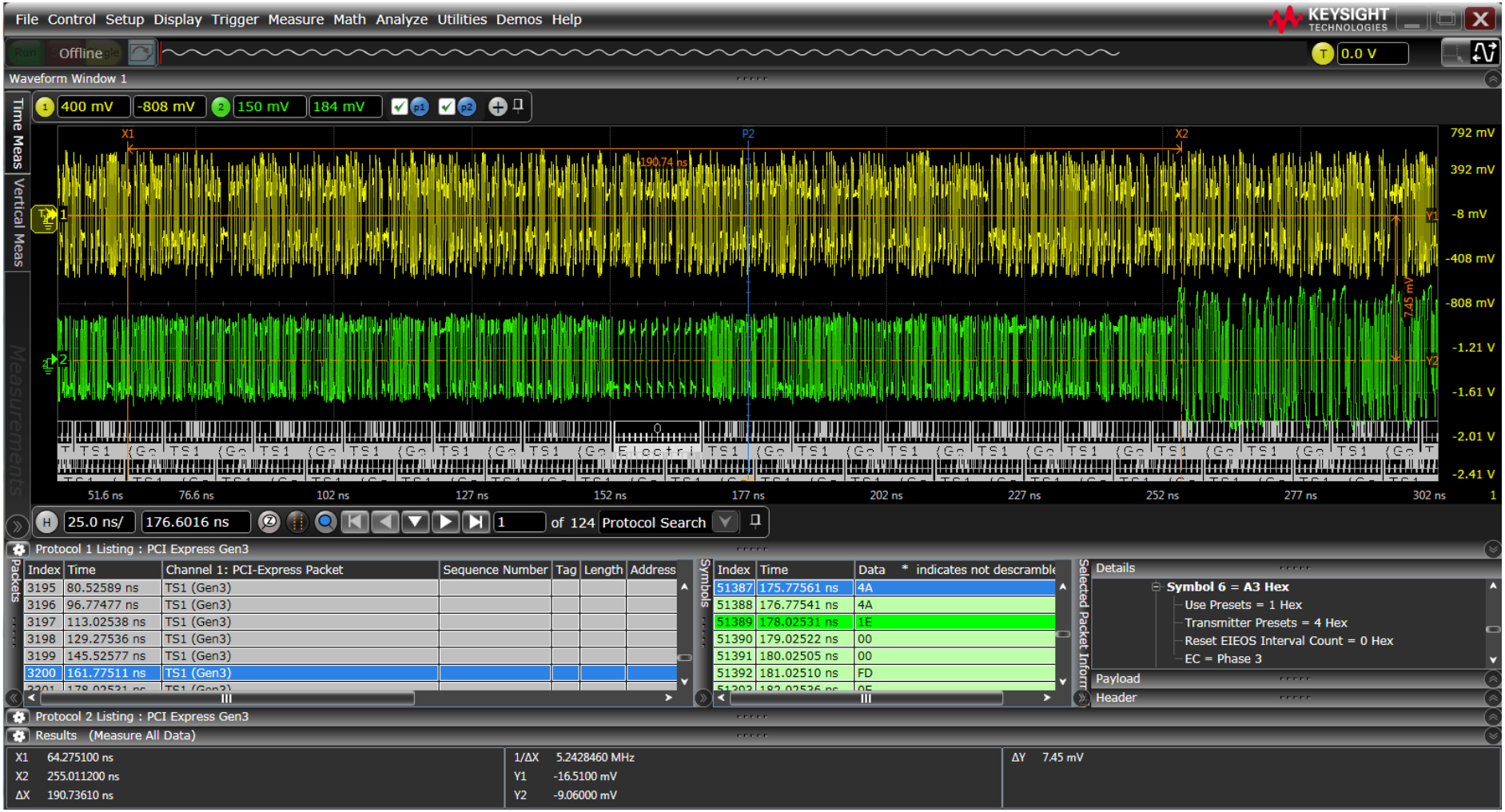
Tests 2.4 – Protocol Response Time



First TS1 with change request to first TS1 with acknowledgement ➔ 104ns

Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.4 – Electrical Response Time



First TS1 with change request to physical waveform change ➔ 191ns

Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.4 – Example Test Result Report

KEYSIGHT TECHNOLOGIES

BitifEye Digital Test Solutions

Show all results
Show only selected

Print

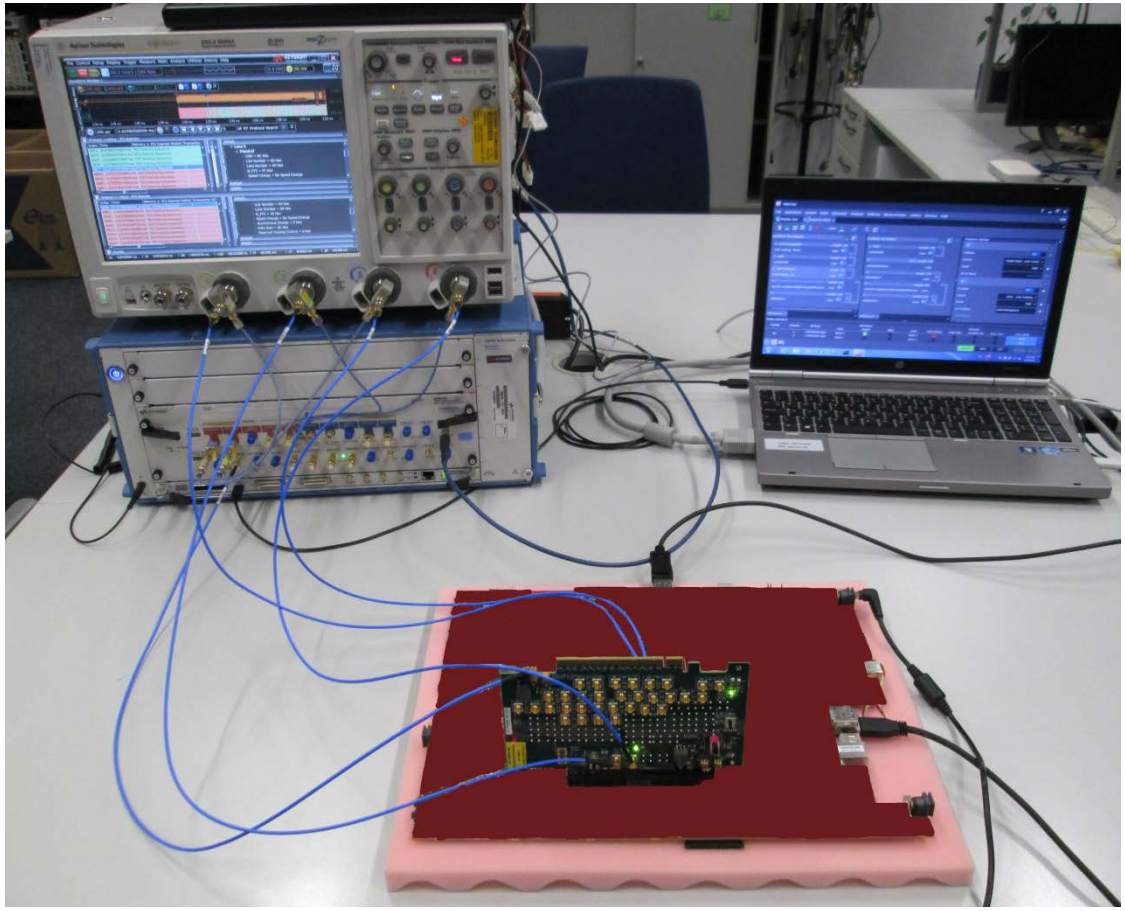
- L0_Cal_8GTps_EQ_Cust_Preset
- L0_Cal_8GTps_RJ
- L0_Cal_8GTps_SJ
- L0_Cal_8GTps_CBB3_DM_SI
- L0_Cal_8GTps_CBB3_Eye_Height
- L0_Cal_8GTps_CBB3_Eye_Width
- L0_Cal_8GTps_CBB3_Comp_Eye
- L0_Rx_8GTps_CBB3_DeEmph_Scan
- L0_Rx_8GTps_CBB3_PreSh_Scan
- L0_Rx_8GTps_CBB3_PreComp_2.8
- L0_Rx_8GTps_CBB3_Comp_2.8
- L0_EqRx_8GTps_CBB3_Com_2.10
- L0_Tx_8GTps_EQ_2_3
- L0_Tx_8GTps_EQ_Comp_2_4

Use Power Switch Automation	True
Power Switch Channel Number	2
Power Cycle Off On Duration	7 s
Power Cycle Settling Time	8 s
Power Cycle max. Retries for LB Training	3

Result	DUT Target Preset	Electrical response time [ns]	Protocol response time [ns]	Pre-Shoot [dB]	Min Spec PS [dB]	Max Spec PS [dB]	De-Emphasis [dB]	Min Spec DE [dB]	Max Spec DE [dB]	Comment
pass	P0	129.87	125.25	0.00	0.00	0.00	-6.03	-7.50	-4.50	DUT reported cursors: (0,45,15)
pass	P1	125.12	136.12	0.00	0.00	0.00	-3.54	-4.50	-2.50	DUT reported cursors: (0,50,10)
pass	P2	126.25	125.87	0.00	0.00	0.00	-4.45	-5.90	-2.90	DUT reported cursors: (0,48,12)
pass	P3	131.87	124.62	0.00	0.00	0.00	-2.71	-3.50	-1.50	DUT reported cursors: (0,52,8)
pass	P4	132.25	121.62	0.00	0.00	0.00	0.00	0.00	0.00	DUT reported cursors: (0,60,0)
pass	P5	126.37	130.37	1.93	0.90	2.90	0.00	0.00	0.00	DUT reported cursors: (6,54,0)
pass	P6	128.50	132.00	2.69	1.50	3.50	0.00	0.00	0.00	DUT reported cursors: (8,52,0)
pass	P7	134.50	132.37	3.51	2.50	4.50	-6.03	-7.50	-4.50	DUT reported cursors: (6,42,12)
pass	P8	131.12	121.62	3.91	2.50	4.50	-3.92	-4.50	-2.50	DUT reported cursors: (8,44,8)
pass	P9	130.75	128.12	3.50	2.50	4.50	0.00	0.00	0.00	DUT reported cursors: (10,50,0)
pass	P0' (0,45,15)	127.12	128.25	0.00	0.00	0.00	-6.03	-7.50	-4.50	
pass	P1' (0,50,10)	127.12	127.75	0.00	0.00	0.00	-3.54	-4.50	-2.50	
pass	P2' (0,48,12)	126.00	124.12	0.00	0.00	0.00	-4.46	-5.90	-2.90	
pass	P3' (0,52,8)	142.12	120.12	0.00	0.00	0.00	-2.70	-3.50	-1.50	
pass	P4' (0,60,0)	127.00	126.87	0.00	0.00	0.00	0.00	0.00	0.00	
pass	P5' (6,54,0)	130.50	121.37	1.93	0.90	2.90	0.00	0.00	0.00	
pass	P6' (8,52,0)	127.25	121.37	2.68	1.50	3.50	0.00	0.00	0.00	
pass	P7' (6,42,12)	125.37	128.12	3.50	2.50	4.50	-6.03	-7.50	-4.50	
pass	P8' (8,44,8)	123.75	123.37	3.91	2.50	4.50	-3.93	-4.50	-2.50	
pass	P9' (10,50,0)	133.75	119.87	3.52	2.50	4.50	0.00	0.00	0.00	

Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.7 – Test Setup



J-BERT M8020A is used to train the device and issue a trigger to the scope allowing to capture phase 2

J-BERT TX signal as well as DUT TX signals are split and captured by the scope

J-BERT M8020A is synchronized to the system by the system's 100MHz clock

It is not necessary to turn off SSC on the system side

Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.7 – Link EQ TX Test for Systems

What does the test do?

This tests checks if the system is reacting to preset and cursor requests of the system in phase 2. Next to the waveform, protocol as well as electrical response times are checked to be within 1µs.

How does the test work?

The test system simulates the upstream port and trains the link up through recovery. Phase 2 and phase 3 of the link equalization are performed. The system TX signal as well as the test system TX signal are captured for phase 2. The captured data is analyzed and decoded to find the initial TX eq change request of the test system as well as to find the acknowledgement of the system and physical waveform change. Once in loopback the waveform of the looped pattern is captured on the scope and analyzed using SIGTEST. The test is repeated for presets 0 through 9 as well as for the cursors reported by the AIC for each preset.

What are the requirements on the system to be able to perform this test?

The system must be able to be trained into loopback through recovery. The system must be able to perform phase 2 and phase 3 and be able to react on cursor requests. It must be possible to change the initial preset of the system to P4 and P7 (usually a BIOS entry) to be able to measure response times for all presets reliably.

Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.7 – Example Test Result Report

KEYSIGHT TECHNOLOGIES

BitifEye Digital Test Solutions

Show all results
Show only selected

Print

- L0_Cal_8GTps_DeEmphasis
- L0_Cal_8GTps_EQ_Preset
- L0_Cal_8GTps_EQ_Cust_Preset
- L0_Cal_8GTps_RJ
- L0_Cal_8GTps_SJ
- L0_Cal_8GTps_CBB3_DM_SI
- L0_Cal_8GTps_CLB3_Eye_Height
- L0_Cal_8GTps_CLB3_Eye_Width
- L0_Cal_8GTps_CLB3_Comp_Eye
- L0_Rx_8GTps_CLB3_DeEmph_Scan
- L0_Rx_8GTps_CLB3_PreSh_Scan
- L0_Rx_8GTps_CLB3_Comp_2.9
- L0_EqRx_8GTps_CLB3_Com_2.11
- L0_Tx_8GTps_EQ_Comp_2_7

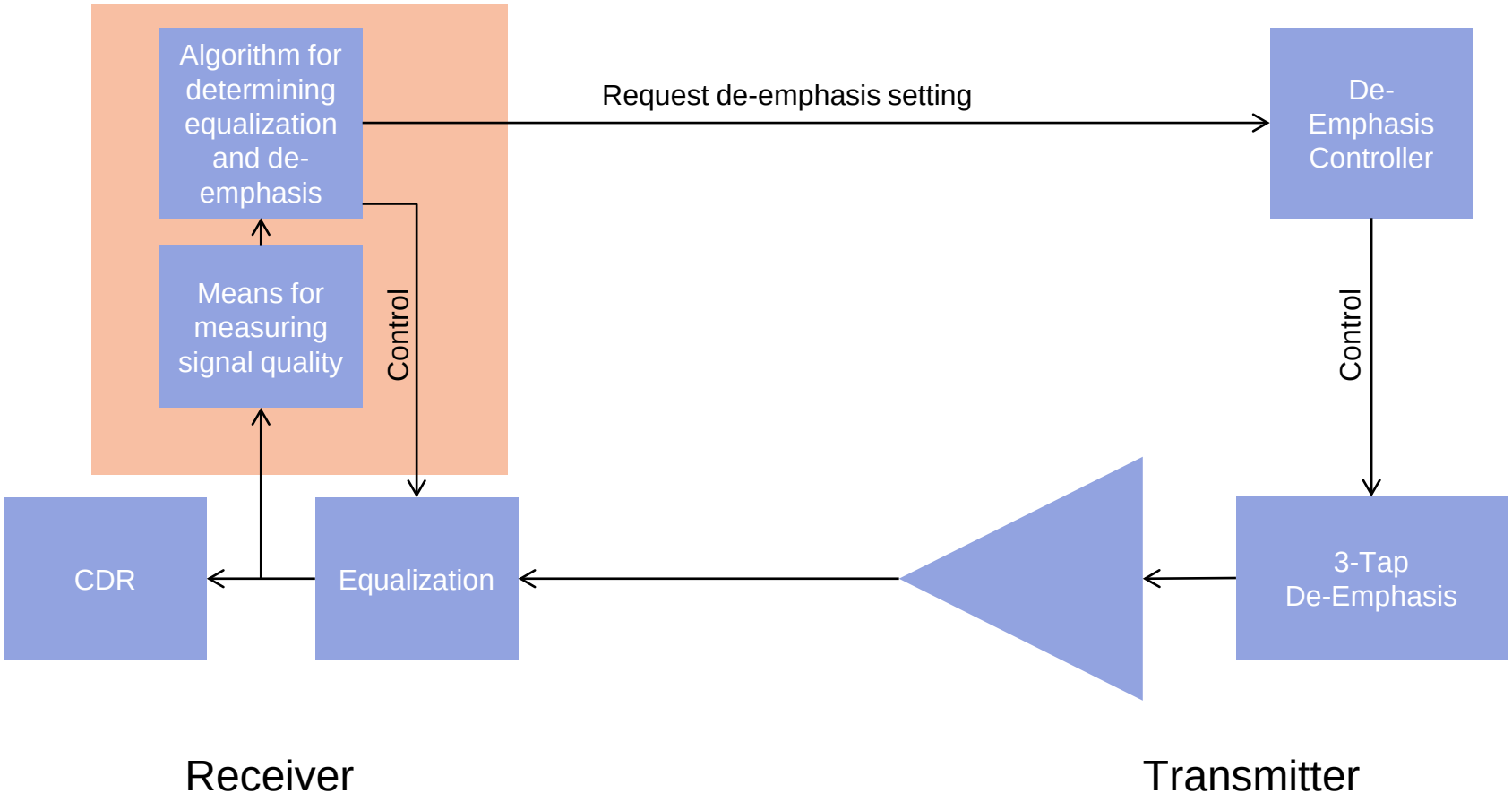
Result	DUT Target Preset	Electrical response time [ns]	Protocol response time [ns]	Pre-Shoot [dB]	Min Spec PS [dB]	Max Spec PS [dB]	De-Emphasis [dB]	Min Spec DE [dB]	Max Spec DE [dB]	Comment
*** FAIL ***	P0	n/a	404.50	0.00	0.00	0.00	-6.32	-7.50	-4.50	DUT reported cursors: (0,24,8) Could not find a preset change on the waveform 1
pass	P1	177.66	417.12	0.00	0.00	0.00	-3.29	-4.50	-2.50	DUT reported cursors: (0,27,5)
pass	P2	167.29	432.50	0.00	0.00	0.00	-4.12	-5.90	-2.90	DUT reported cursors: (0,26,6)
pass	P3	183.41	395.25	0.00	0.00	0.00	-2.39	-3.50	-1.50	DUT reported cursors: (0,28,4)
pass	P4	208.41	411.37	0.00	0.00	0.00	0.00	0.00	0.00	DUT reported cursors: (0,32,0)
pass	P5	183.79	426.12	1.74	0.90	2.90	0.00	0.00	0.00	DUT reported cursors: (3,29,0)
pass	P6	180.28	399.50	2.37	1.50	3.50	0.00	0.00	0.00	DUT reported cursors: (4,28,0)
*** FAIL ***	P7	n/a	n/a	3.28	2.50	4.50	-5.66	-7.50	-4.50	DUT reported cursors: (3,23,6) Found response before request Could not find a preset change on the waveform 1, 2
pass	P8	196.41	429.50	3.93	2.50	4.50	-3.95	-4.50	-2.50	DUT reported cursors: (4,24,4)
pass	P9	191.03	425.62	3.30	2.50	4.50	0.00	0.00	0.00	DUT reported cursors: (5,27,0)
pass	P0' (0,24,8)	169.54	435.87	0.00	0.00	0.00	-6.33	-7.50	-4.50	
pass	P1' (0,27,5)	186.04	422.62	0.00	0.00	0.00	-3.27	-4.50	-2.50	
pass	P2' (0,26,6)	182.41	425.75	0.00	0.00	0.00	-4.12	-5.90	-2.90	
pass	P3' (0,28,4)	183.16	444.00	0.00	0.00	0.00	-2.34	-3.50	-1.50	
pass	P4' (0,32,0)	182.29	440.50	0.00	0.00	0.00	0.00	0.00	0.00	
pass	P5' (3,29,0)	182.54	406.87	1.72	0.90	2.90	0.00	0.00	0.00	
pass	P6' (4,28,0)	184.28	437.12	2.36	1.50	3.50	0.00	0.00	0.00	
*** FAIL ***	P7' (3,23,6)	n/a	n/a	3.28	2.50	4.50	-5.67	-7.50	-4.50	Found response before request Could not find a preset change on the waveform 1, 2
pass	P8' (4,24,4)	199.41	409.12	3.97	2.50	4.50	-3.95	-4.50	-2.50	
pass	P9' (5,27,0)	167.78	399.25	3.28	2.50	4.50	0.00	0.00	0.00	

1. Initial preset could not be changed from P7 to a different value ➔ P0 and P7 electrical response times could not be measured.
2. It is not possible to find an acknowledgment for a P7 change request when the system is at P7 already

KEYSIGHT TECHNOLOGIES

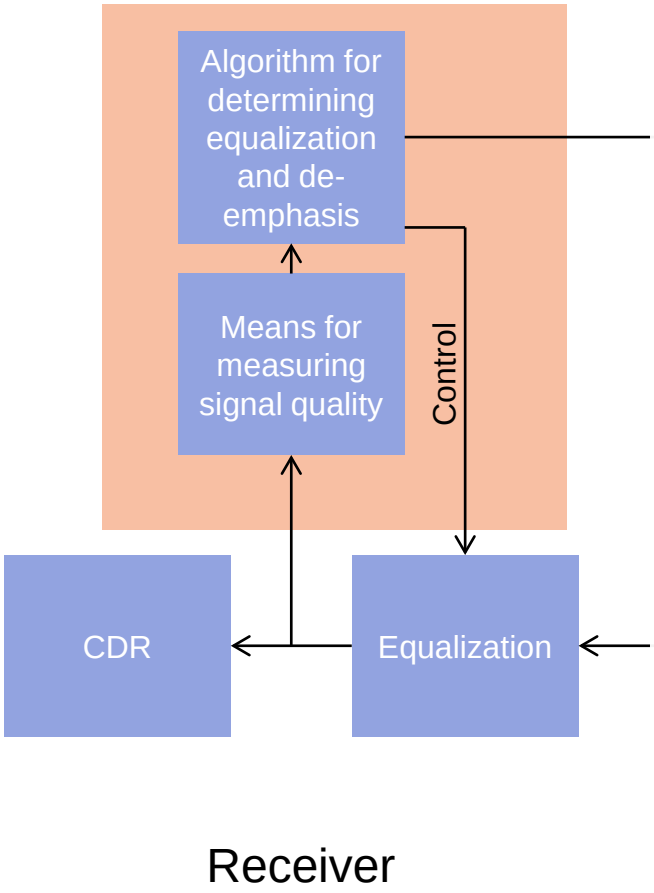
Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.10 and 2.11 focus on the receiver



Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.10 and 2.11 focus on the receiver



Receiver

The PCIe 3.0 Receiver Link Equalization Tests specified in 2.10 and 2.11 are the most important test of a DUT, they:

- Determine the DUT's ability to request appropriate amounts of transmitter equalization
- Determine the DUT's ability to internally apply the appropriate amount of receiver equalization
- Determine the quality of the DUT's algorithm for optimizing the link quality
- Determine the DUT's ability to optimize TxEQ and RxEQ in a short period of time

Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.10 – Link EQ RX Test for AIC

What does the test do?

This tests checks if the AIC is able to optimize the systems TX to achieve a link with a target ber of 10^{-12}.

How does the test work?

The test system simulates the downstream port and trains the link up and into loopback through recovery. Phase 2 and phase 3 of the link equalization are performed and not bypassed. The test pattern used in loopback is the modified compliance pattern. The training is performed under full RX stress conditions. The same stress signal calibration used for test 2.8 RX Jitter Tolerance Test is applied.

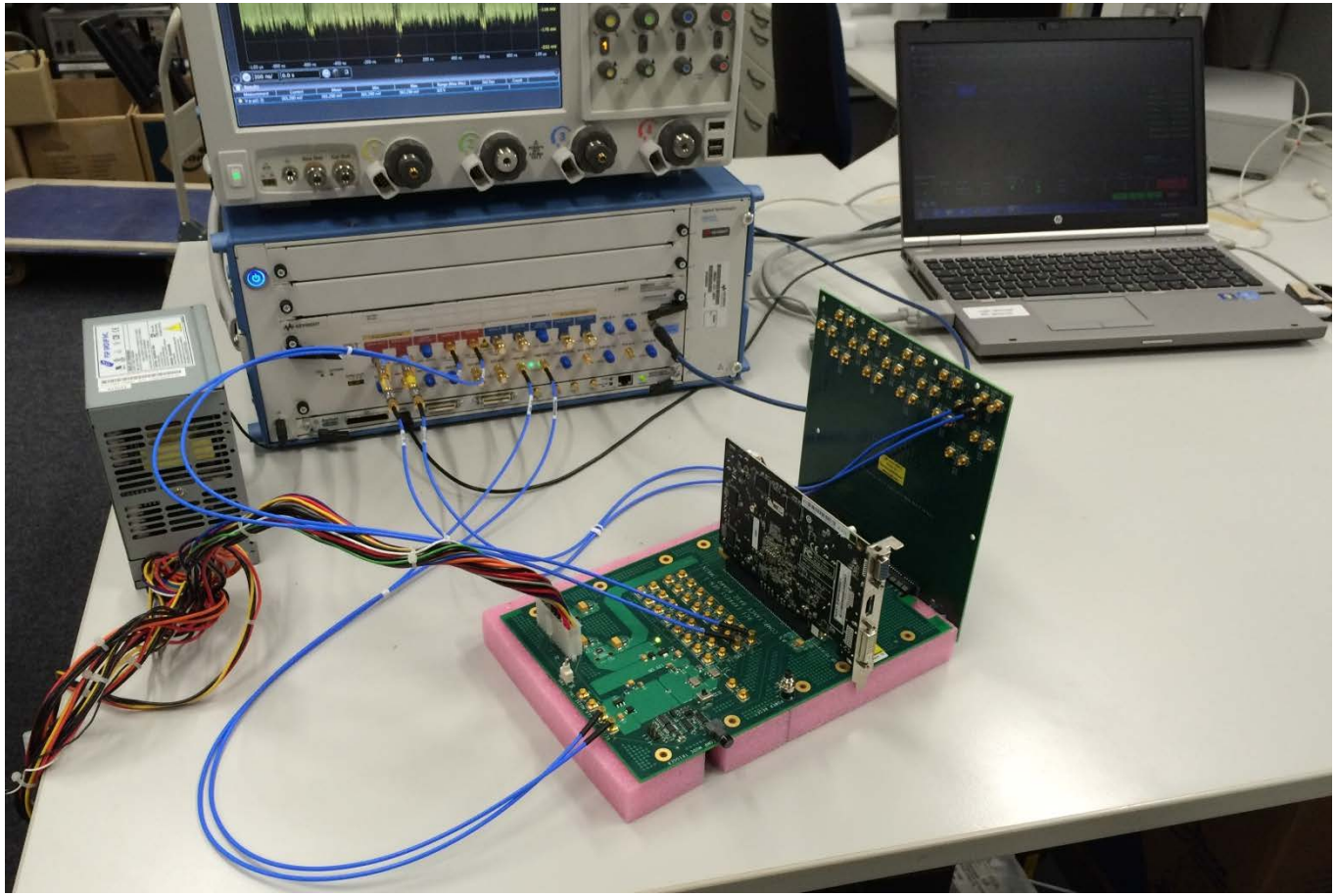
The test is performed P7 and P8 as BERT TX preset.

What are the requirements on the AIC to be able to perform this test?

The AIC must be able to be trained into loopback through recovery. The AIC must be able to perform phase 2 and phase 3.

Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.10 – Test Setup



J-BERT M8020A is used to train the device through L0 and recovery into loopback

Phase 2 and 3 are performed and the AIC optimizes J-BERT TX to the actual stress signal

J-BERT checks the looped signal for the ber

Very clean setup since no additional instruments or repeaters are required

Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.10 – Example Test Report

KEYSIGHT TECHNOLOGIES

BitifEye Digital Test Solutions

Show all results

Show only selected

Print

- Summary
- Instruments
- L0_Cal_8GTps_PreShoot
- L0_Cal_8GTps_DeEmphasis
- L0_Cal_8GTps_EQ_Preset
- L0_Cal_8GTps_EQ_Cust_Preset
- L0_Cal_8GTps_RJ
- L0_Cal_8GTps_SJ
- L0_Cal_8GTps_CBB3_DM_SI
- L0_Cal_8GTps_CBB3_Eye_Height
- L0_Cal_8GTps_CBB3_Eye_Width
- L0_Cal_8GTps_CBB3_Comp_Eye

Differential Mode Sinusoidal Interference	30.01 mV
Random Jitter	2.711 ps
Sinusoidal Jitter	12.5 ps
Offline	False
Enable Impairments for Link Training	True
Eye-Height	45 mV
Eye-Width	40.75 ps
Sinusoidal Jitter Frequency	100 MHz
BER Mode	FixedTime
BER Measurement Duration	125 s
Allowed Bit Error	1
Initial Preset	P7
DUT Tx Preset	P4
Data Rate Deviation	0 ppm
DUT Target Preset	P4
Interactive Training Script File	C:\Documents and Settings\All Users\Application Data\Bitifeye\Valiframe\Settings\PCIExpress3\Pcie3_8G_M8020A_ILT_Loopback.txt
Suppress Loopback Training Messages	False
Use CDR	True
CDR Loop Bandwidth	12 MHz
Peaking	1 dB
Analyzer Equalization	6dB
Capture and Compare Mode	False
Relax Time	3 s
Use Power Switch Automation	True
Power Switch Channel Number	2
Power Cycle Off On Duration	7 s
Power Cycle Settling Time	8 s
Power Cycle max. Retries for LB Training	3

Result	Initial Generator Preset	Final Generator Preset	Final Generator Pre-shoot [dB]	Final Generator De-emphasis [dB]	Allowed Bit Errors []	Measured Bit Errors []
pass	P7	20	2.50	-4.44	1	0
pass	P8	20	2.50	-4.44	1	0

Tx/Rx Link Equalization Testing for PCIe 3.0

Test 2.11 – Link EQ RX Test for Systems

What does the test do?

This tests checks if the system is able to optimize the AIC TX to achieve a link with a target ber of 10^{-12}.

How does the test work?

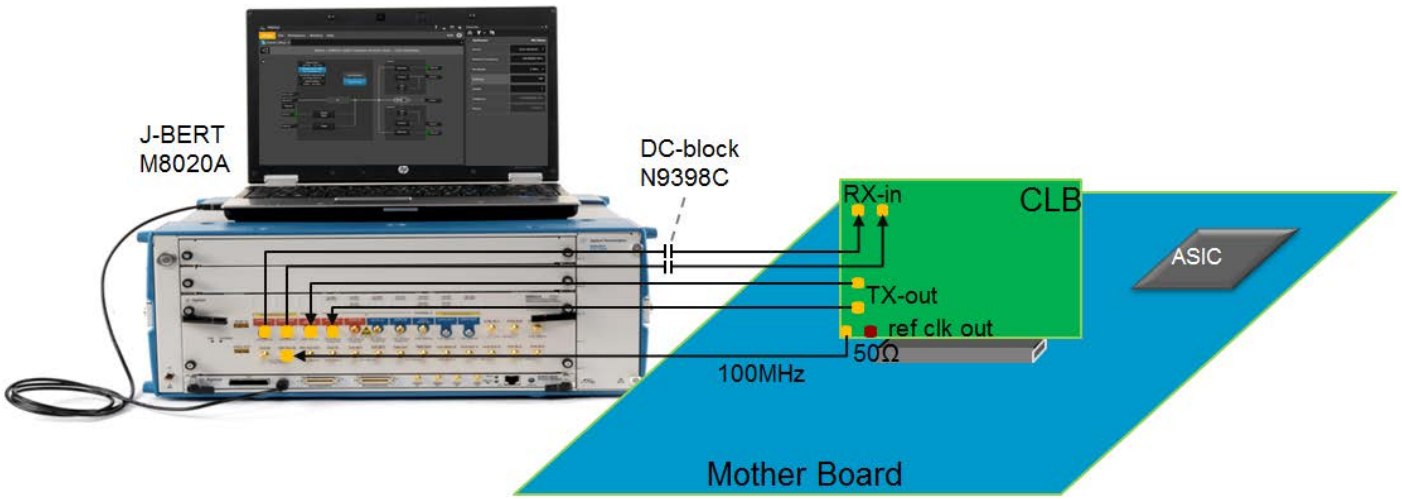
The test system simulates the downstream port and trains the link up and into loopback through recovery. Phase 2 and phase 3 of the link equalization are performed and not bypassed. The test pattern used in loopback is the modified compliance pattern. The training is performed under full RX stress conditions. The same stress signal calibration used for test 2.8 RX Jitter Tolerance Test is applied.

What are the requirements on the system to be able to perform this test?

The system must be able and set up in BIOS to be trained into loopback through recovery.
The system must be able and set up in BIOS to perform phase 2 and phase 3.

Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.11 – Test Setup



J-BERT is running on the system's 100MHz reference clock

J-BERT M8020A is used to train the device through L0 and recovery into loopback

Phase 2 and 3 are performed and the Systems optimizes J-BERT TX to the actual stress signal

J-BERT checks the looped signal for the ber

Very clean setup since no additional instruments or repeaters are required

Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.11 – Example Test Report

KEYSIGHT TECHNOLOGIES

BitifEye Digital Test Solutions

Show all results
Show only selected

Print

- Summary
- Instruments
- L0_Cal_8GTps_PreShoot
- L0_Cal_8GTps_DeEmphasis
- L0_Cal_8GTps_EQ_Preset
- L0_Cal_8GTps_EQ_Cust_Preset
- L0_Cal_8GTps_RJ
- L0_Cal_8GTps_SJ
- L0_Cal_8GTps_CBB3_DM_SI
- L0_Cal_8GTps_CLB3_Eye_Height
- L0_Cal_8GTps_CLB3_Eye_Width
- L0_Cal_8GTps_CLB3_Comp_Eye
- L0_Rx_8GTps_CLB3_DeEmph_Scan
- L0_Rx_8GTps_CLB3_PreSh_Scan
- L0_Rx_8GTps_CLB3_Comp_2.9
- L0_EqRx_8GTps_CLB3_Com_2.11
- L0_Tx_8GTps_EQ_Comp_2_7

Product Number: PCI Express PCI Express 3 Station Unknown User 8/11/2015 10:52:47 AM

L0_EqRx_8GTps_CLB3_Com_2.11

for PCI Express 3.0 System

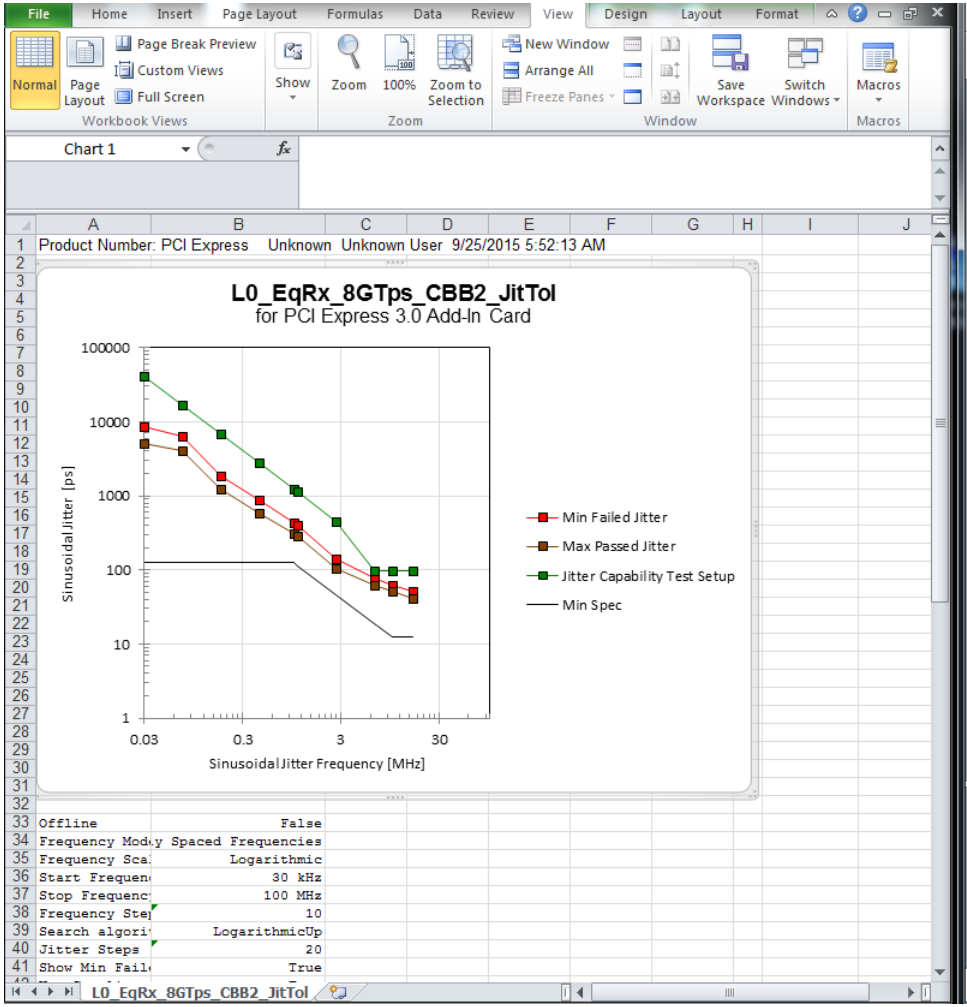
Differential Mode Sinusoidal Interference	26.96 mV
Random Jitter	2.735 ps
Sinusoidal Jitter	12.5 ps
Offline	False
Enable Impairments for Link Training	True
Eye-Height	49 mV
Eye-Width	44.5 ps
Sinusoidal Jitter Frequency	100 MHz
BER Mode	FixedTime
BER Measurement Duration	125 s
Allowed Bit Error	1
DUT Tx Preset	P4
DUT Target Preset	P7
Interactive Training Script File	C:\Documents and Settings\All Users\Application Data\Bitifeye\Valiframe\Settings\PCIExpress3\Pcie3_8G_M8020A_ILT_Loopback.txt
Suppress Loopback Training Messages	False
CDR Loop Bandwidth	12 MHz
Peaking	1 dB
Analyzer Equalization	6dB
Capture and Compare Mode	False
Relax Time	1 s
Use Power Switch Automation	False

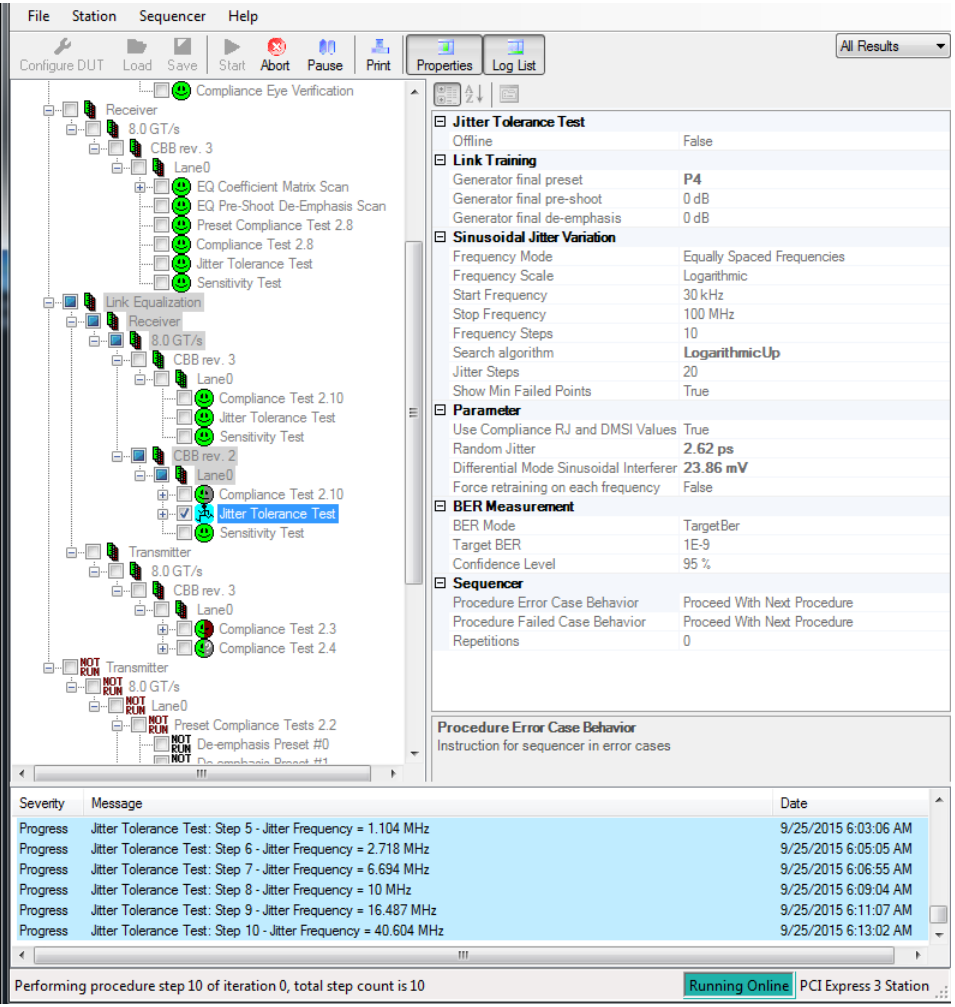
Result	Initial Generator Preset	Final Generator Preset	Final Generator Pre-shoot [dB]	Final Generator De-emphasis [dB]	Allowed Bit Errors []	Measured Bit Errors []
pass	P7	P6	2.50	0.00	1	0

Agenda

- Introduction
- Dynamic Link Equalization
- TX/RX Link Equalization Tests
- Test Automation
- RX Stress Signal Calibration
- Summary

N5990A Automation Software





N5990A Automation Software

Calibration and Test Overview

Test name	Result	
L0_Cal_8GTps_PreShoot	Passed	Cal point before (riser +) CBB + CLB
L0_Cal_8GTps_DeEmphasis	Passed	
L0_Cal_8GTps_EQ_Preset	Passed	
L0_Cal_8GTps_EQ_Cust_Preset	Passed	
L0_Cal_8GTps_RJ	Passed	
L0_Cal_8GTps_SJ	Passed	
L0_Cal_8GTps_CBB3_DM_SI	Passed	Cal point after (riser +) CBB + CLB
L0_Cal_8GTps_CBB3_Eye_Height	Passed	
L0_Cal_8GTps_CBB3_Eye_Width	Passed	
L0_Cal_8GTps_CBB3_Comp_Eye	Passed	
L0_Ver_8GTps_CBB3_Comp_Eye	Passed	
L0_Rx_8GTps_CBB3_EQtable	Passed	Long Channel RX Tests without Link EQ (Short channel RX tests are optional)
L0_Rx_8GTps_CBB3_DeEmph_Scan	Passed	
L0_Rx_8GTps_CBB3_PreSh_Scan	Passed	
L0_Rx_8GTps_CBB3_PreComp_2.8	Passed	
L0_Rx_8GTps_CBB3_Comp_2.8	Passed	
L0_Rx_8GTps_CBB3_JitTol	Passed	
L0_Rx_8GTps_CBB3_Sensitivity	Passed	
L0_EqRx_8GTps_CBB3_Com_2.10	Passed	Long Channel RX Link EQ Test
L0_EqRx_8GTps_CBB3_JitTol	Passed	
L0_EqRx_8GTps_CBB3_Sens	Passed	
L0_EqRx_8GTps_CBB2_Com_2.10	Passed	Short Channel RX Link EQ Test
L0_EqRx_8GTps_CBB2_JitTol	Passed	
L0_EqRx_8GTps_CBB2_Sens	Passed	
L0_Tx_8GTps_EQ_2_3	Passed	TX Link EQ Test
L0_Tx_8GTps_EQ_Comp_2_4	Passed	

N5990A Automation Software

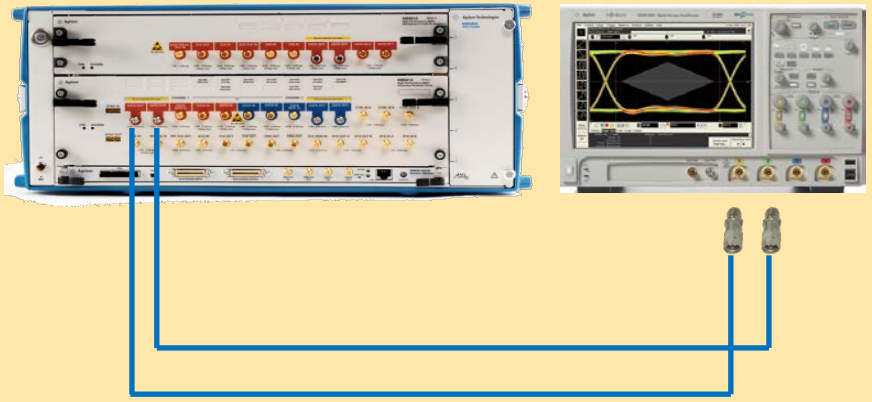
Cal and Test Coverage

- DUT Types:
  - Chip – Base Specification
  - System – Electrical PHY Test Specification (CEM)
  - AIC – Electrical PHY Test Specification (CEM)
  - Switch – Electrical PHY Test Specification (CEM)
  - U.2 system and U.2 device will be added
- 2.5GT/s, 5GT/s and 8GT/s
- Clocking Modes:
  - CC – common reference clock
  - SRNS – separate reference clock no SSC
  - SRIS – separate reference clock independent SSC
- Cal and Tests for:
  - RX
  - RX / TX Link EQ for 8GT/s
  - TX (interfacing to respective rt-scope compliance test application)

Agenda

- Introduction
- Dynamic Link Equalization
- TX/RX Link Equalization Tests
- Test Automation
- RX Stress Signal Calibration
- Summary

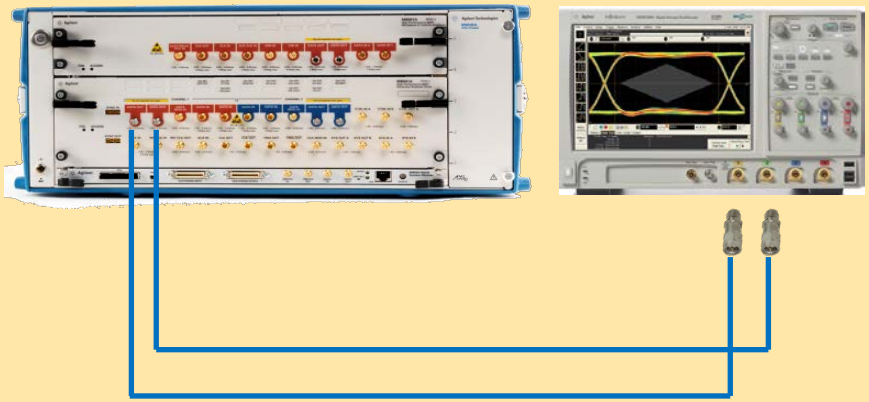
Presets and Amplitude



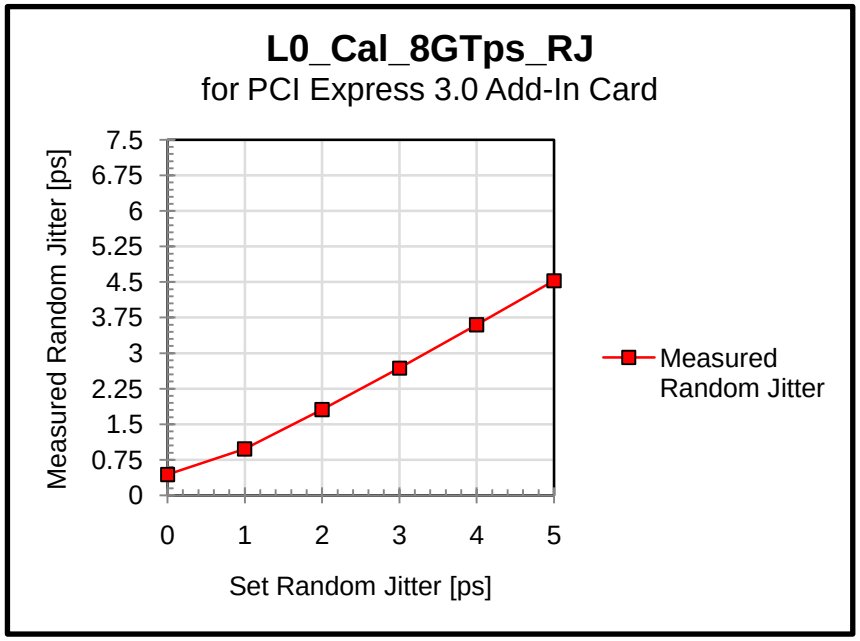
Automated by ValiFrame Software

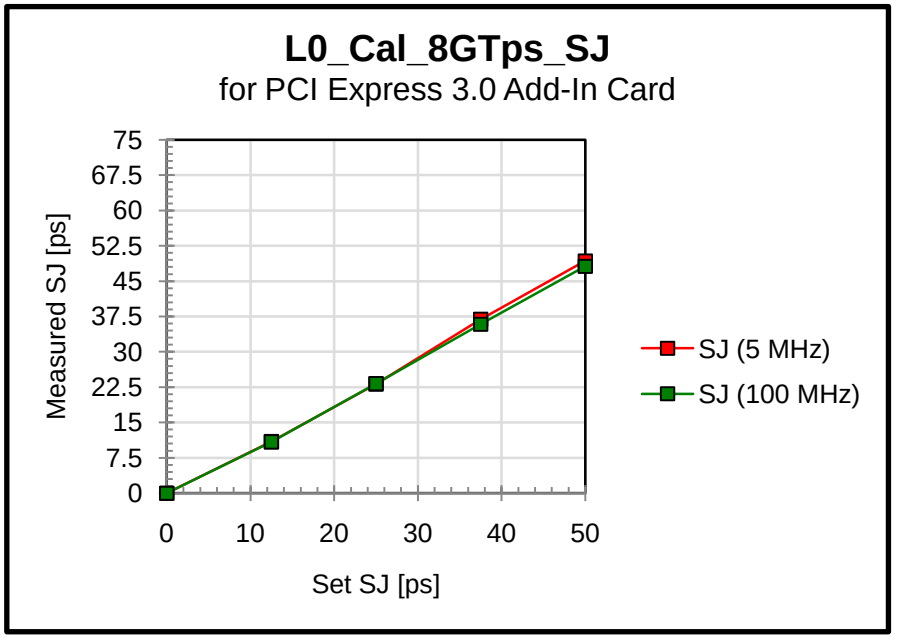
Preset	Pre-Shoot [dB]	De-Emphasis [dB]	Differential Voltage [mV]	Set Pre-Shoot [dB]	Set De-Emphasis [dB]	Set Differential Voltage [mV]
0	0.00	-6.00	800	0.08	-6.02	691
1	0.00	-3.50	800	-0.03	-3.68	681
2	0.00	-4.40	800	0.09	-4.43	676
3	0.00	-2.50	800	0.02	-2.65	681
4	0.00	0.00	800	0.11	-0.32	766
5	1.90	0.00	800	1.92	-0.27	752
6	2.50	0.00	800	2.58	-0.17	755
7	3.50	-6.00	800	3.36	-5.83	681
8	3.50	-3.50	800	3.38	-3.34	664
9	3.50	0.00	800	3.53	-0.09	744

SJ and RJ

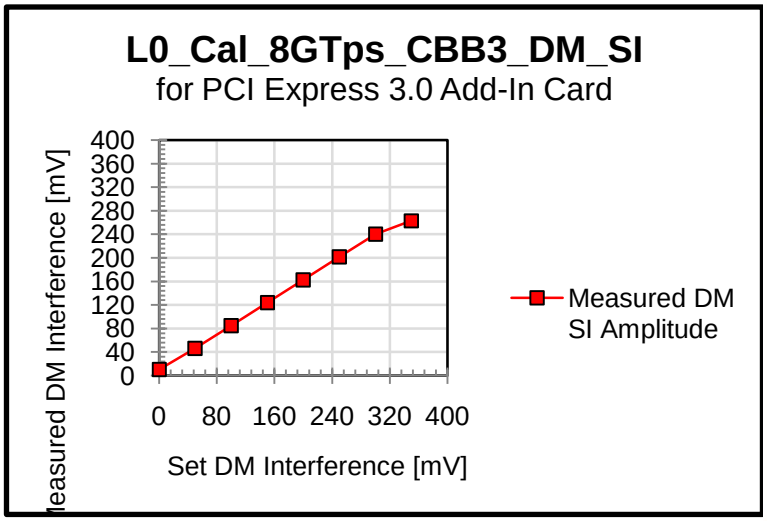


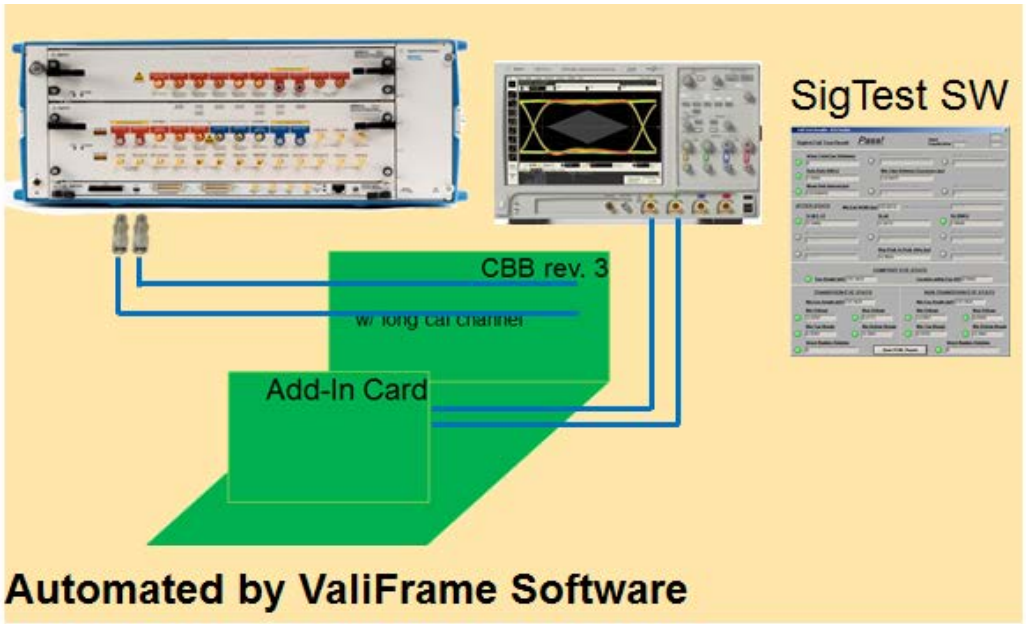
Automated by ValiFrame Software

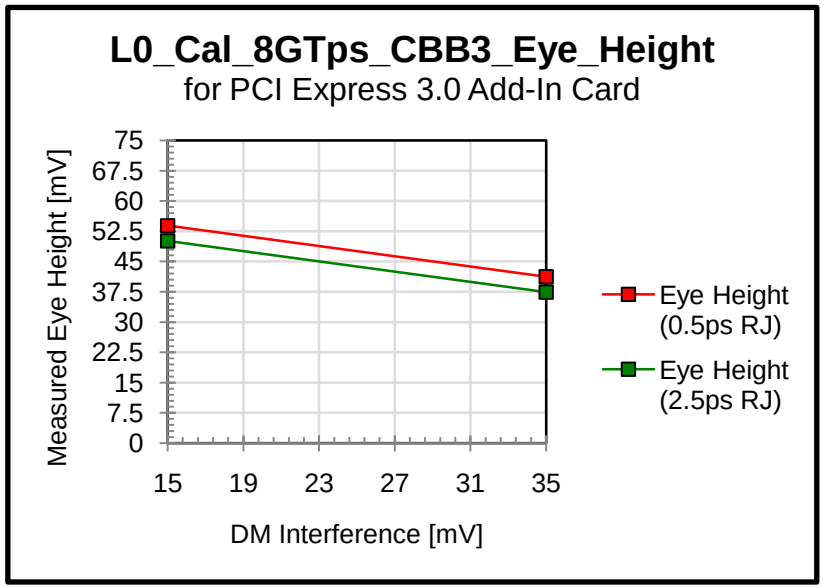


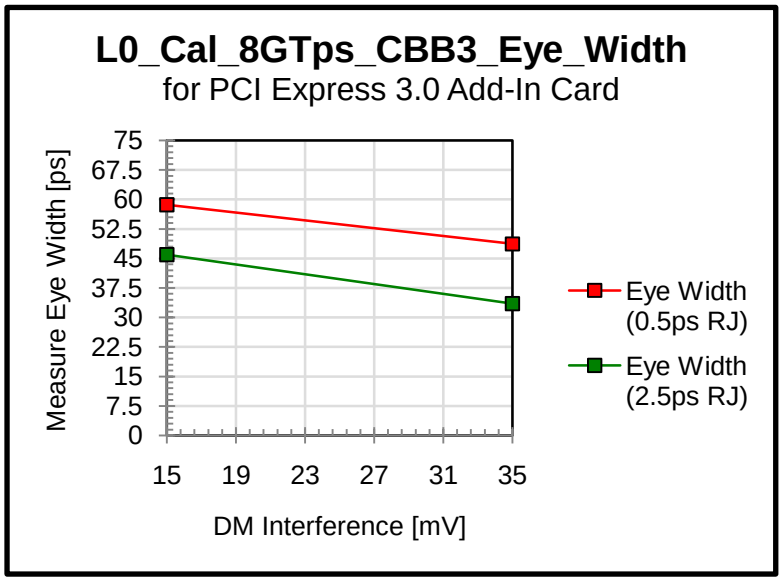


DMI and Eye


L0_Cal_8GTps_CBB3_DM_SI
for PCI Express 3.0 Add-In Card
Measured DM SI Amplitude
Set DM Interference [mV]
0 80 160 240 320 400
0 40 80 120 160 200 240 280 320 360 400


SigTest SW
CBB rev. 3
Add-In Card
Automated by ValiFrame Software


L0_Cal_8GTps_CBB3_Eye_Height
for PCI Express 3.0 Add-In Card
Measured Eye Height [mV]
DM Interference [mV]
Eye Height (0.5ps RJ)
Eye Height (2.5ps RJ)
0 7.5 15 22.5 30 37.5 45 52.5 60 67.5 75
15 19 23 27 31 35


L0_Cal_8GTps_CBB3_Eye_Width
for PCI Express 3.0 Add-In Card
Measure Eye Width [ps]
DM Interference [mV]
Eye Width (0.5ps RJ)
Eye Width (2.5ps RJ)
0 7.5 15 22.5 30 37.5 45 52.5 60 67.5 75
15 19 23 27 31 35

Final Calibrated Eye

Set up BERT to generate compliance pattern with P7 activated:

1. Adjust DM-SI to meet specified EH
2. Adjust RJ to meet specified EW
3. Re-check EH and if necessary re-adjust DM-SI once
4. Record the final calibration values RJ_{cal} and $DM\text{-}SI_{cal}$ for later usage

L0_Cal_8GTps_CBB3_Comp_Eye

for PCI Express 3.0 Add-In Card

SigTest Ver	3.1.63
BERT System	DE54300110
Offline	False
Max Number	8
Number of A	5
Scope Conne	ect Connect
Jitter Unit	Time

DMSI [mV]	RJ [ps]	Eye-Height [mV]	Eye-Width [ps]
21.3	2.85	44.8	41.2

CEM Rx Jitter Tolerance Spec

According to PCI Express Electrical PHY Test Specification

Parameter	Min	Max	Unit	SigTest	
				Technology	Template
Vpp		800	mV	N/A	N/A
RJ (Random Jitter)	1.5	1.7	ps RMS	PCI_3_0_RX_CAL	PCIE_3_8GB_Rx_Sj_CAL
SJ (Sinusoidal Jitter) @ 100 MHz	12.5	13.5	ps PP	PCI_3_0_RX_CAL	PCIE_3_8GB_Rx_Sj_CAL
Differential Mode Sinusoidal Interference at 2.1 GHz	14	16	mV PP	N/A	N/A
$V_{RX-EH-8G}$ Eye Height		AIC: 41 to 46 System: 45 to 50	mV	PCI_3_0_RX_CAL	AIC: PCIE_3_8GB_RX CARD_CAL_MULTI_CTLE_DFE_EMBED01 System: PCIE_3_8GB_RX SYS_CAL_MULTI_CTLE_DFE_ EMBED01
$T_{RX-EW-8G}$ Eye Width		AIC: 39.25 to 41.25 System: 43 to 45	ps	PCI_3_0_RX_CAL	AIC: PCIE_3_8GB_RX CARD_CAL_MULTI_CTLE_DFE_EMBED01 System: PCIE_3_8GB_RX SYS_CAL_MULTI_CTLE_DFE_ EMBED01

Setup

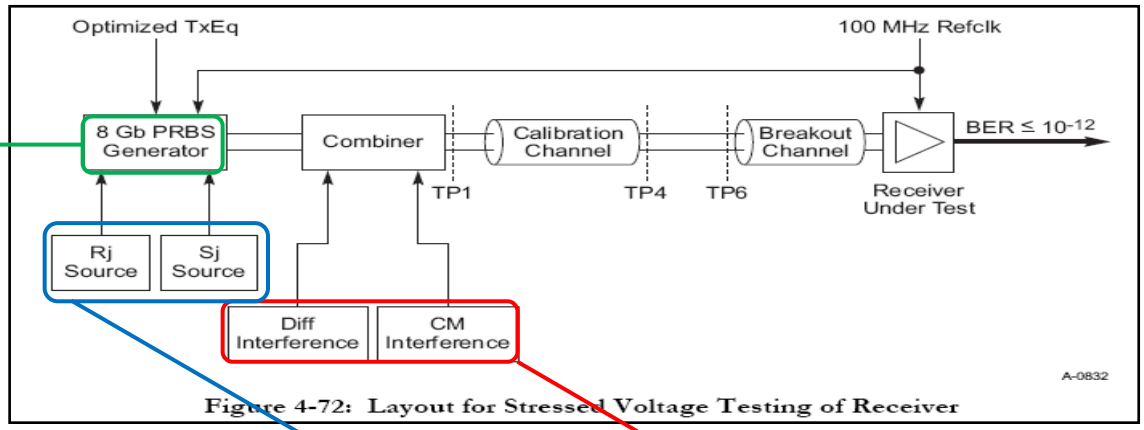
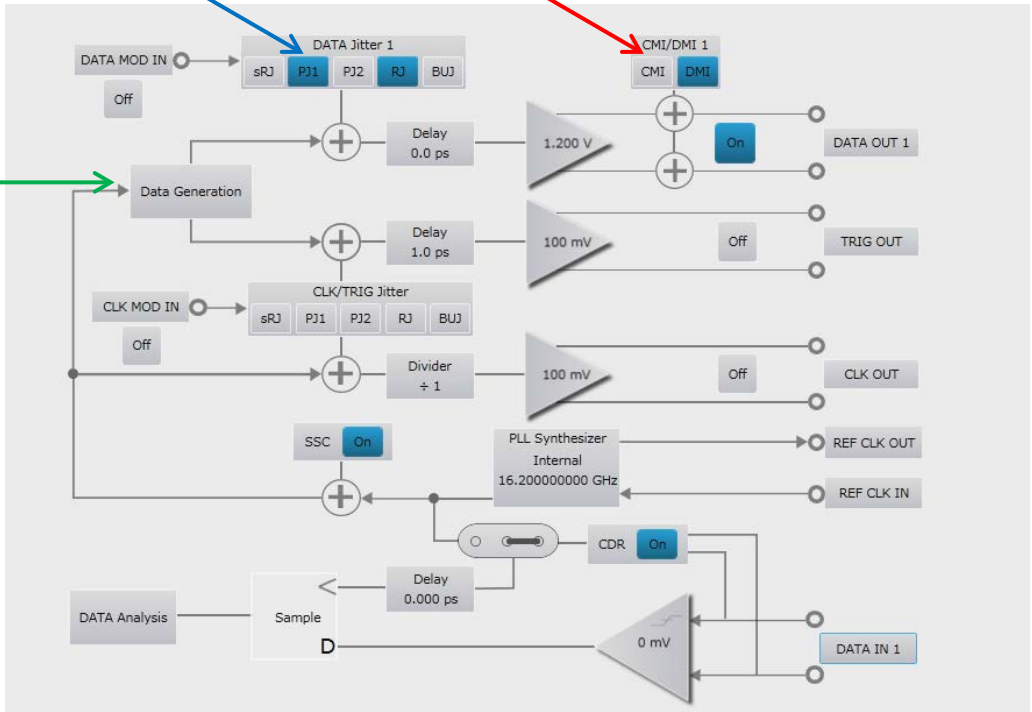


Figure 4-72: Layout for Stressed Voltage Testing of Receiver

Build in Jitter Sources:

- 8 Tap De-emphasis
- SJ
- RJ
- DMI
- CMI (Base Spec)
- Clock Multiplier
- ISI Channel Emulation
- Error Detector Equalization



Agenda

- Introduction
- Dynamic Link Equalization
- TX/RX Link Equalization Tests
- Test Automation
- RX Stress Signal Calibration
- Summary

PCI Express Link Equalization Testing

Summary

- The Link EQ Tests are designed to check the link equalization algorithms as well as the PHY performance
- The Link EQ RX Tests are better suited to test a DUT's ability to work in worst case channel scenario compared to the RX Jitter Tolerance Test
- The Link EQ Tests and especially the TX Link EQ Tests are time consuming and a test automation with automated remote power on/off switching is very helpful
- The J-BERT M8020A in combination with Keysight's V-, X-, Z- and Q- Series oscilloscopes and the N5990A Test Automation for PCIe covers all your RX, TX and Link EQ test needs
- The J-BERT M8020A is ready for testing 16Gb/s today!

Thank you!