Keysight Measurement Forum 2016

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Board Design & Simulation with Recent Enhancements EEsof ADS Signal and Power Integrity

KEYSIGHT TECHNOLOGIES

HARDWARE+SOFTWARE+PEOPLE=INSIGHTS

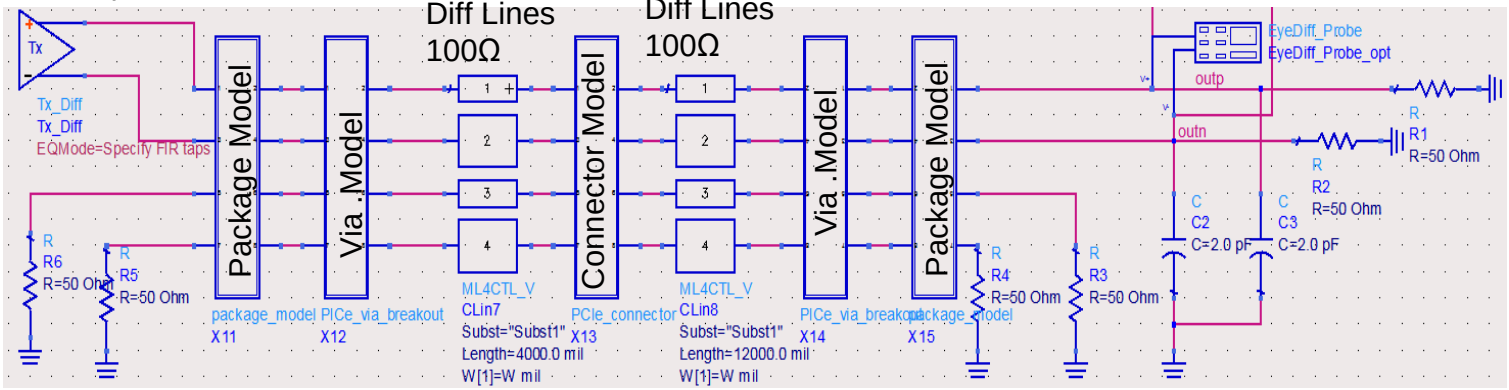
Agenda Super Speed USB with Type-C Connector

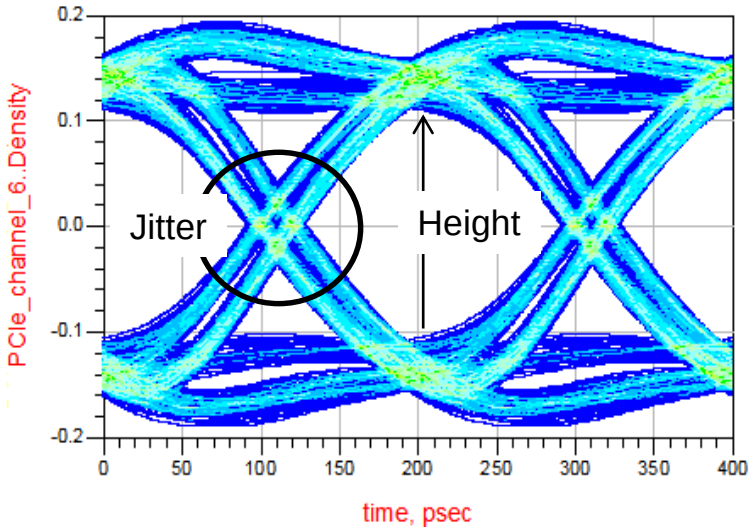
- Motivation: Why Simulation?
- Introduction of Super Speed USB Designs and Simulation Techniques
- Pre-Layout Study and Analysis
- Channel Modeling, Simulation and Optimization
- Post-Layout Analysis
  - IR-Drop-, PDN-Impedance-, Power Plane Resonance- and Power Aware SI Analysis
- Compliance Test, Design Guides and Utilities
- Demo and Advanced Design Techniques

Motivation: Why Simulation [1]

Channel Simulation

De-Emphasis=5dB

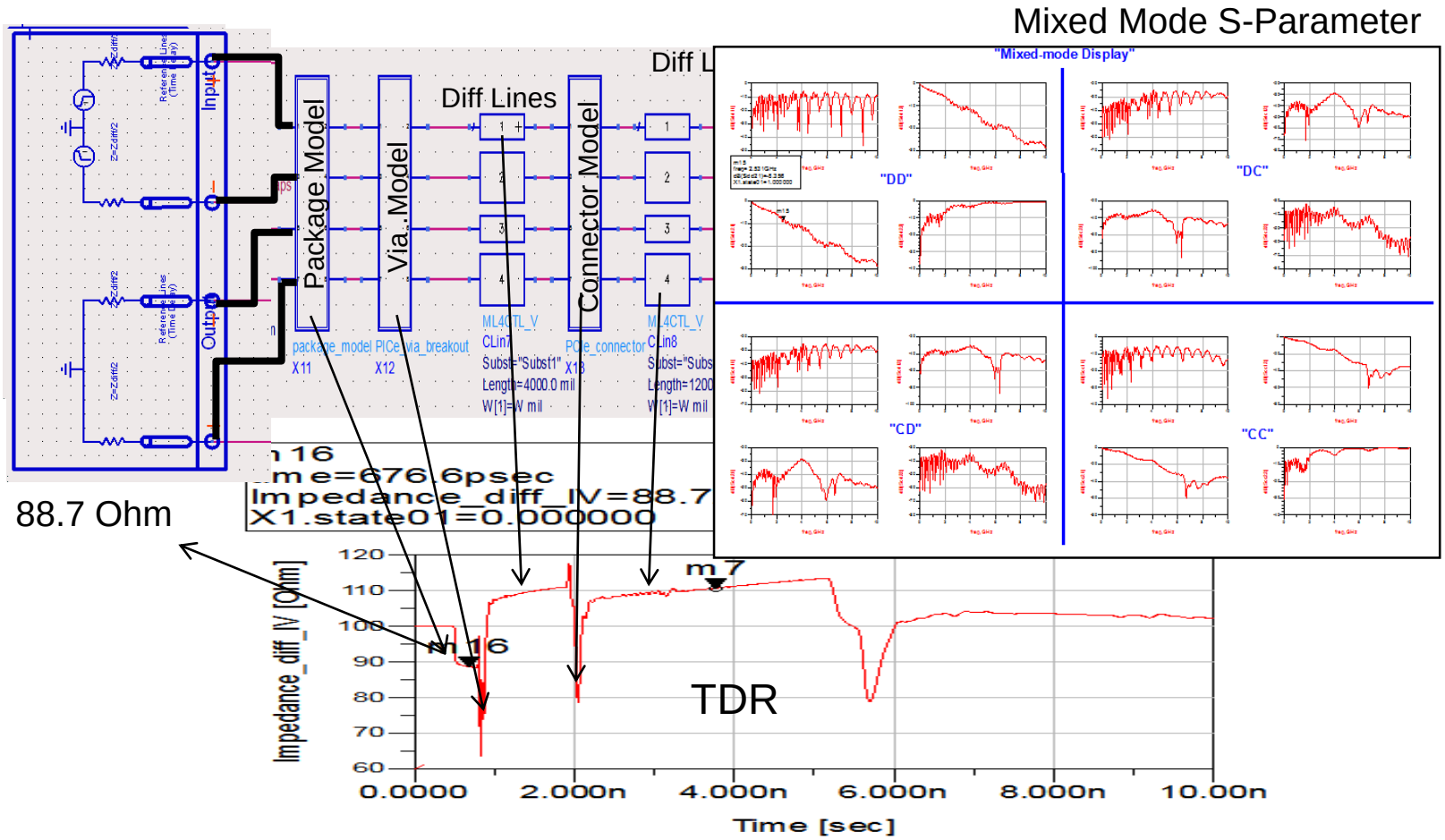




measurement	...channel_6..Summary
Level1	0.140
Level0	-0.139
LevelMean	4.692E-4
Amplitude	0.279
Height	0.192
HeightDB	-7.167
Width	1.592E-10
SNR	9.377
RiseTime	8.862E-11
FallTime	8.899E-11
JitterPP	4.080E-11
JitterRMS	1.050E-11
WidthAtBER	1.628E-10
HeightAtBER	0.218
CrossingLevel	-0.002

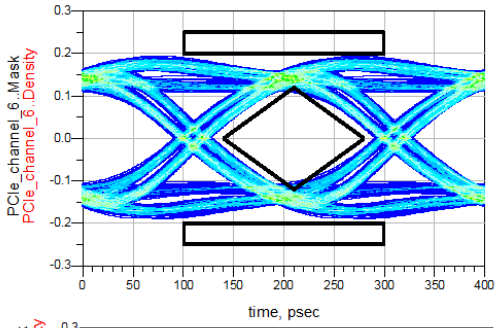
Motivation: Why Simulation [2]

TDR and Mixed Mode S-Parameter Simulation

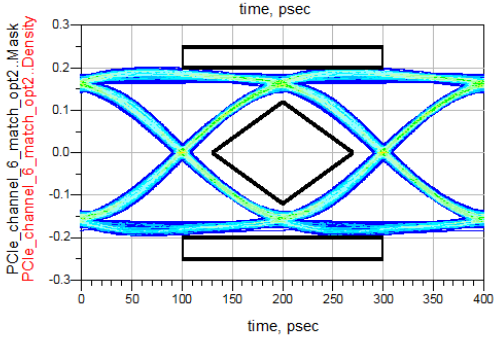


Motivation: Why Simulation [3]

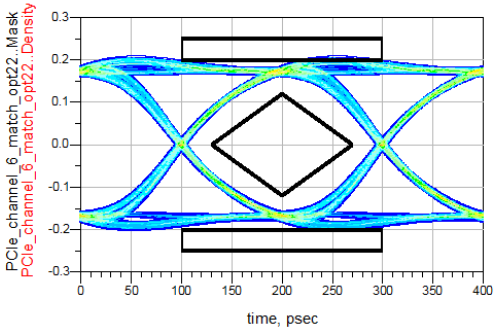
Optimization of the Channel traces (w, s), De-Emphasis and Matching



measurement	...channel_6..Summary
Level1	140.0 m
Level0	-139.1 m
LevelMean	469.2 u
Amplitude	279.1 m
Height	192.0 m
HeightDB	-7.167
Width	159.2 p
SNR	9.377
RiseTime	88.62 p
FallTime	88.99 p
JitterPP	40.80 p
JitterRMS	10.50 p
WidthAtBER	162.8 p
HeightAtBER	218.0 m
MaskViolated	1.000



measurement	...atch_opt2..Summary
Level1	161.4 m
Level0	-154.6 m
LevelMean	3.364 m
Amplitude	316.0 m
Height	256.0 m
HeightDB	-5.918
Width	182.0 p
SNR	13.89
RiseTime	91.20 p
FallTime	92.00 p
JitterPP	15.91 p
JitterRMS	3.182 p
WidthAtBER	182.4 p
HeightAtBER	279.0 m
MaskViolated	1.000
CrossingLevel	1.000 m



measurement	...atch_opt22..Summary
Level1	172.0 m
Level0	-167.2 m
LevelMean	2.408 m
Amplitude	339.1 m
Height	290.0 m
HeightDB	-5.376
Width	188.4 p
SNR	20.69
RiseTime	77.40 p
FallTime	78.57 p
JitterPP	11.60 p
JitterRMS	2.466 p
WidthAtBER	188.0 p
HeightAtBER	314.0 m
MaskViolated	1.000
CrossingLevel	1.000 m

Improvement Factor of
Eye Height → +50%
Jpp →3/4 less Jitter

Eye Height	Jrms	Jpp
Before Optimization		
192	10.5psec	40.8psec
Optimization of de-emphasis and Traces		
256	3.182psec	15.91psec
Opt. De-emph. Traces and Matching		
290	2.66psec	11.6psec

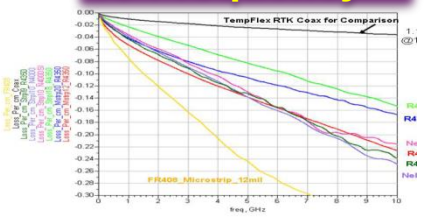
Introduction: Super Speed USB

Difference between USB 3.0 and USB 3.1

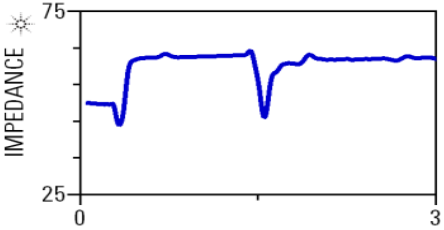
	USB 3.0 (Gen1/SuperSpeed)	USB 3.1 (Gen2/SuperSpeed+)
Data Rate	5 Gb/s	10 Gb/s
Coding	8b/10b	128b/132b
Target Channel	3 meter (-17 dB @ 2.5 GHz)	1 meter (-20 dB @ 5 GHz)
CDR	JTF BW 4.9Mhz	JTF BW 7.5Mhz
SSC	Slew rate test	New df/dt requirement: 1250 (max) ppm/µs
De-emphasis	Post: -3dB (Required)	Pre: 2.7dB (Informative) / Post: -3dB (Informative)
RX Ref EQ	CTLE	CTLE + 1 tap DFE
Eye Height, TJ	100mV, 132ps(.66UI)	70mV, 71.3ps(.714UI)

Challenge in HSD-Design - Physical Layer Constraints

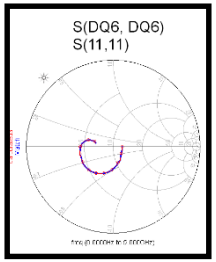
Material Loss vs Frequency



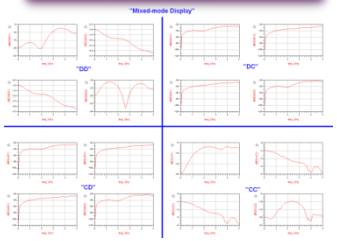
Interconnections Impedance TDR



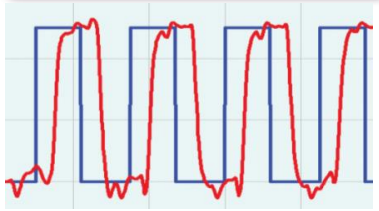
Matching

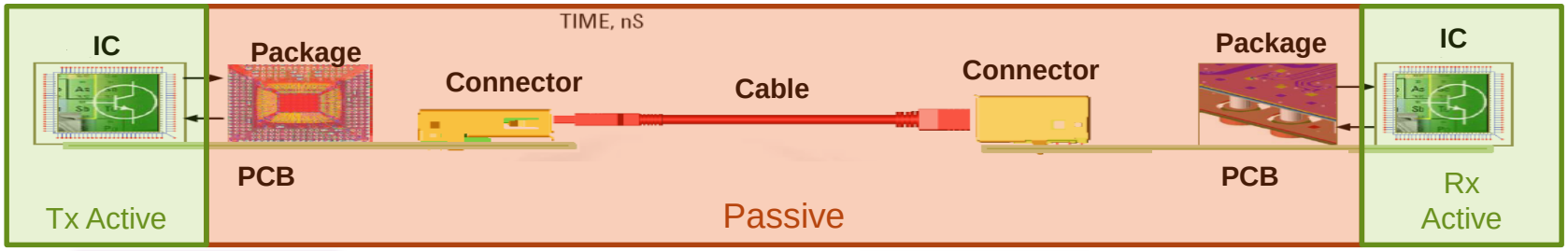


EMI/X-Talk Mixed Mode

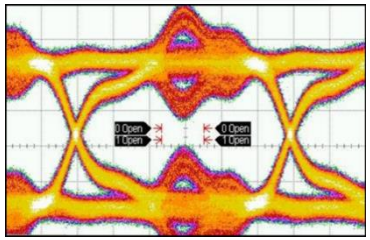


Electrical Length Skew

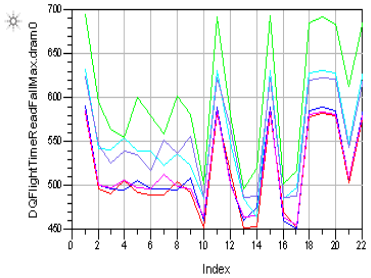




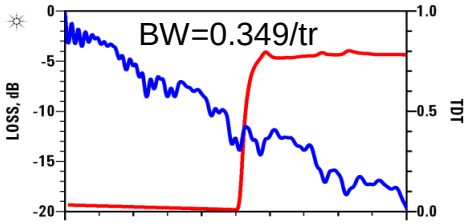
Cross Talk and Jitter



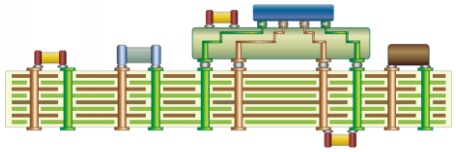
Tolerances



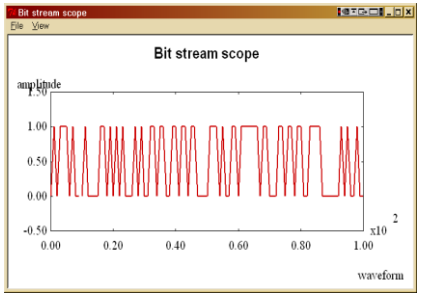
Bandwidth RiseTime



Power Integrity, $L(\frac{di}{dt})$



USB 3.1 Type-C Example



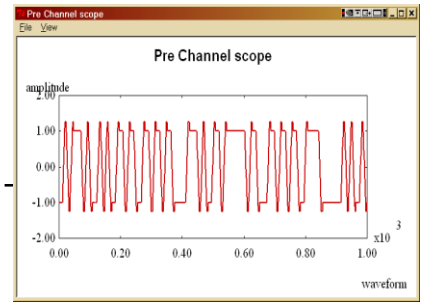
Channel Adaptation- IBIS-AMI Model

IC Design

Pattern Generator

Encoder 128b/132b

Pre-emphasis/Driver



Die

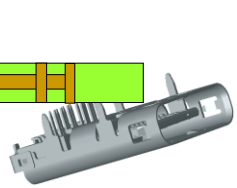
Driver

Tx

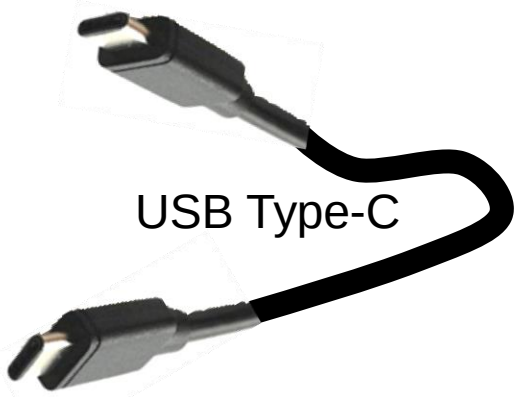
Package

Card

Board Traces/Vias



USB Type-C



Board/Connector/Package Design

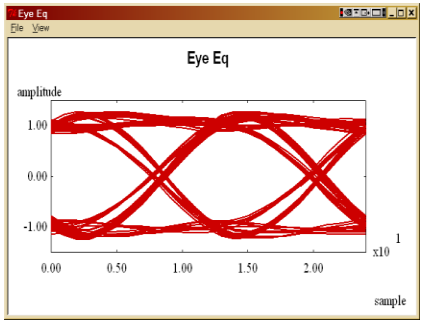
Rx

Die

Receiver

Package

Card

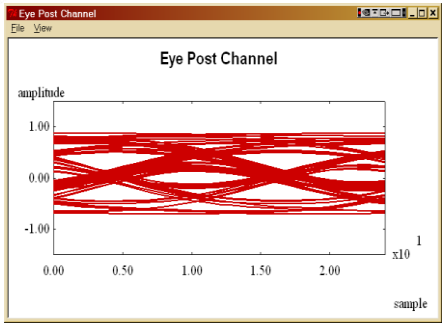


IC Design - IBIS-AMI-Model

Decoder

Equalizer

Signal Recovery



CTLE + 1 tap DFE

KEYSIGHT TECHNOLOGIES

USB Type-C Pre-Layout Study using ADS

Package Model

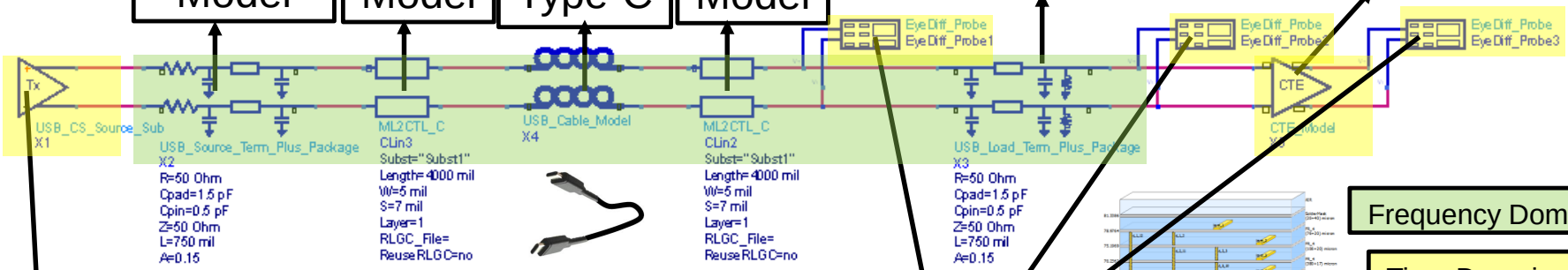
PCB Model

USB Type-C

PCB Model

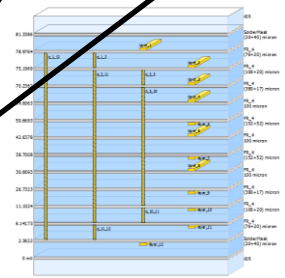
Package + Load Termination

Rx or IBIS-AMI Equalizer CTE/DFE/FFE



Channel Simulator

Eye Probes

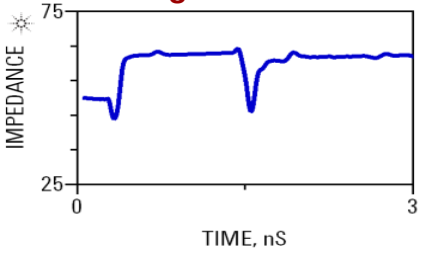


Frequency Domain

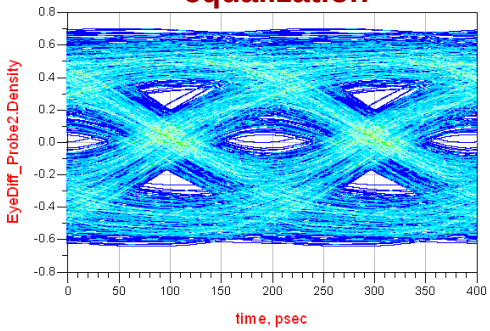
Time Domain

Tx or IBIS-AMI
PRBS
8B10B Encoder
De/Pre-Emphasis
Impedance
Jitter

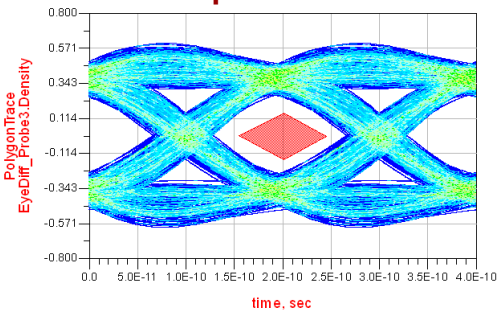
TDR, Impedance along the Channel



Eye diagram before equalization



Eye diagram after equalization

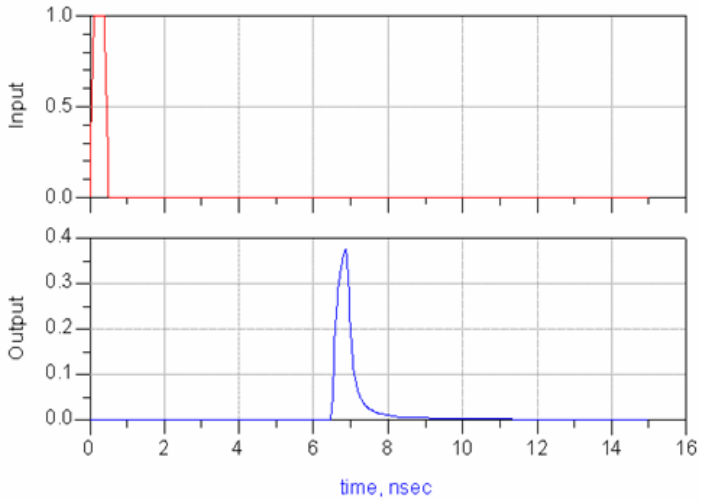


KEYSIGHT TECHNOLOGIES

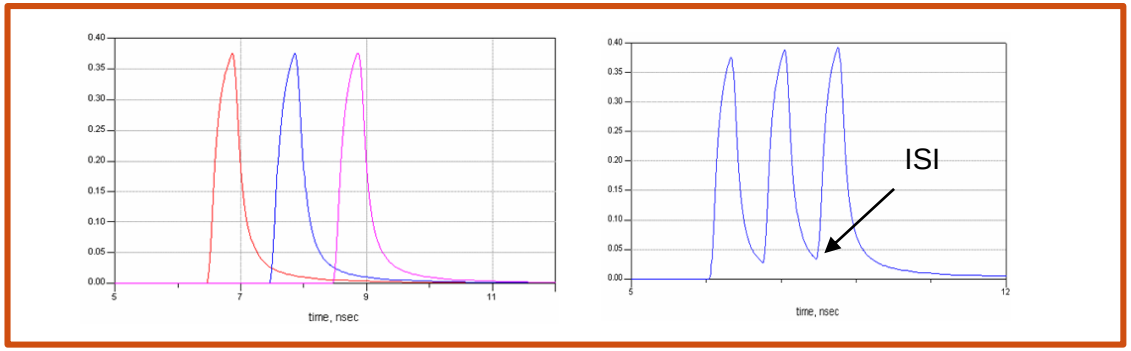
Channel Simulation Technologies

Fast Channel Simulation – Ultra Low BER

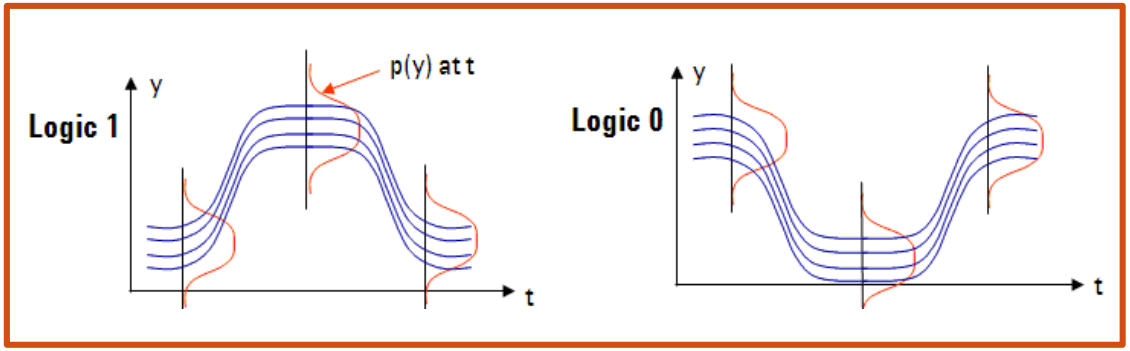
Step response calculated using short SPICE-like transient simulation



Bit by bit mode : Superposition of bits



Statistical mode : Statistical techniques

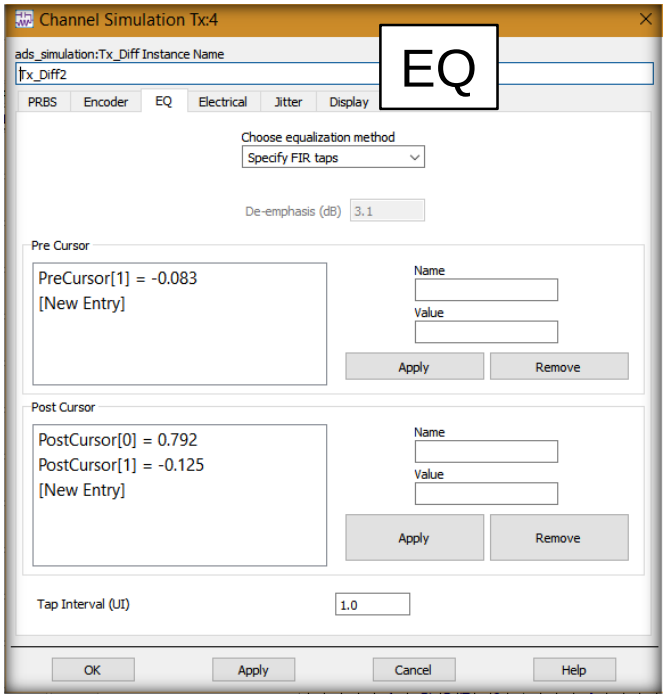


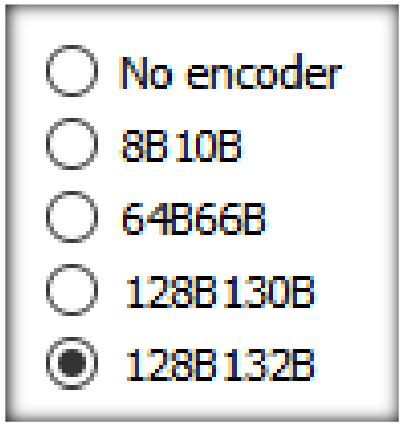
USB3.1 - Tx Source or IBIS-AMI

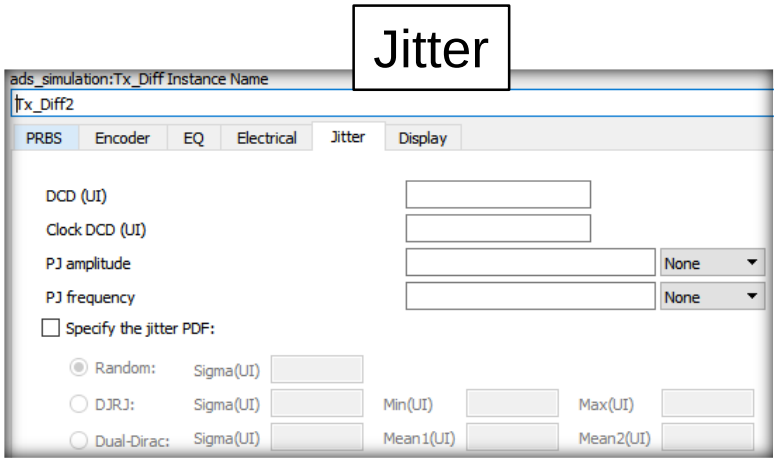
10 Gbps Channel Source

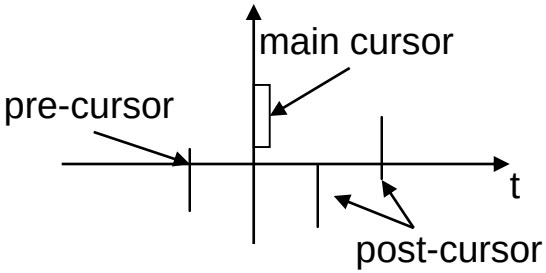
Pre: 2.7dB (Informative)

Post: -3dB (Informative)

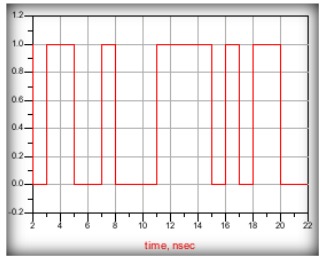




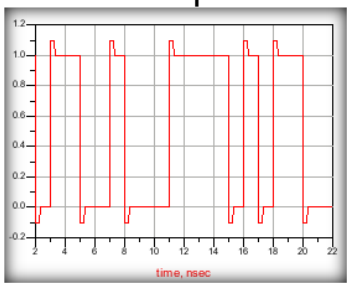




Before emphasis



After emphasis



USB3.1 Rx - Receiver Model or IBIS_AMI

Continuous-Time-Linear Equalizer (CTLE): pole-zero

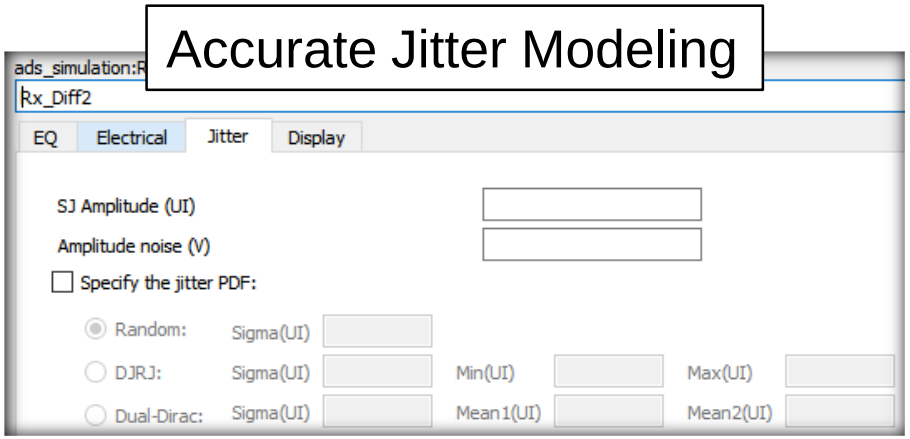
Feed-Forward-Equalizer (FFE)

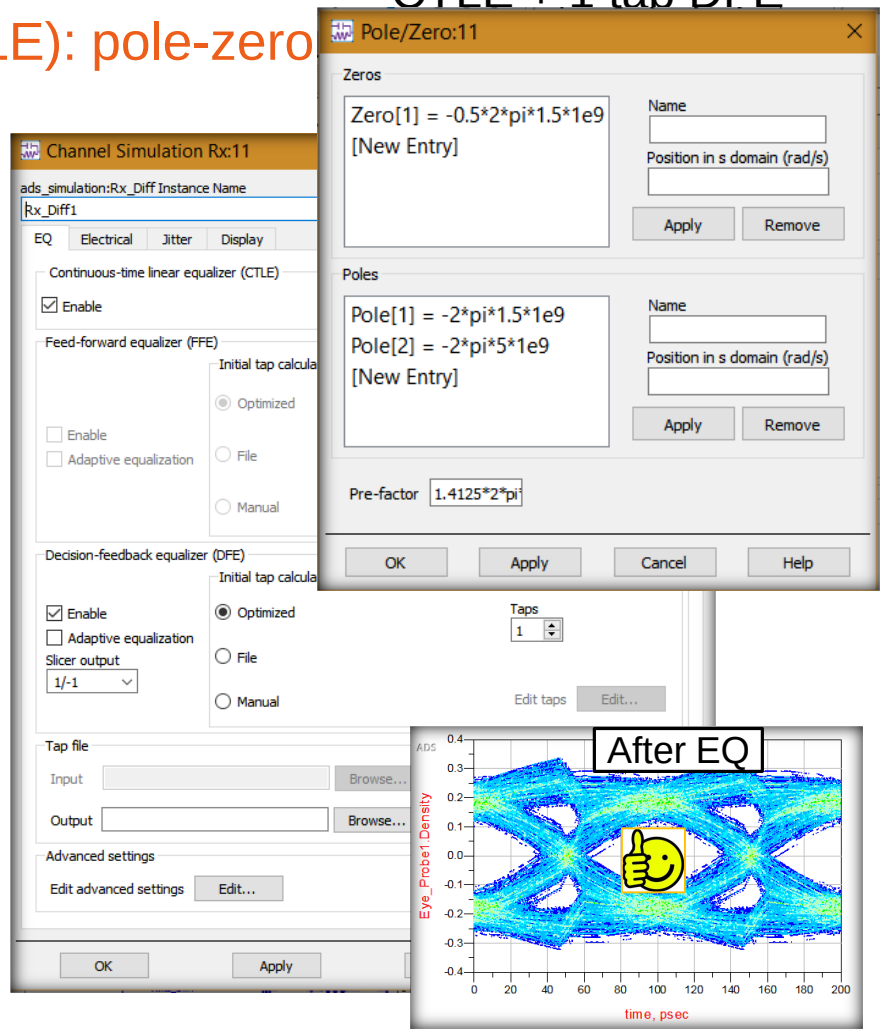
Decision Feedback Equalizer (DFE)

Optimization of Taps

Download Tap-Coefficients to File

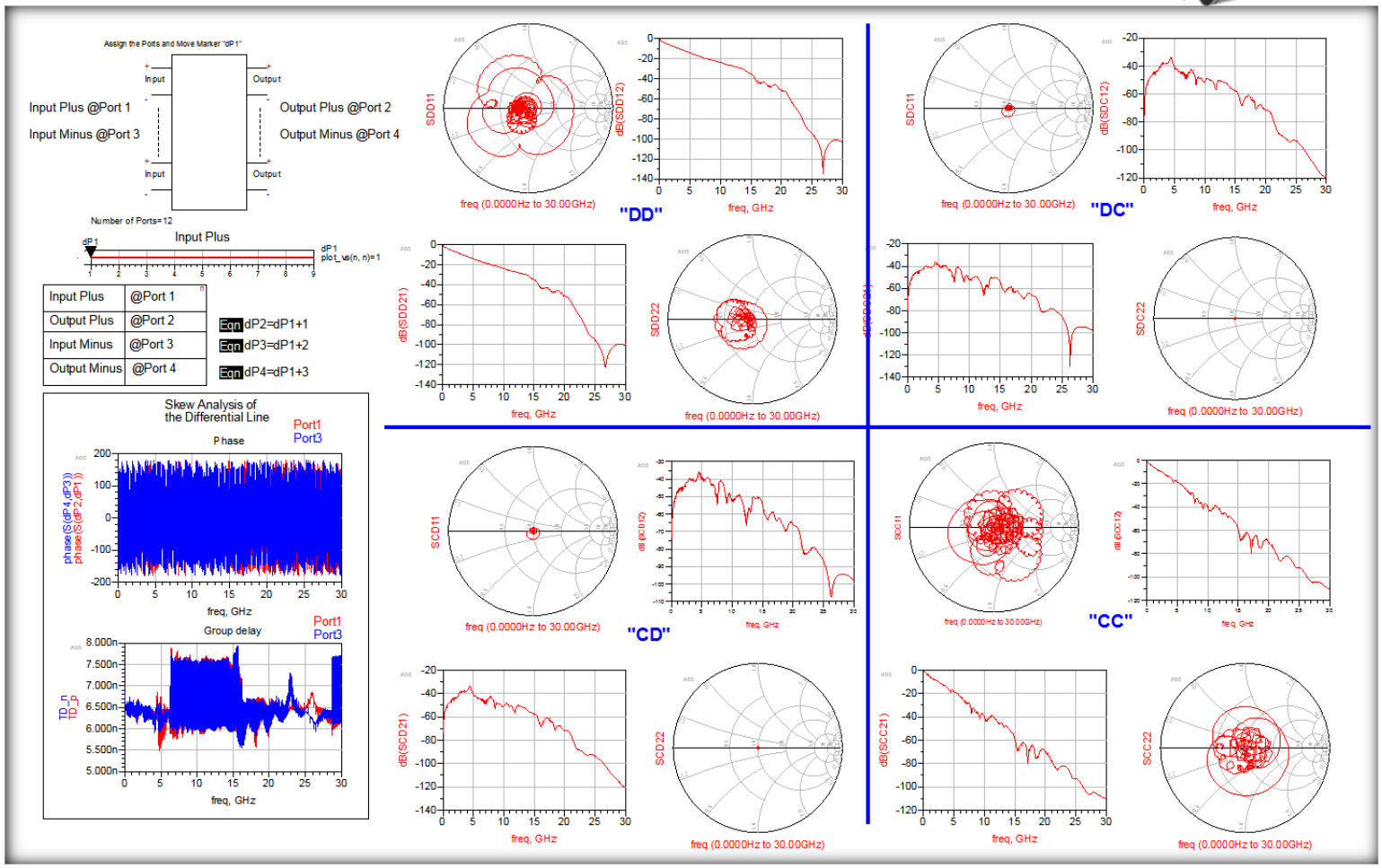
CTLE + 1 tap DFE





Pre-Layout Study USB Type-C Connector

S-Parameter - Connectors and 1 Meter Cable



Pre-Layout Study USB Type-C

TDR - Connectors and 1 Meter Cable

Assign the Ports and Move Marker "dP1"

Input Plus @Port 1

Input Minus @Port 3

Output Plus @Port 2

Output Minus @Port 4

Diff Input Looking into Port1,Port3

Input Plus

plot_vs(n, n)=1

Estimation - Locate Discontinuity move slider "Linput and Loutput"

Define er: Eqn er=3.9

Define Type v: v=1 (Microstrip Line) v=2 (Strip Line) v=3 (Coax Line) v=4 (Wire or Twisted Pair) Eqn v=1

Define v for the Wire: Eqn v_Wire=2e8 [m/sec]

Define Micro strip Data: Eqn w=5 mil, Eqn h=3.8 mil

TDR at Input: Move Marker "Linput"
TDR-Time=6.133 nsec
Propagation-Time=2.867 nsec
Location L=531.425 mm / 20.922 inch
Z=95.692 Ohm

TDR at Output: Move Marker "Loutput"
TDR-Time= 1.400 nsec
Propagation-Time=0.500 nsec
Location L(Loutput)=92.690 mm / 3.649 inch
Z(output)=73.712 Ohm

calculated v=1.854 *10e8 m/s

TDR from S-Parameter Simulation

Define the Parameter

Eqn Delay_Ref_Line=200 psec Eqn Zdiff=100

Eqn Tstop=20 nsec Eqn NumPts=301

Move the Marker win to select the Window type

Diff-in Diff-Out Window=Kaiser 7.865

Com-In Diff-Out Window=Kaiser 7.865

Diff-In Com-Out Window=Kaiser 7.865

Com-In Com-Out Window=Kaiser 7.865

Diff Output Looking into Port2,Port4

Input Plus	@Port 1
Output Plus	@Port 2
Input Minus	@Port 3
Output Minus	@Port 4

Eqn tP2=tP1+1

Eqn tP3=tP1+2

Eqn tP4=tP1+3

TDR from S-Parameter Simulation - Single Ended

Single Ended

Looking into Port1 Window=Kaiser 7.865

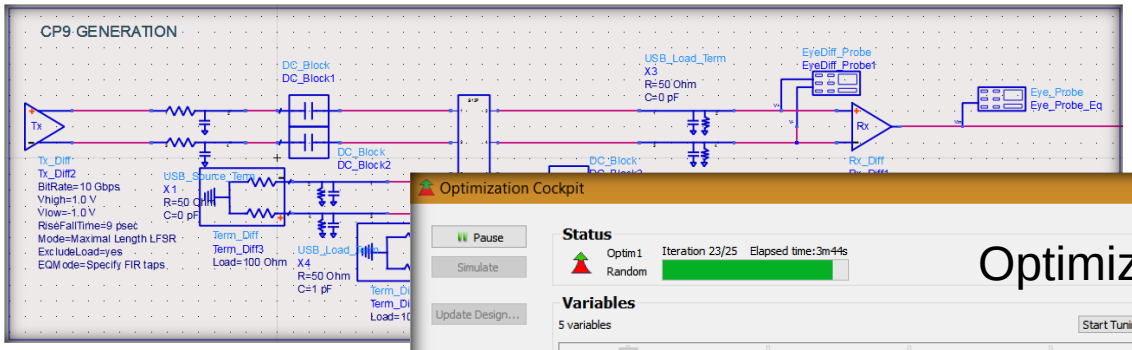
Looking into Port2 Window=Kaiser 7.865

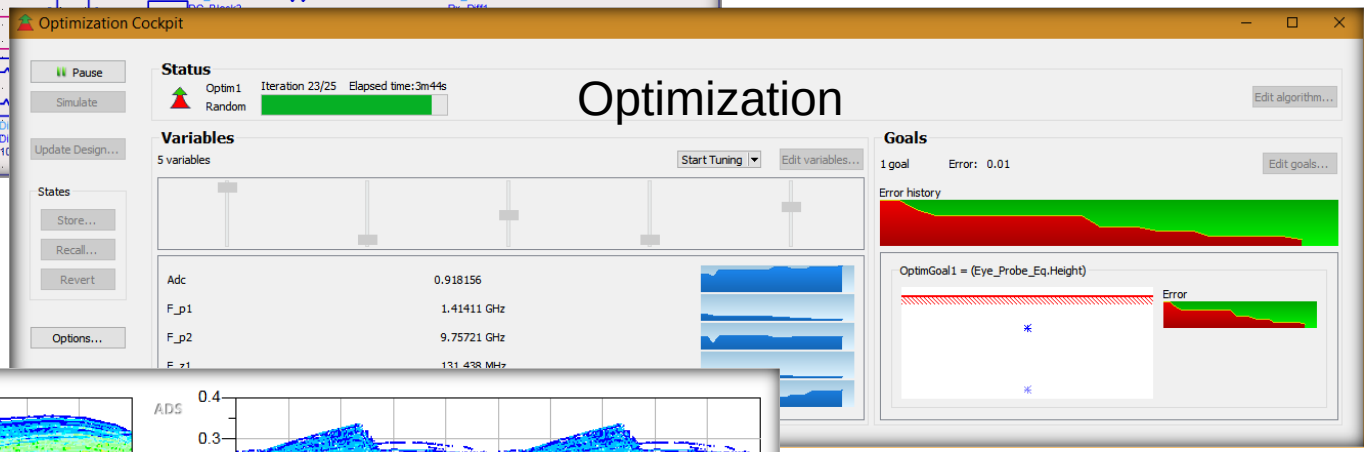
Looking into Port3 Window=Kaiser 7.865

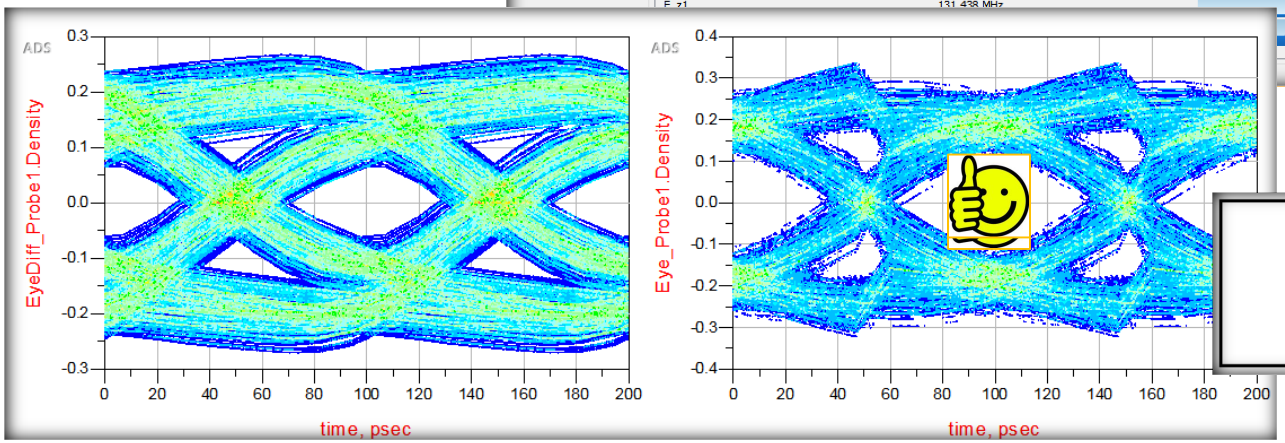
Looking into Port4 Window=Kaiser 7.865

Pre-Layout Study USB Type-C

Channel Simulation/Opt - Connector and Cable



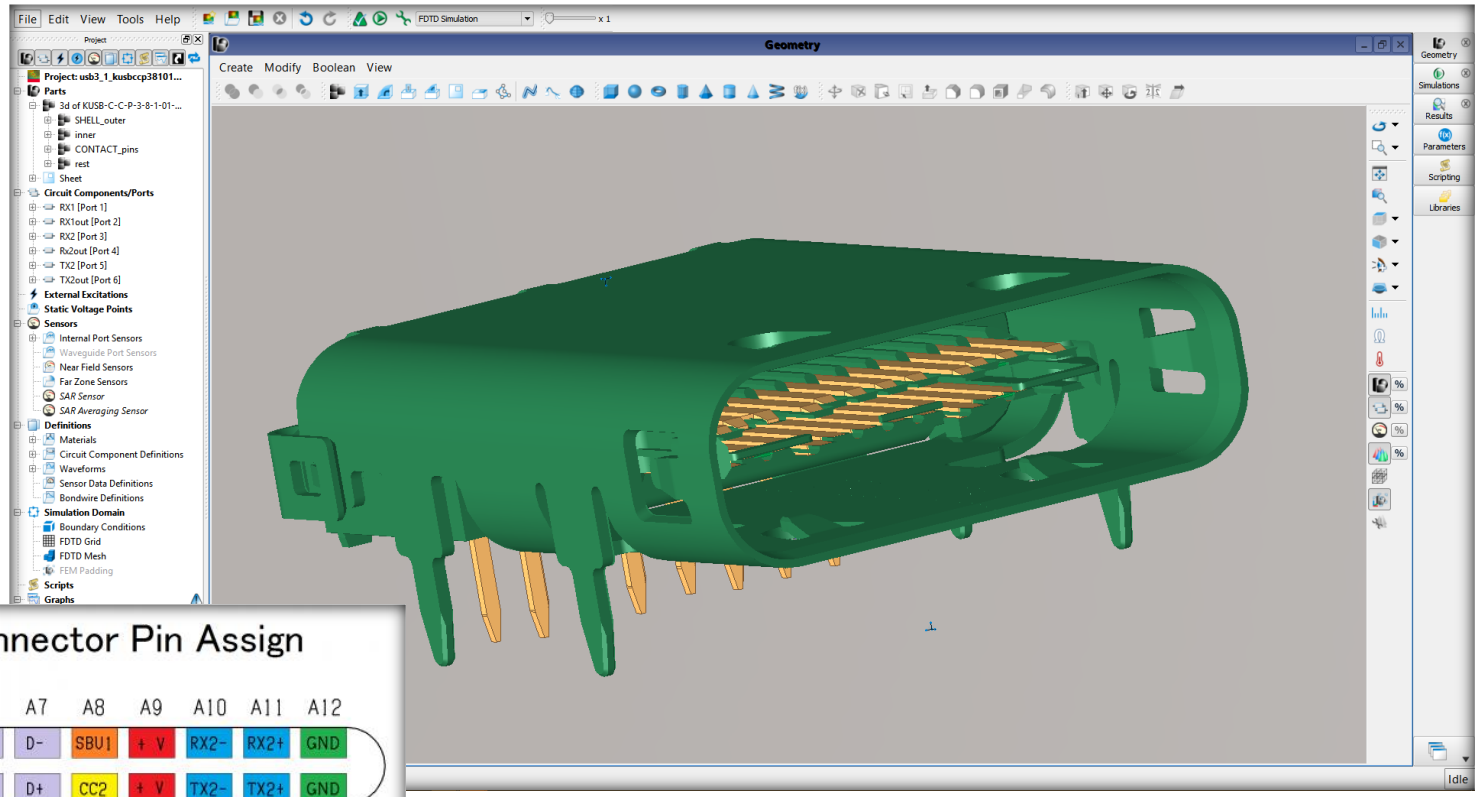


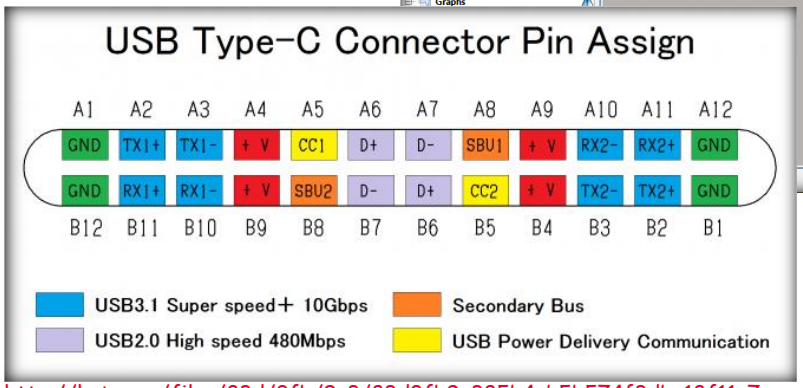


Level1	155.0 m	187.7 m
Level0	-152.5 m	-185.0 m
Height	96.00 m	166.0 m
Width	58.00 p	64.50 p
JitterPP	42.00 p	35.50 p

3DEM Simulation - EMPro FEM/FDTD

USB Type-C Connector 3DEM Simulation





http://hsto.org/files/83d/0fb/9a3/83d0fb9a385b4ab5b574f3dba18f11a7.png

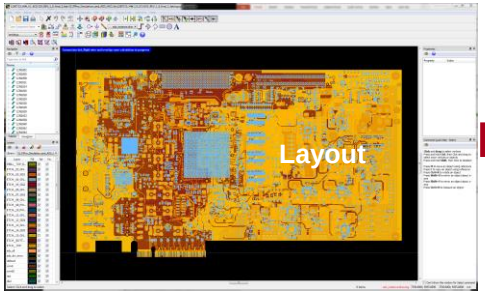
Post-Layout Simulation using PIPro/SIPro in ADS

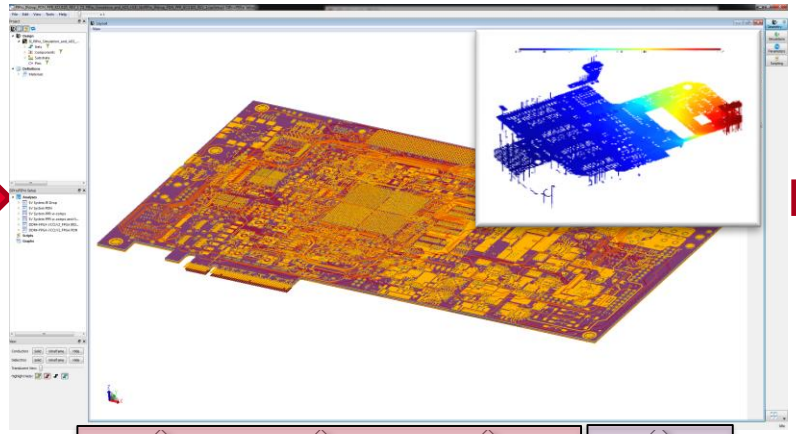
A Cohesive workflow for SI and PI

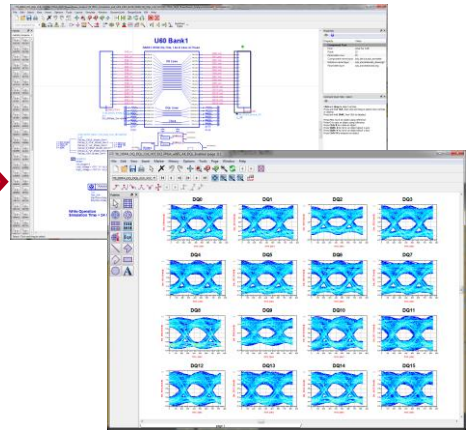
Layout Import into ADS
(Direct *.brd Import, Allegro ADFI or ODB++ flow)

SIPro / PIPro
PCB Characterization and Model Extraction

Signal/Power Integrity Analysis
(Transient Convolution, Channel Sim, DDR Bus Sim)







4 New EM Simulators

PIPro

IR Drop

PDN Z-imp

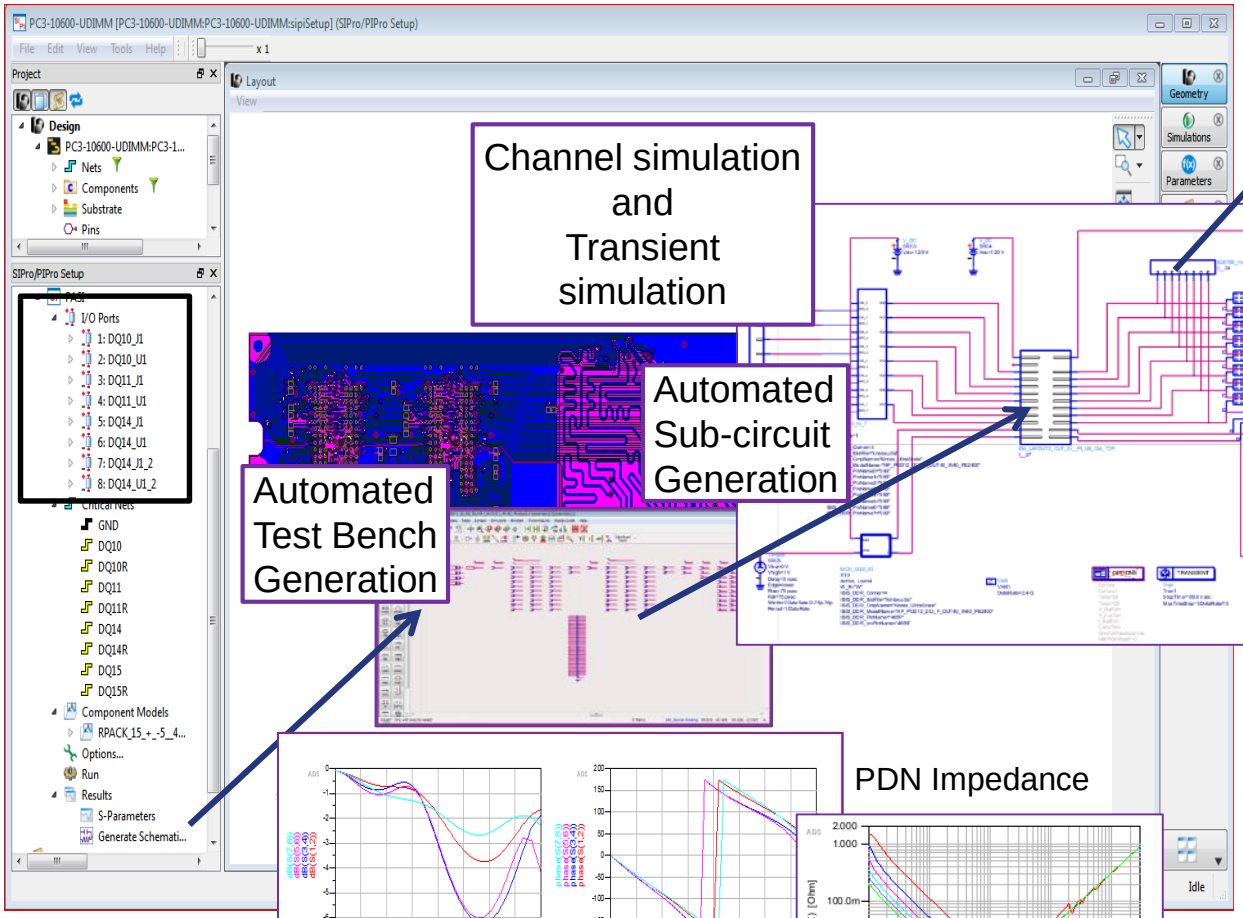
Power Plane Resonances

Power Aware SI

SIPro

Post-Layout Simulation using PIPro/SIPro in ADS

Seamless flow from EM-analyses back into schematic for both SI and PI



I/O ports

Channel simulation and Transient simulation

Automated Sub-circuit Generation

Automated Test Bench Generation

Decap Tuning, Optimization, Circuit-level VRM modeling

SSN Analysis

Data with VCC Bounce

DDR4 Low BER Simulation

And More Simulation!

Compliance Test

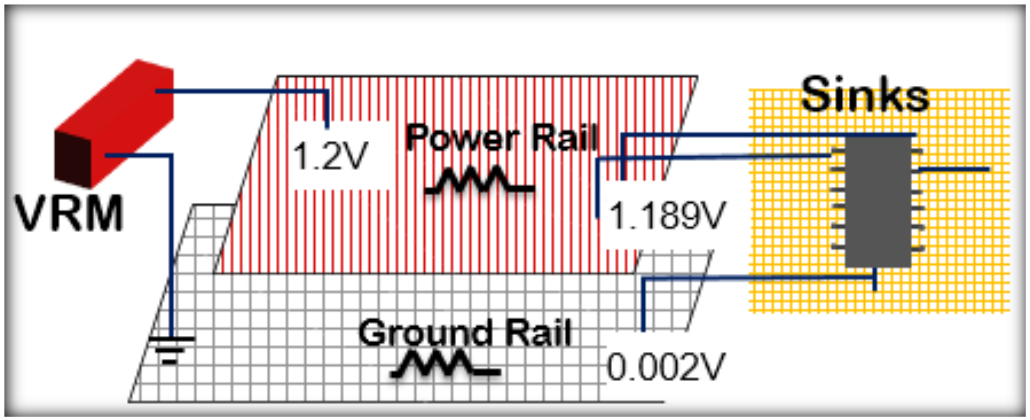
PDN Impedance

S-parameter Extraction

Why, Power Integrity Analysis

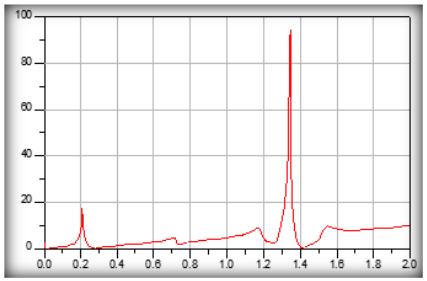
IR Drop

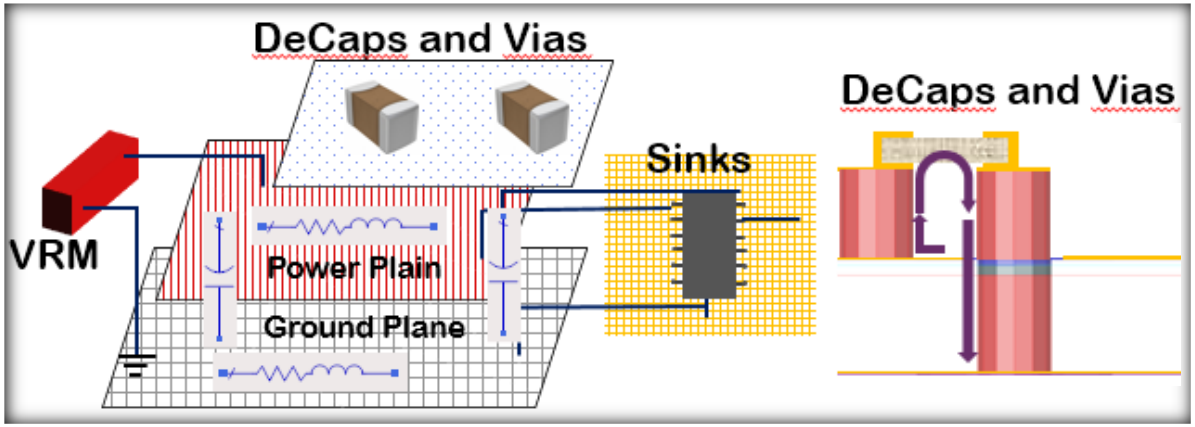
$\Delta V = IR_{near}$ *"IR Drop"*



PDN Impedance "Ripple" Optimization

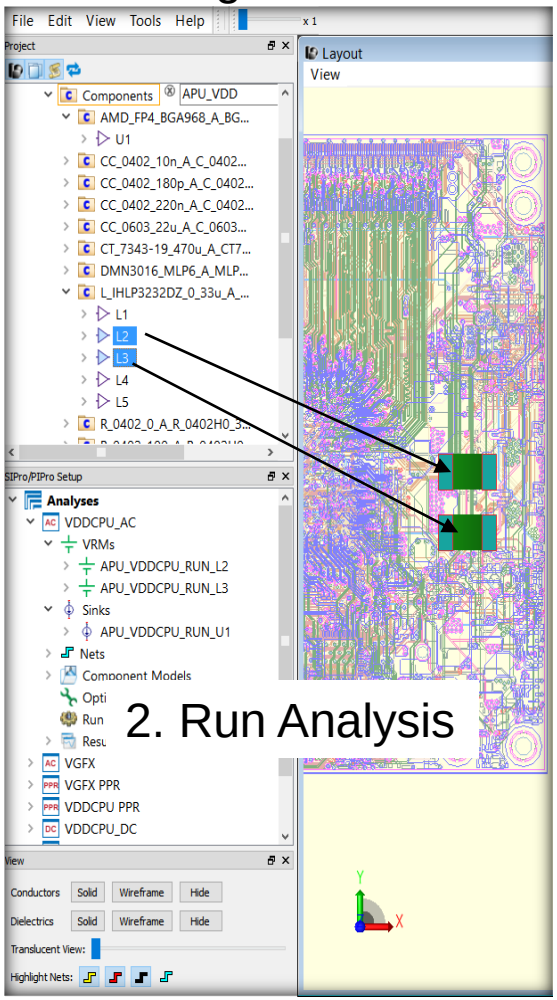
$V_{ripple} = L\ dI/dt$





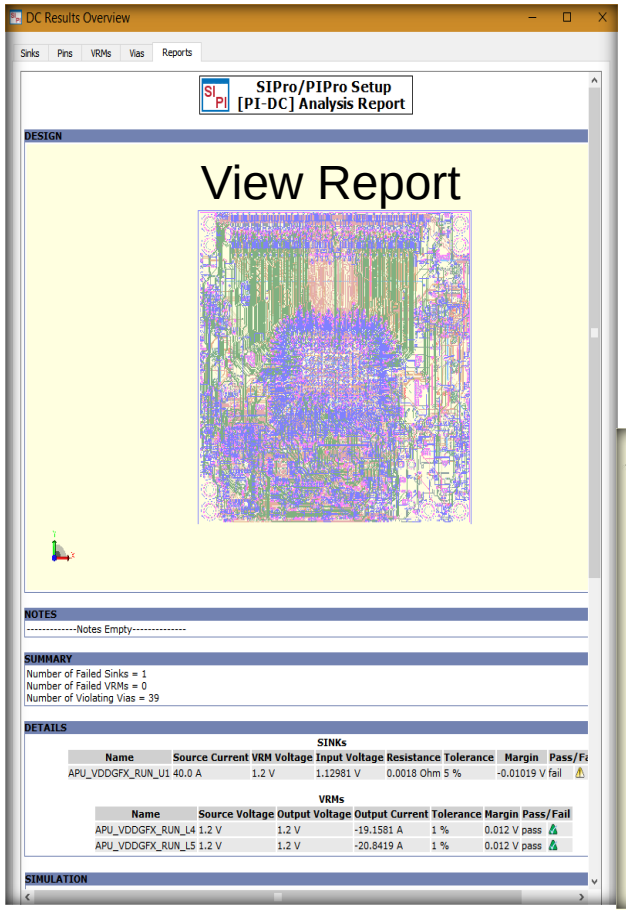
Static IR Drop Analysis in the PDN –DC Analysis

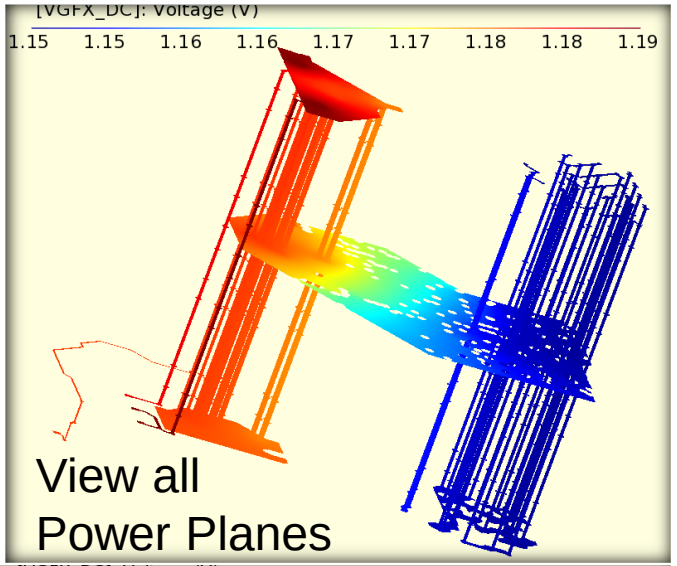
1. Add VRMs, Sinks and configure

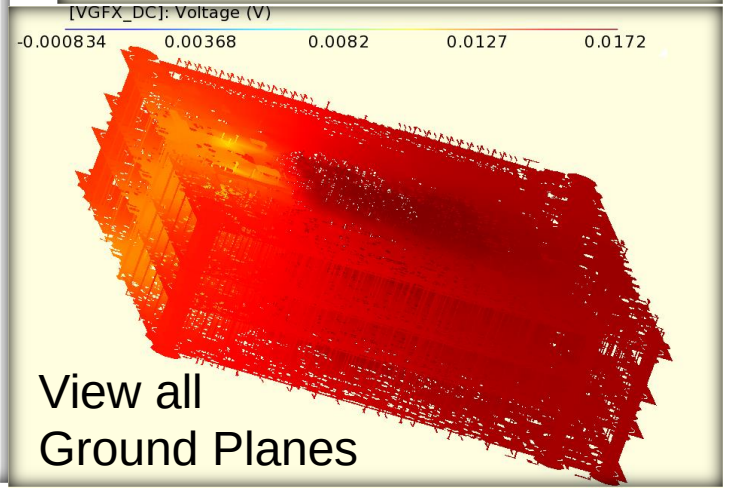


2. Run Analysis

- Run a PI-DC analysis
- View analysis results and report





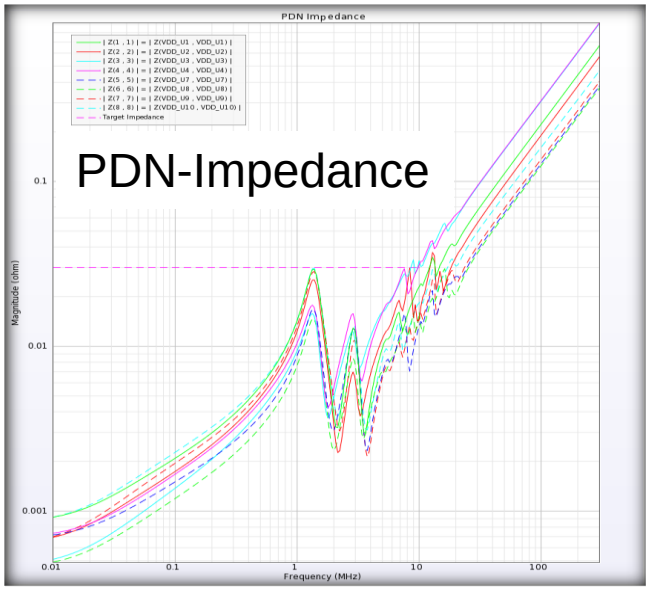


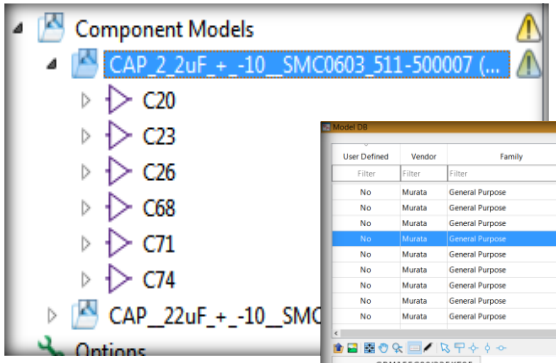
KEYSIGHT TECHNOLOGIES

AC-PDN Impedance Analysis

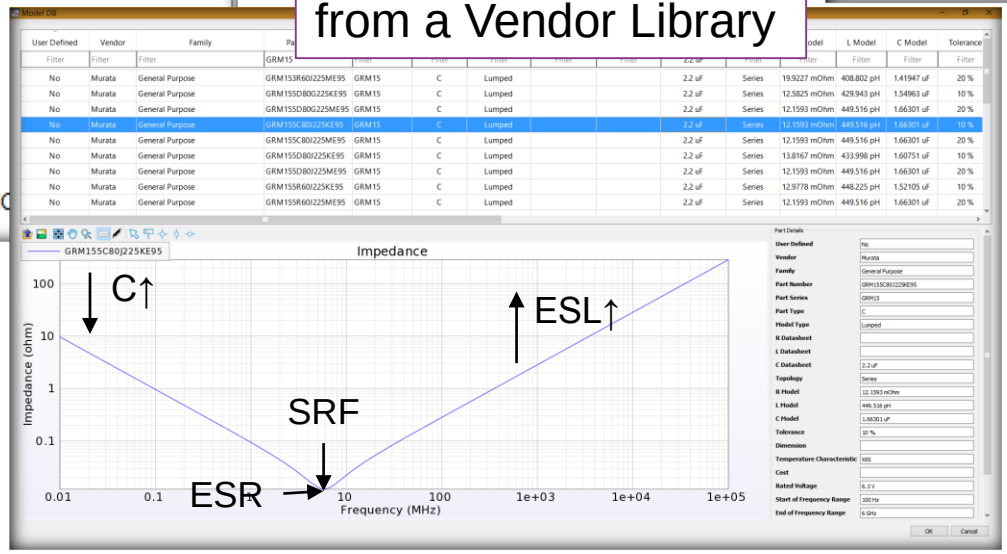
Minimize the PDN-Impedance

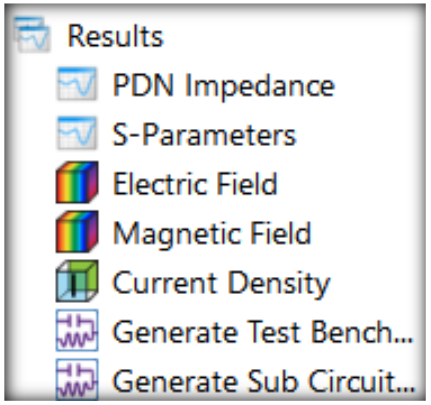
- Reuse the DC-Setup
- Add Cap's
  - Run a PI-AC analysis
  - View analysis results





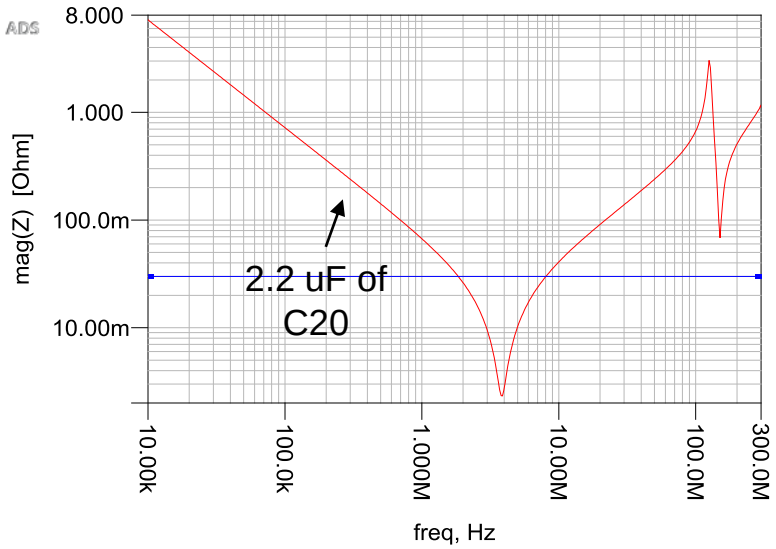
Choose Capacitors from a Vendor Library



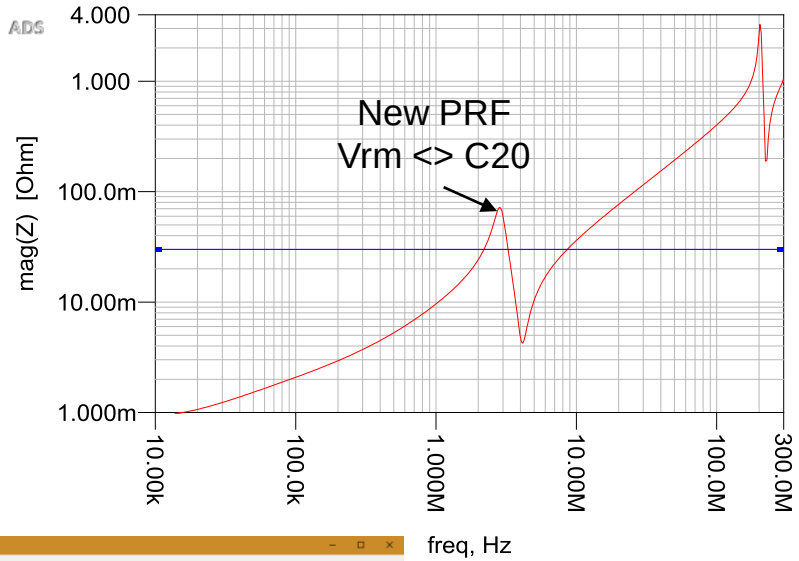


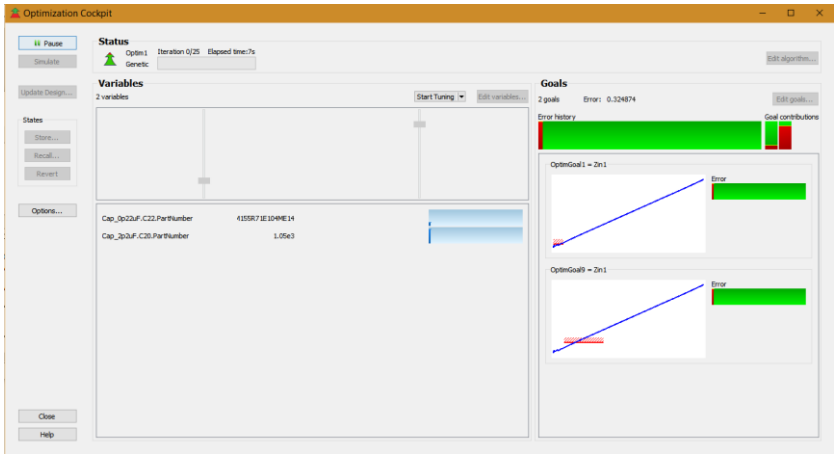
Decap Optimization

C20 Decap, VRM Open



C20 Decap, VRM Closed



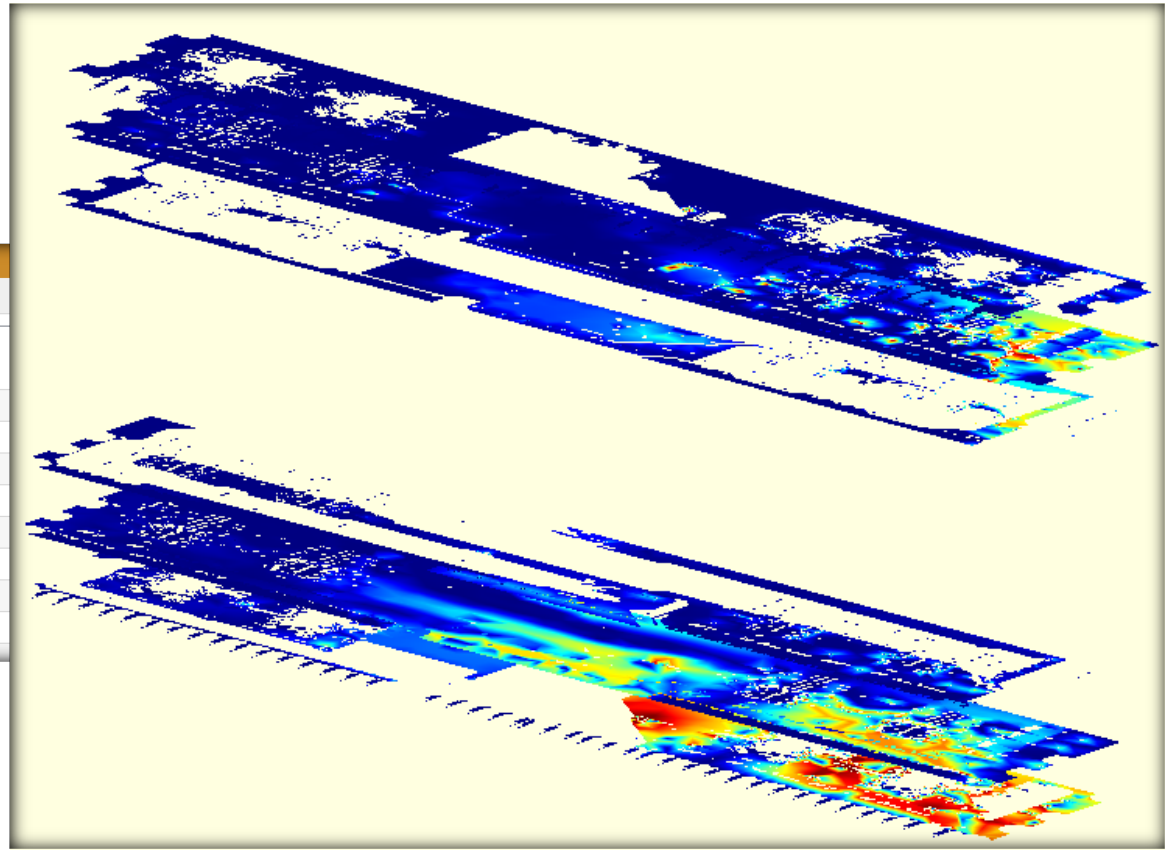


Optimization Cockpit
Statistical Analysis
Sensitivity Analysis
DOE

Power Plane Resonance Analysis

Fast Way to find Hot Spots

Visualizing Hot spots at any Eigenfrequency



Eigenfrequency

PPR Results Overview

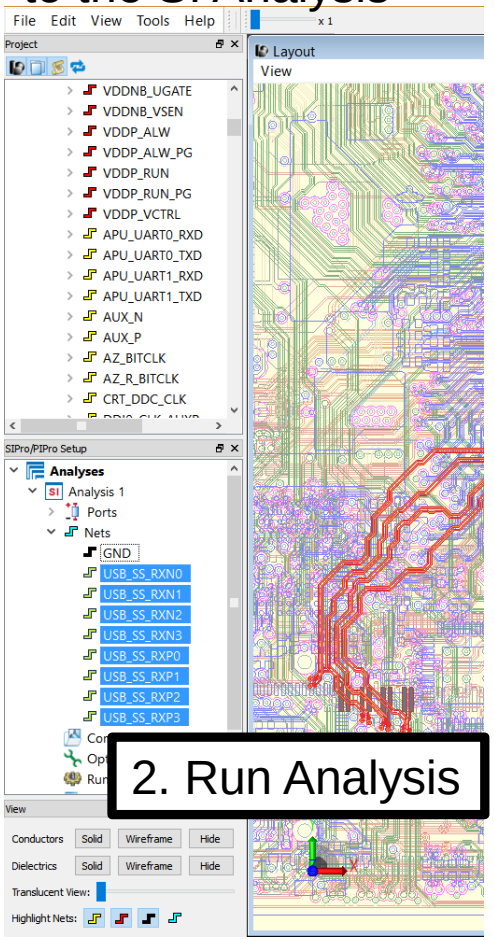
Frequencies

	Eigenfrequency [MHz]	Q Value
1	2.77146	5.28995
2	5.39259	7.76259
3	5.96129	8.92676
4	6.81856	9.78677
5	7.64796	10.1772
6	7.64797	10.1773
7	8.76805	21.8558
8	9.4501	19.9252
9	9.76944	19.3142
10	9.76945	19.3141

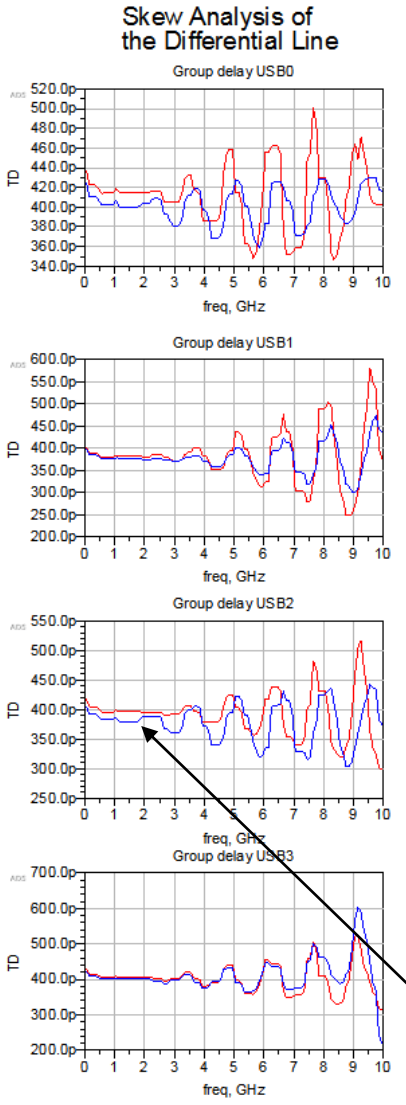
Correlation with AC analysis

SI Analysis

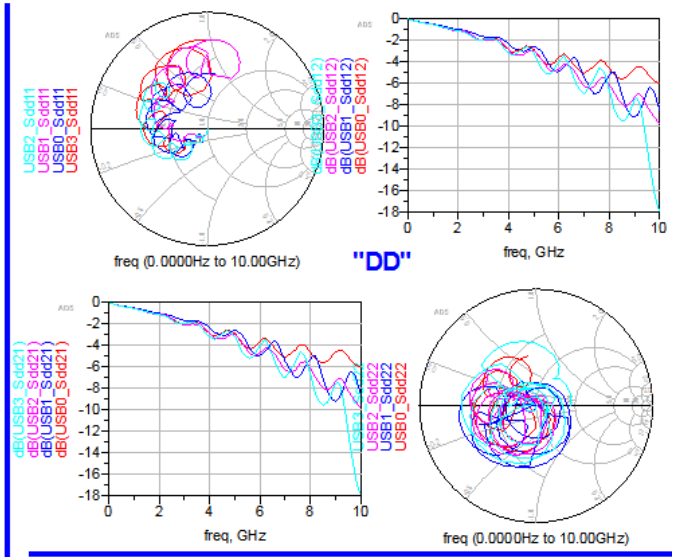
1. Drag and drop the Signal and GND nets to the SI Analysis



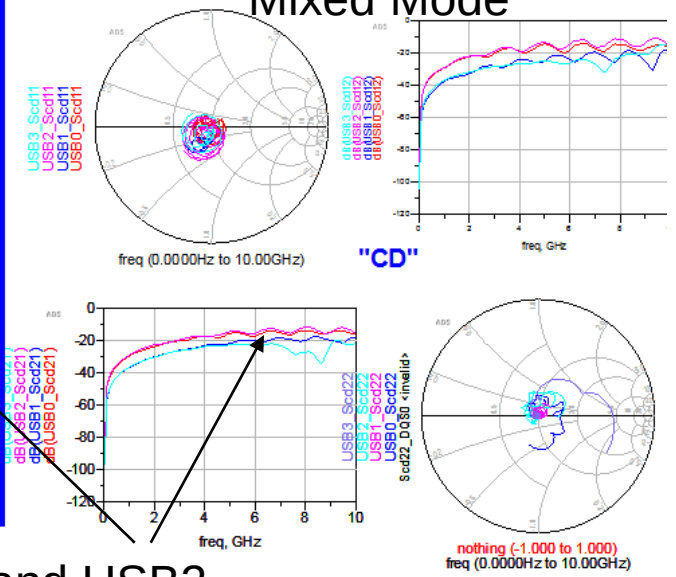
2. Run Analysis



Differential-2-Differential



Mixed Mode



Asymmetry in USB0 and USB2 cause a higher Mode Conversion

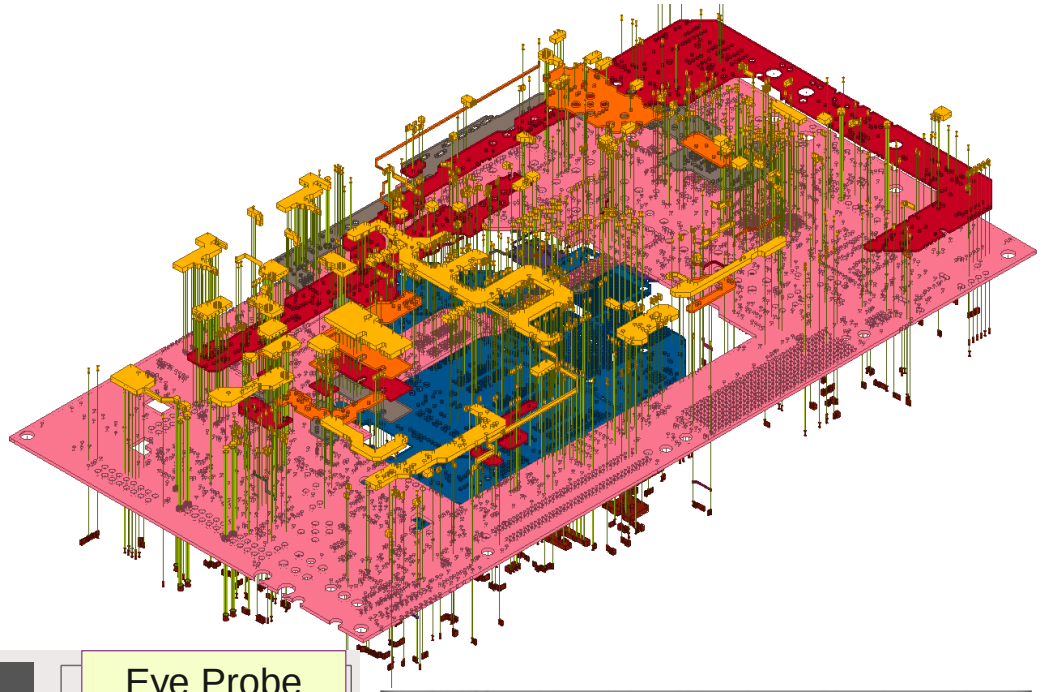
KEYSIGHT TECHNOLOGIES

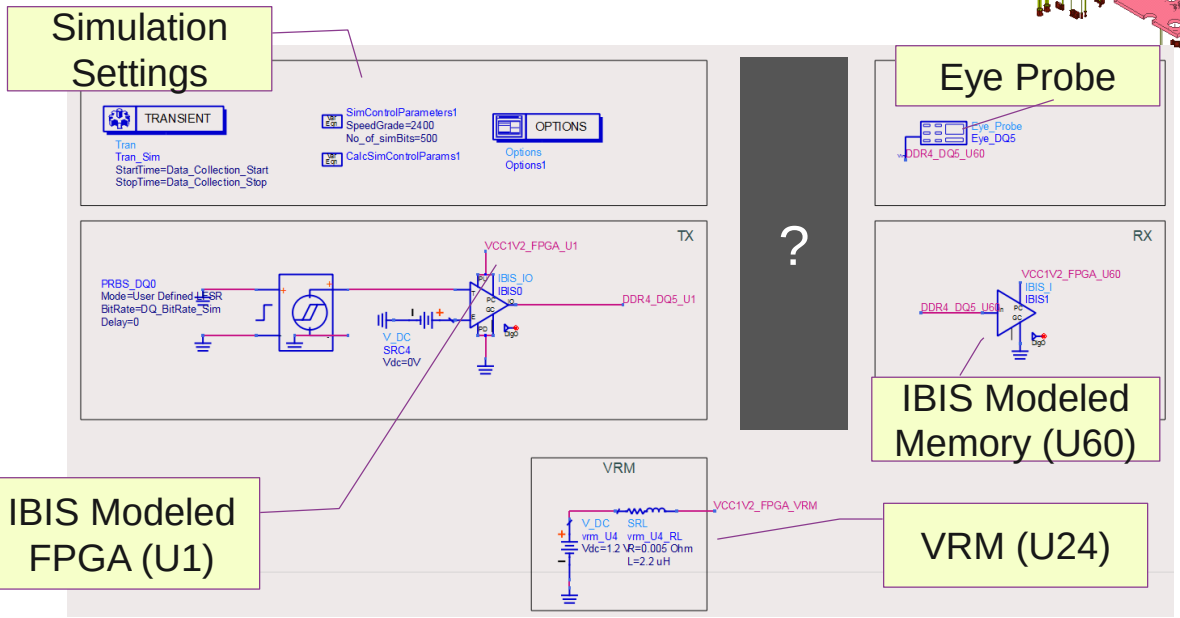
Power Aware SI

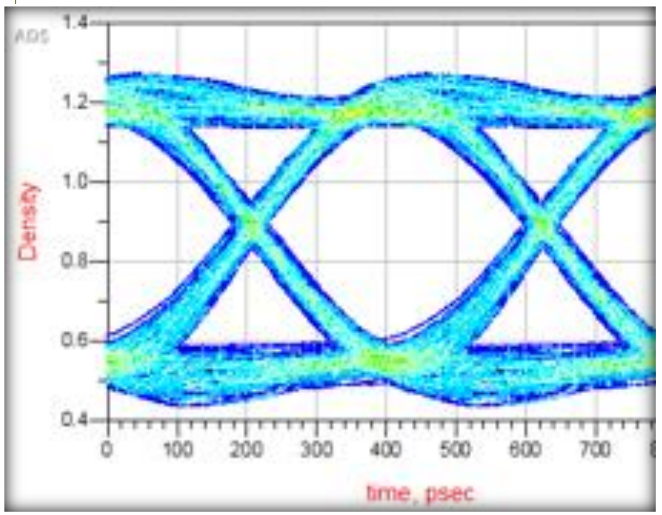
Combined SI-PI Analysis

Setup

1. Extract Model in SIPro
2. Combine IBIS-Model and extracted Model in Schematic



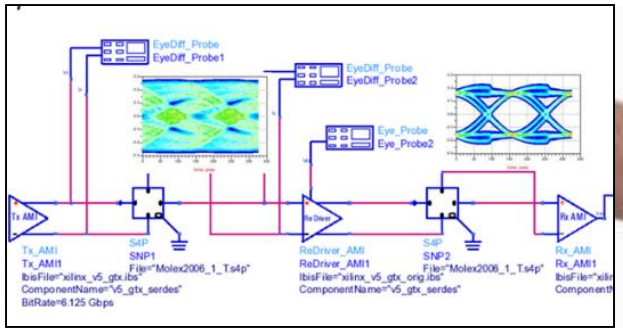


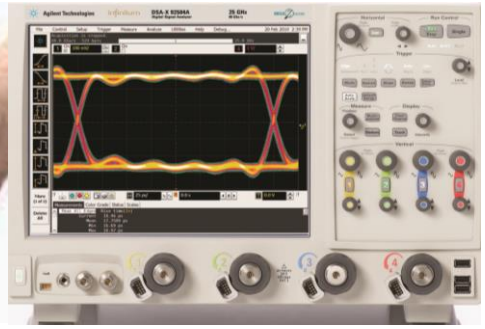


Compliance Test

Using Simulated Signal in Scope Software Infiniium Offline

Design Software meets Measurement



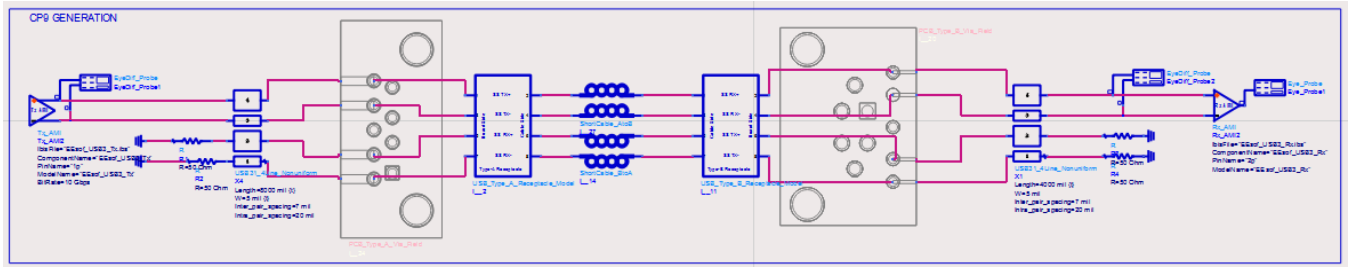


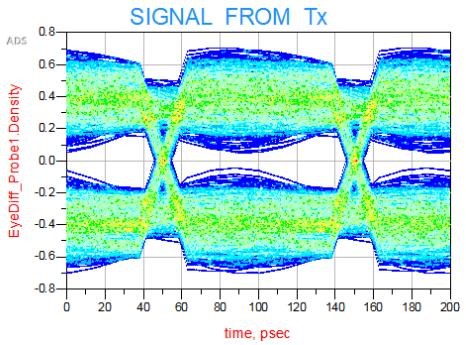
Compliance Test from Simulation including EM-Models

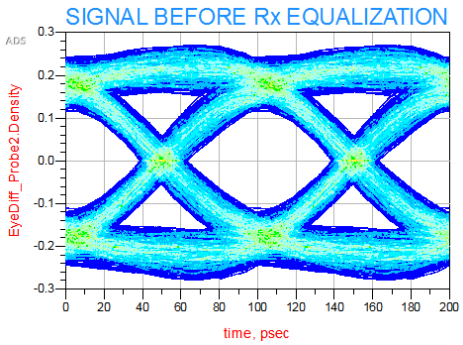
Simulated Signal is used in the Infiniium Offline+USB-Compliance App

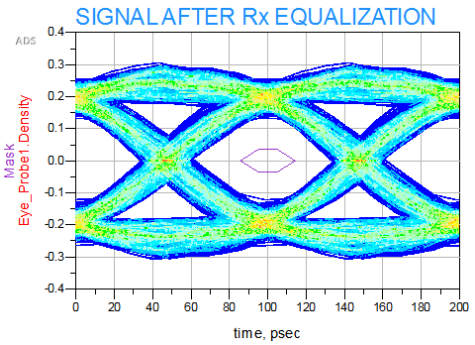
- USB 3.1 Design Guide in ADS includes a wide range of Simulation Models and a set of Full link Tx/Rx Channel Simulation setups, including IBIS-AMI-Model to run Compliance Tests

- The simulated signal is stored in a format which Infiniium can read

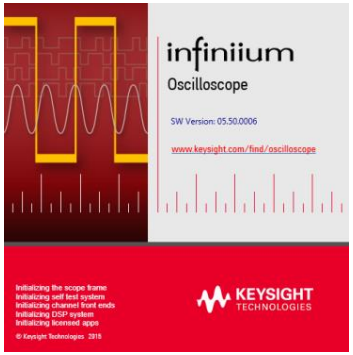






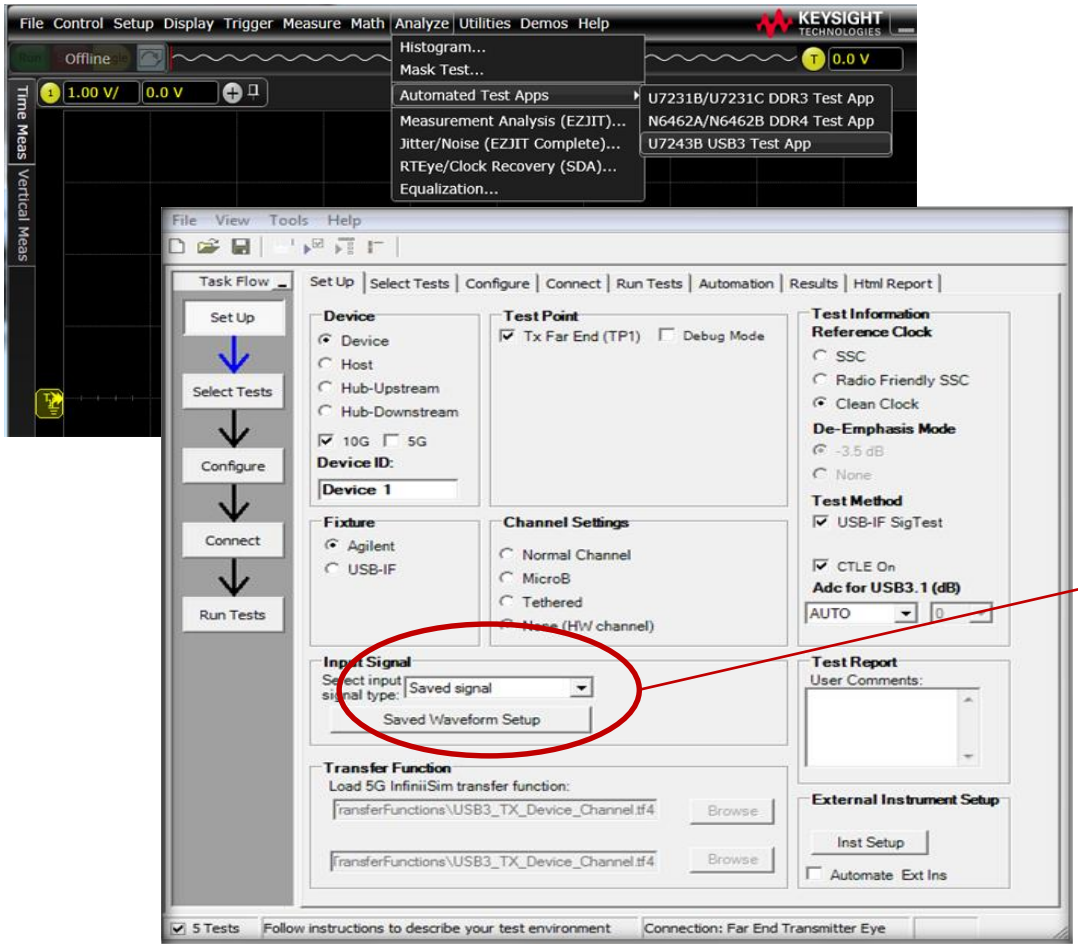


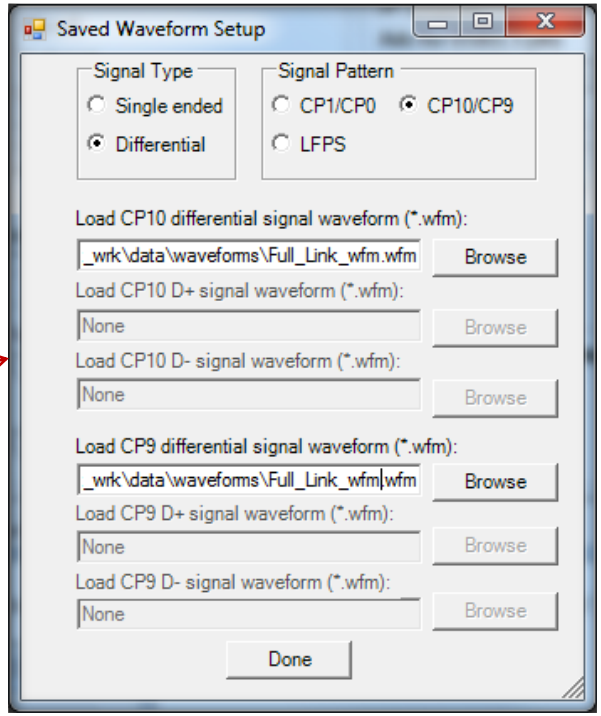
Infiniium Scope Offline Software



USB 3.1 CTB: PHY Simulation to Compliance

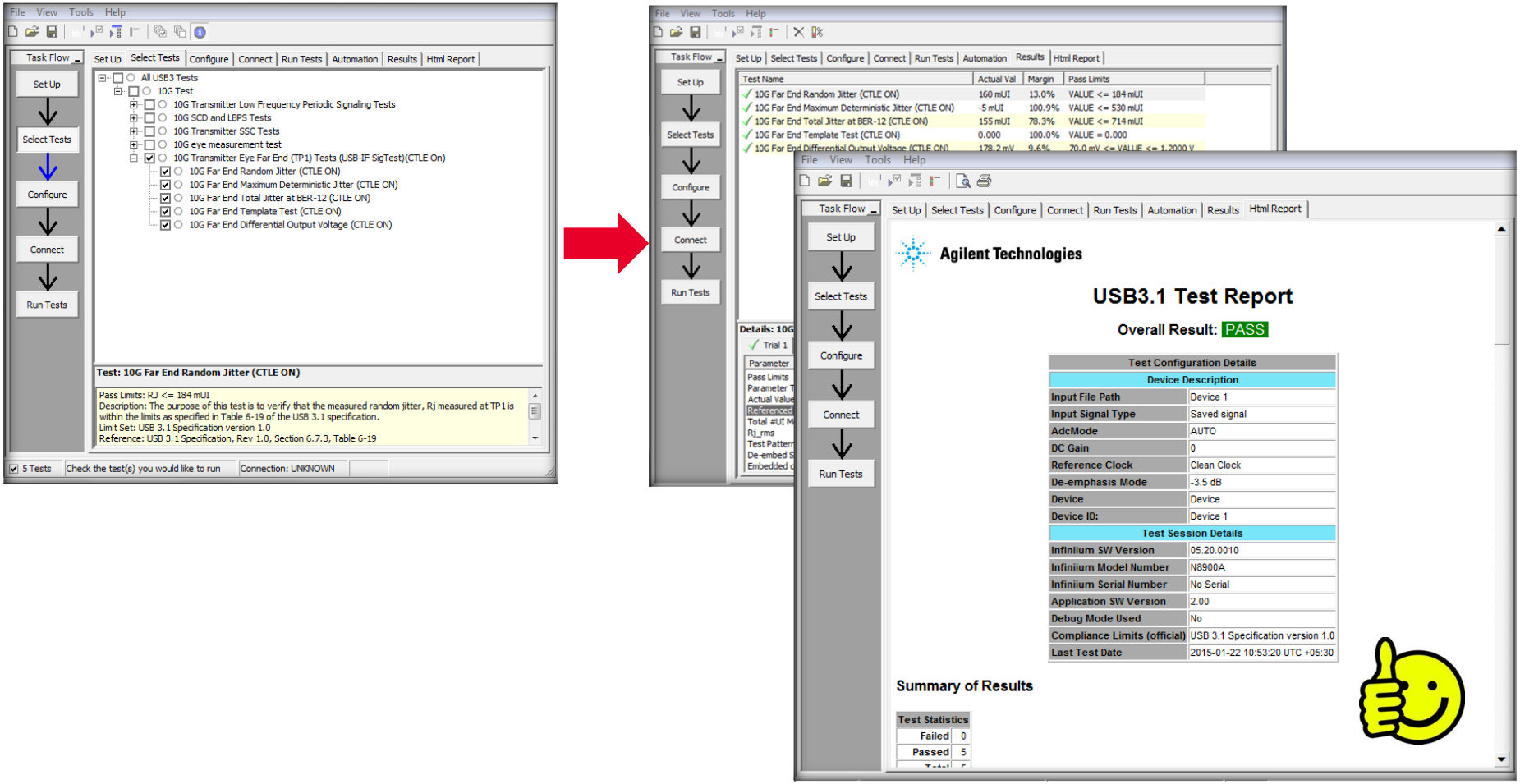
Infiniium Offline and USB app on your PC





USB 3.1 CTB: PHY Simulation to Compliance

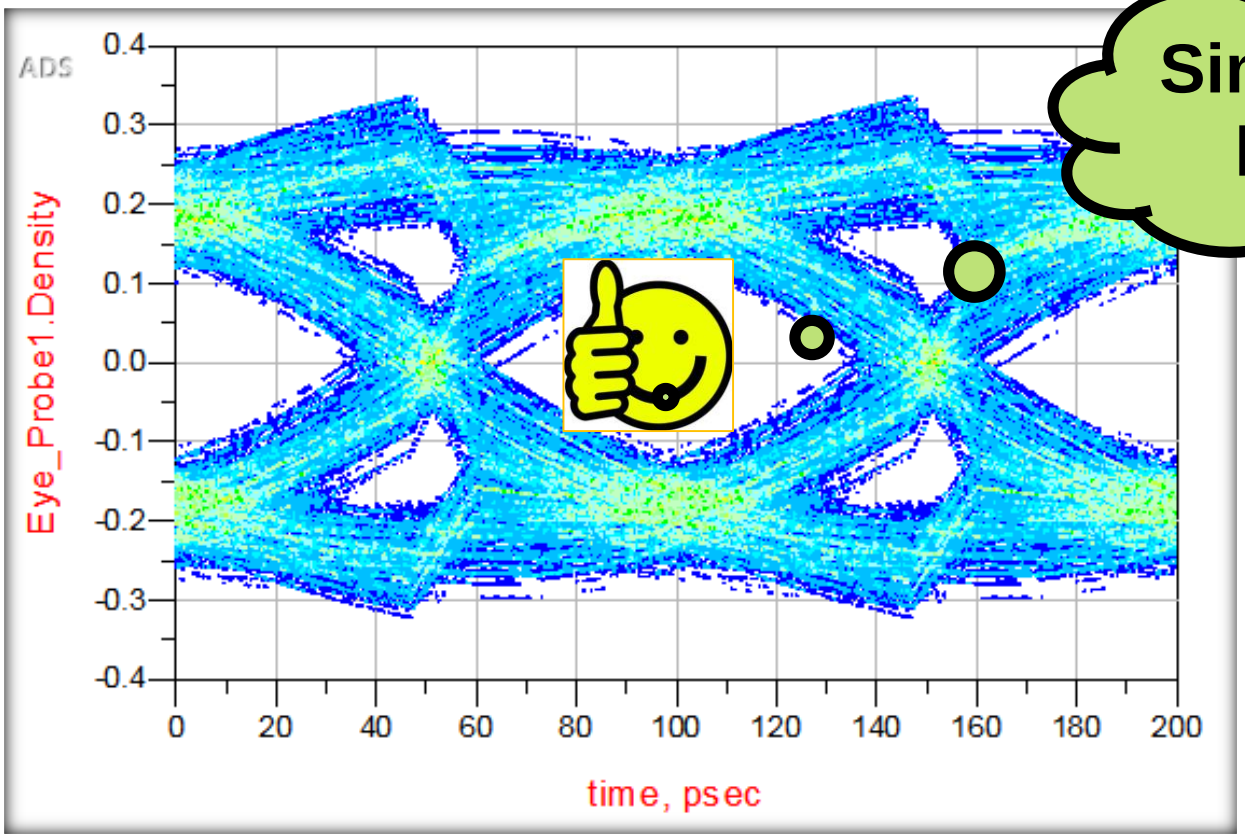
Run compliance tests and view results



Summary

- Could I motivate you to use Simulation?
- Illustrated an example of a Super Speed USB Design and Simulation Techniques
- Pre-Layout Study and Analysis
- Channel Modeling, Simulation and Optimization
- Post-Layout Analysis
  - IR-Drop-, PDN-Impedance-, Power Plane Resonance- and Power Aware SI Analysis
- Compliance Test, Design Guides and Utilities

Thank you for your attendance!
Questions?



Simulation helps!