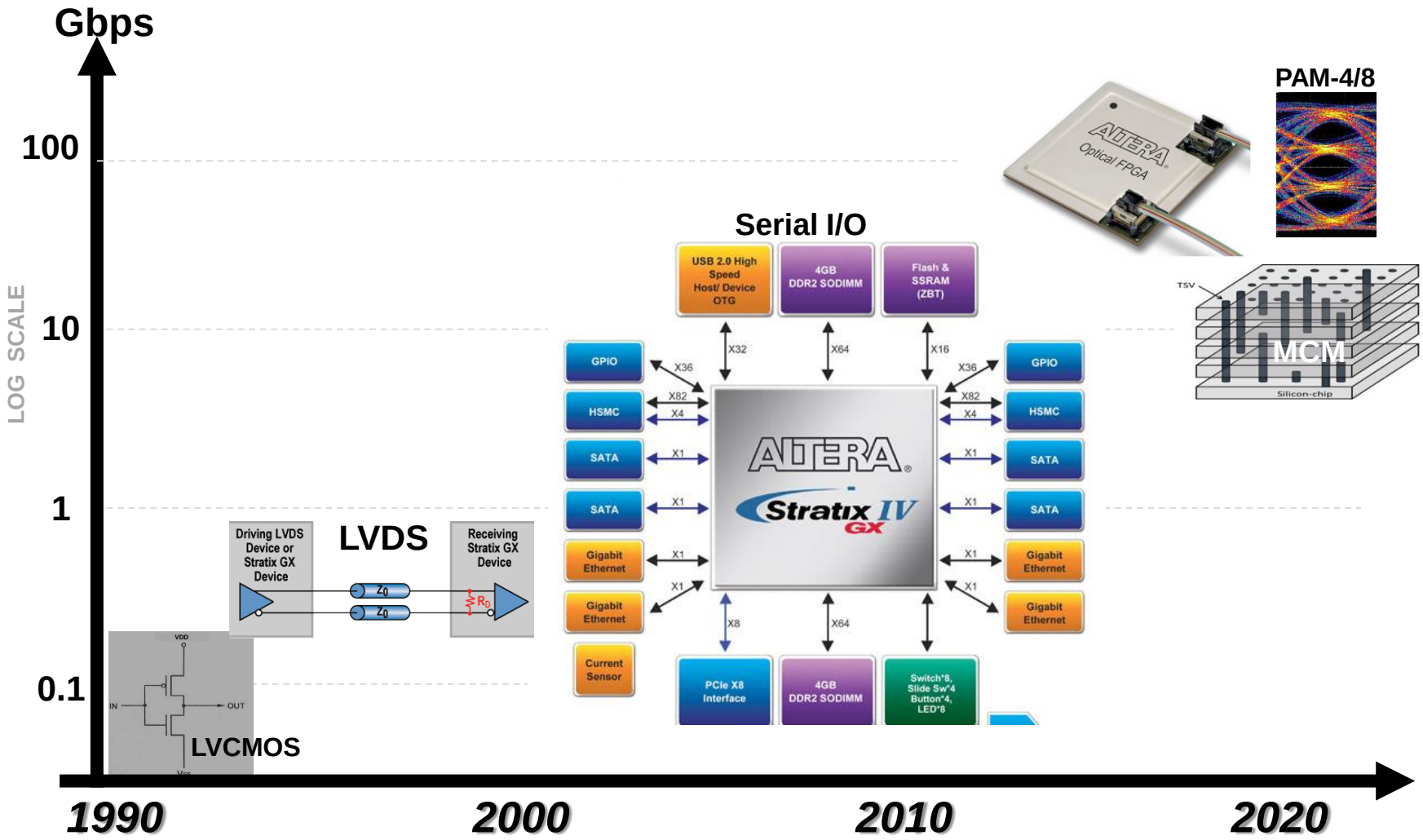
BluePrint Platform Designer

I/O evolution



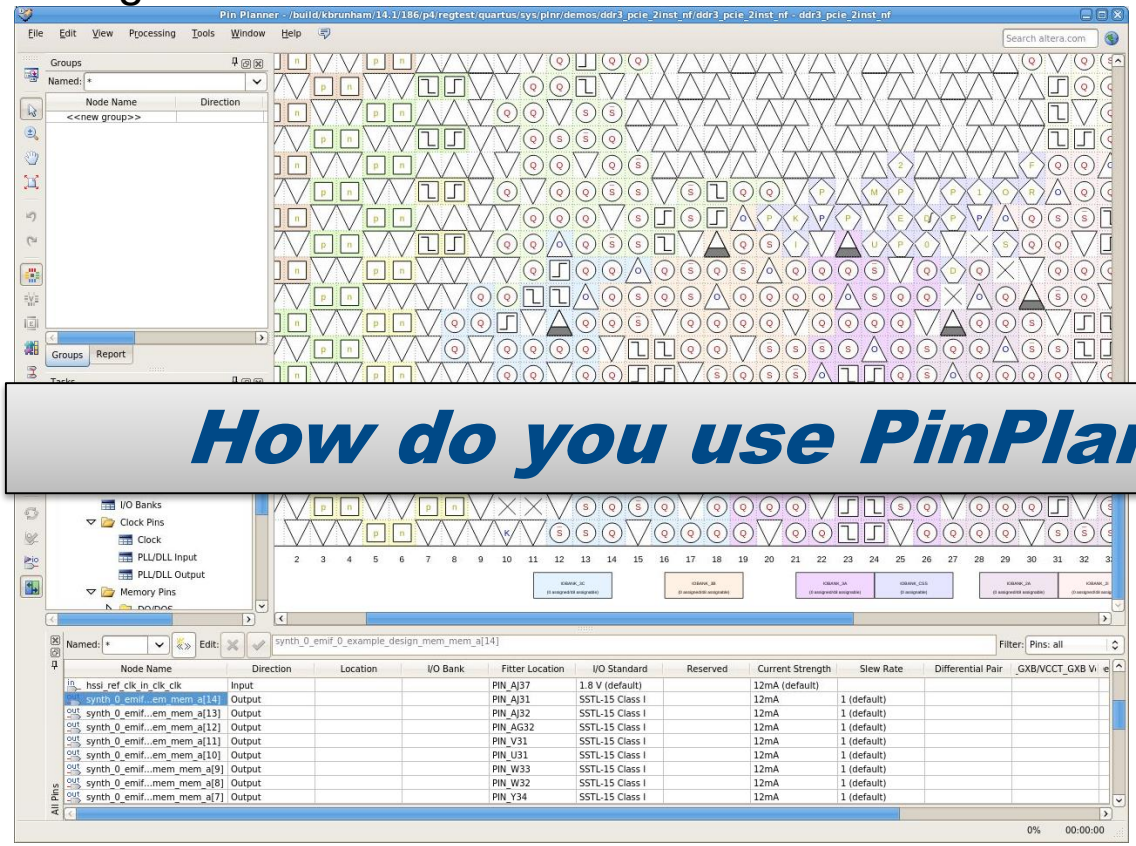
Floorplanning…Floorplanning…Floorplanning…

- Floorplanning is hard to do…
- Floorplanning makes my timing closure worse…
- Floorplanning does not do what I expected…

Shouldn't floorplanning be easy and intuitive?

Creating I/O assignments using the PinPlanner

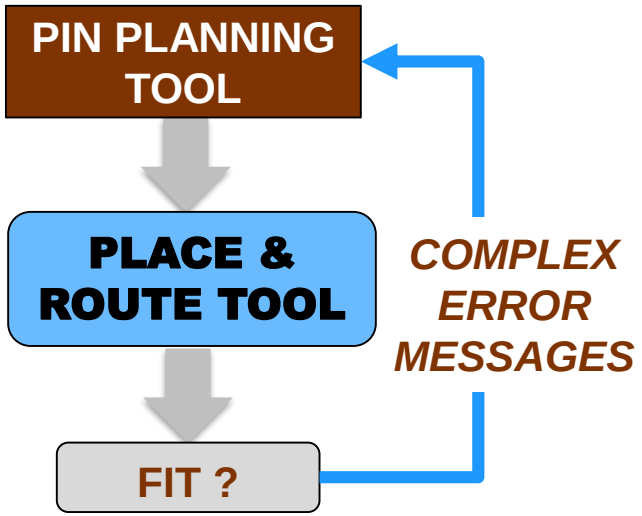
- Traditionally the location for I/O elements can be done using the PinPlanner or Assignment Editor
  - These tools allow the creation of syntactically correct IO and location assignments



How do you use PinPlanner?

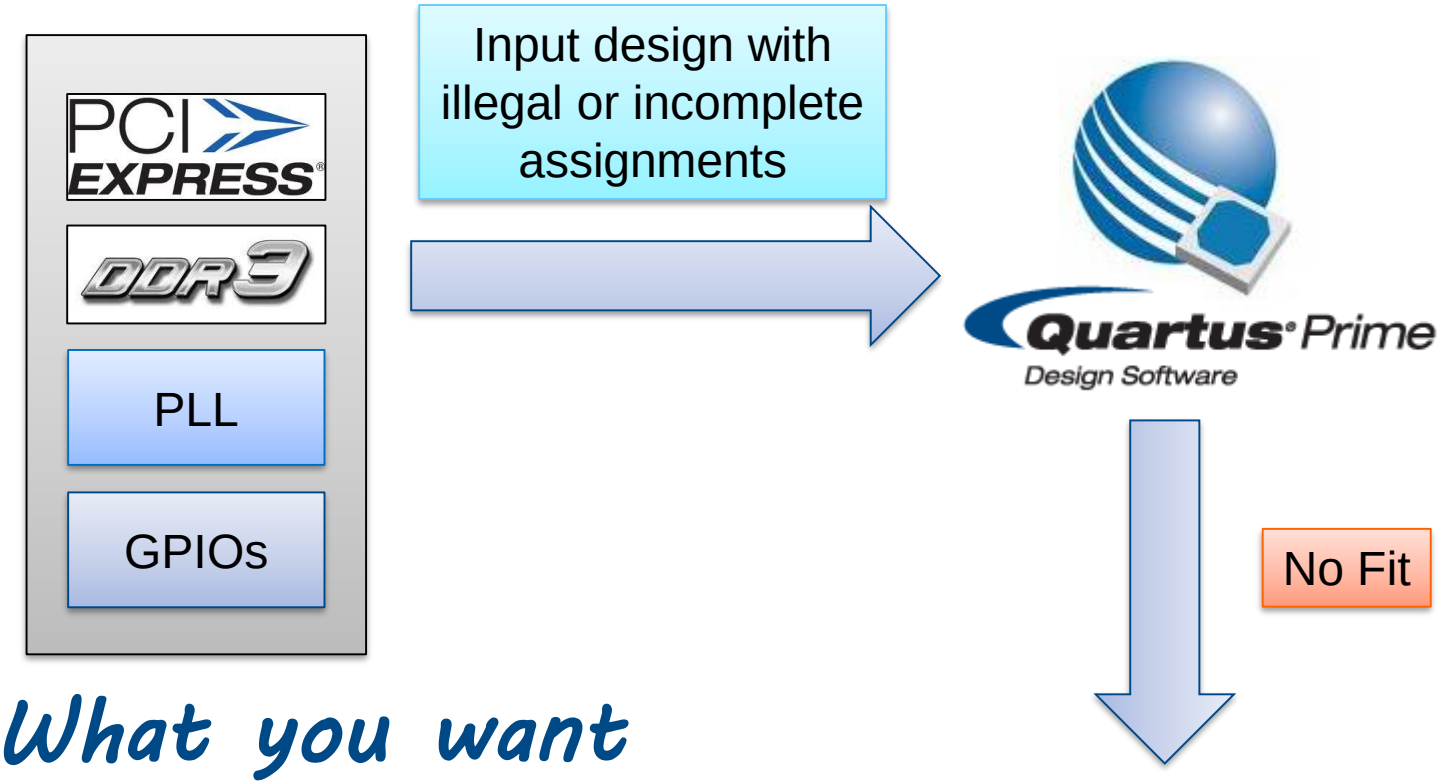
Current I/O Interface Placement Flow

- Current FPGA pin planners can assign locations, but cannot
  - Auto place pins
  - Accurately evaluate placement legality
  - Does not use the Fitter place and route engine
  - Report alternative placement to improve performance and resources
- **Multiple, long iterations to resolve complex error messages**



Note: FPGA tool = QUARTUS, VIVADO etc.,

Problem: FPGA Placement is Complex



What you want

```
Error (175022): The auto-promoted clock driver could not be placed in an
y location to satisfy its connectivity requirements
```

Today, you need an expert on I/O Interface IP

IP Core Requirements

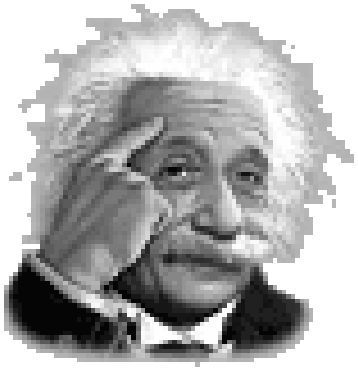
Interface Specification

PCI EXPRESS®

DDR3/4

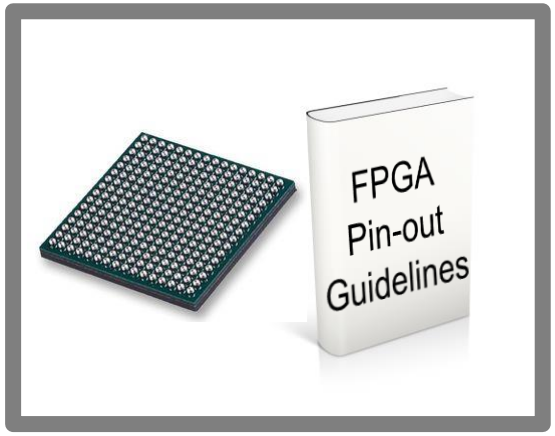
Ethernet

Interlaken



Albert Einstein

FPGA Specification

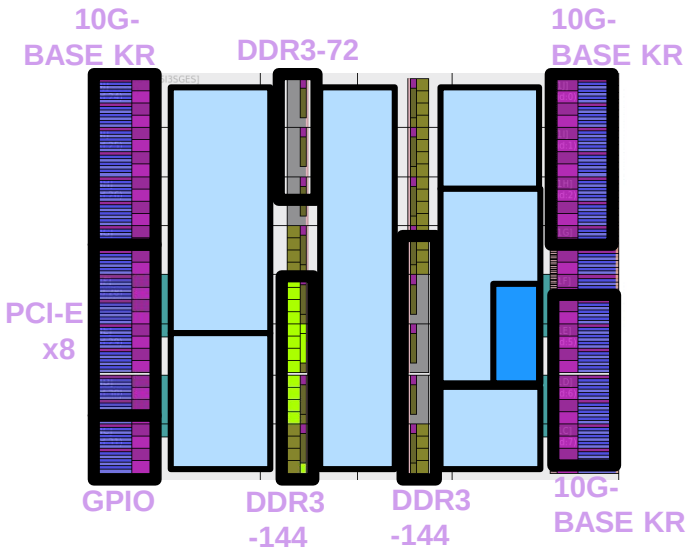


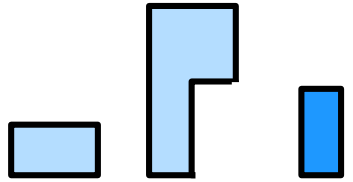
ALTERA

Let us re-capture the challenges

- Don’t want to read tons of documents or debug of complex error messages
  - Instead, need legal & instantaneous I/O placement on package or chip floorplan
- Can we also avoid other legality issues such as clocks and floor-planning ?
  - Assign clock domains in FPGA fabric
  - Check quick fit of logic block partitions

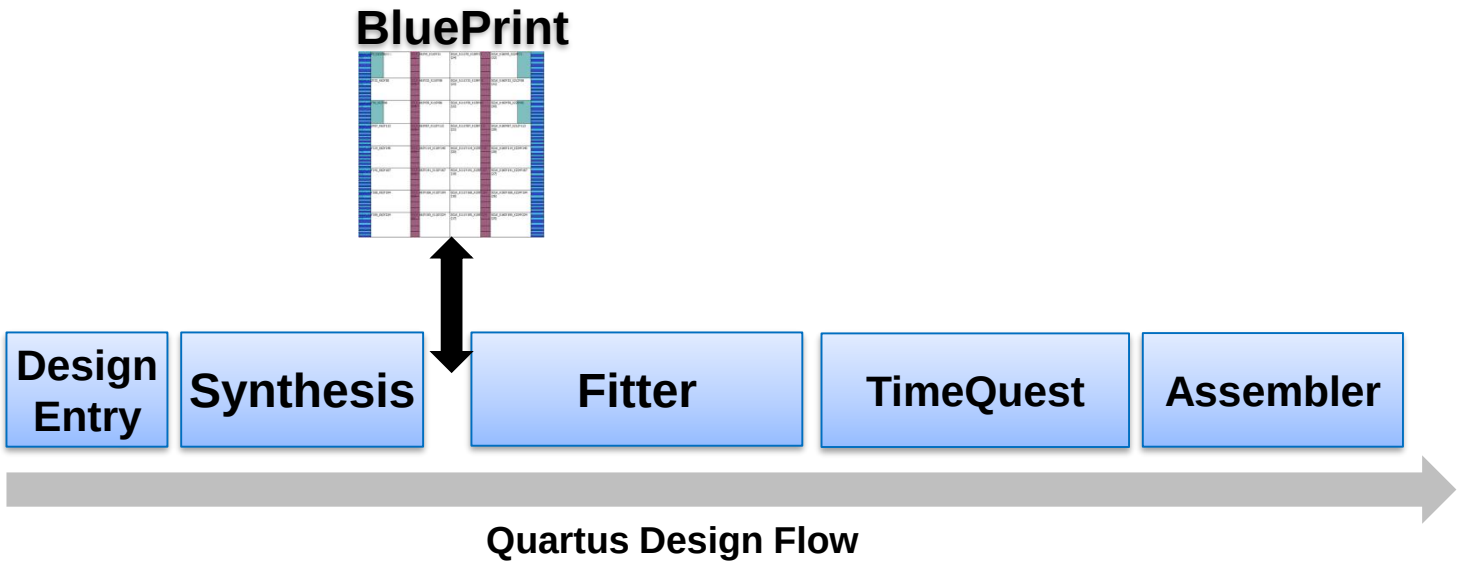
Chip View





Clock / Logic regions

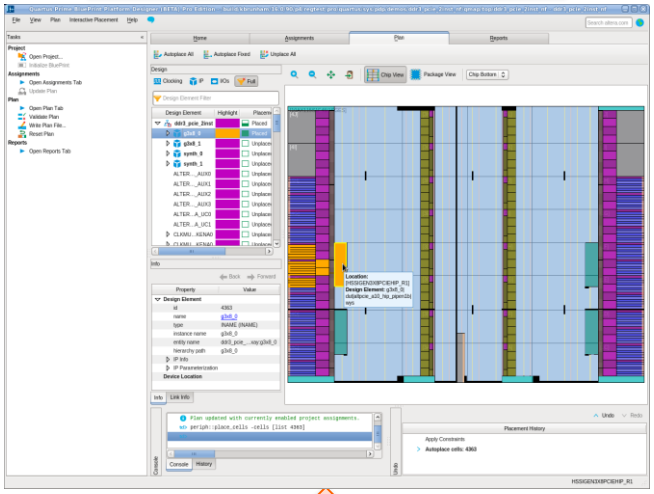
BluePrint Flow



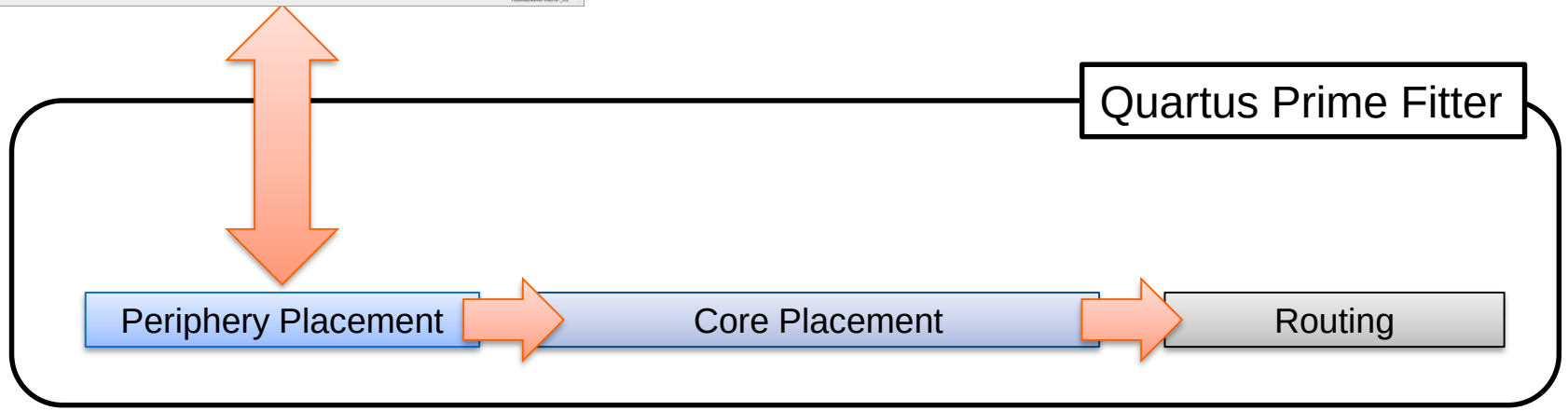
- Synthesize design
  - Create a skeletal system in Qsys, Megawizard or any other design entry method
  - Fabric logic doesn't have to be complete
- Drag & drop I/O interface at top-level onto package, or chip floorplan
  - Optionally, assign core clock domains
- Create a BluePrint in minutes (output Quartus assignment file)

BluePrint: Create legal assignments using the power of the Fitter

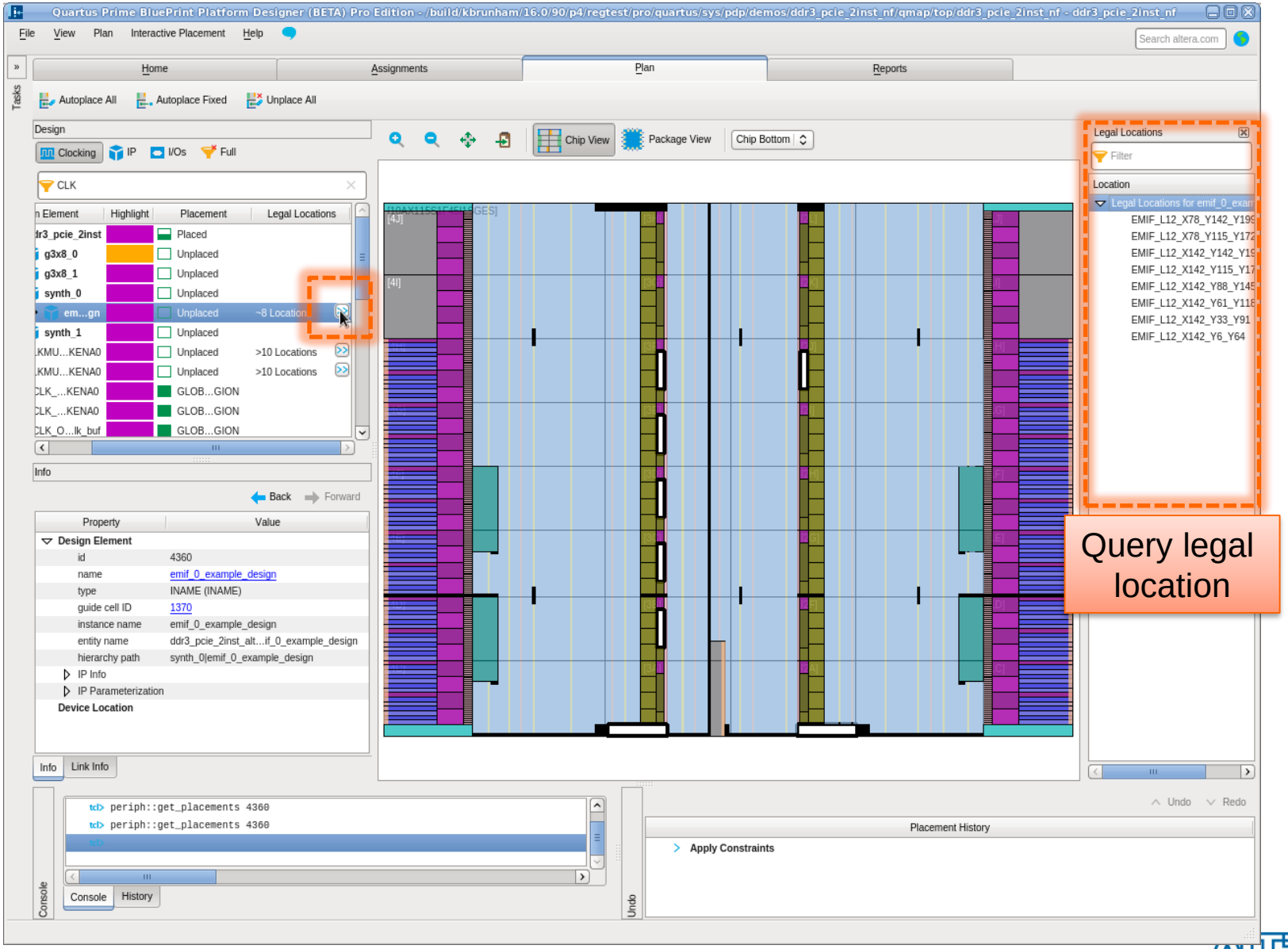
BluePrint Platform Designer



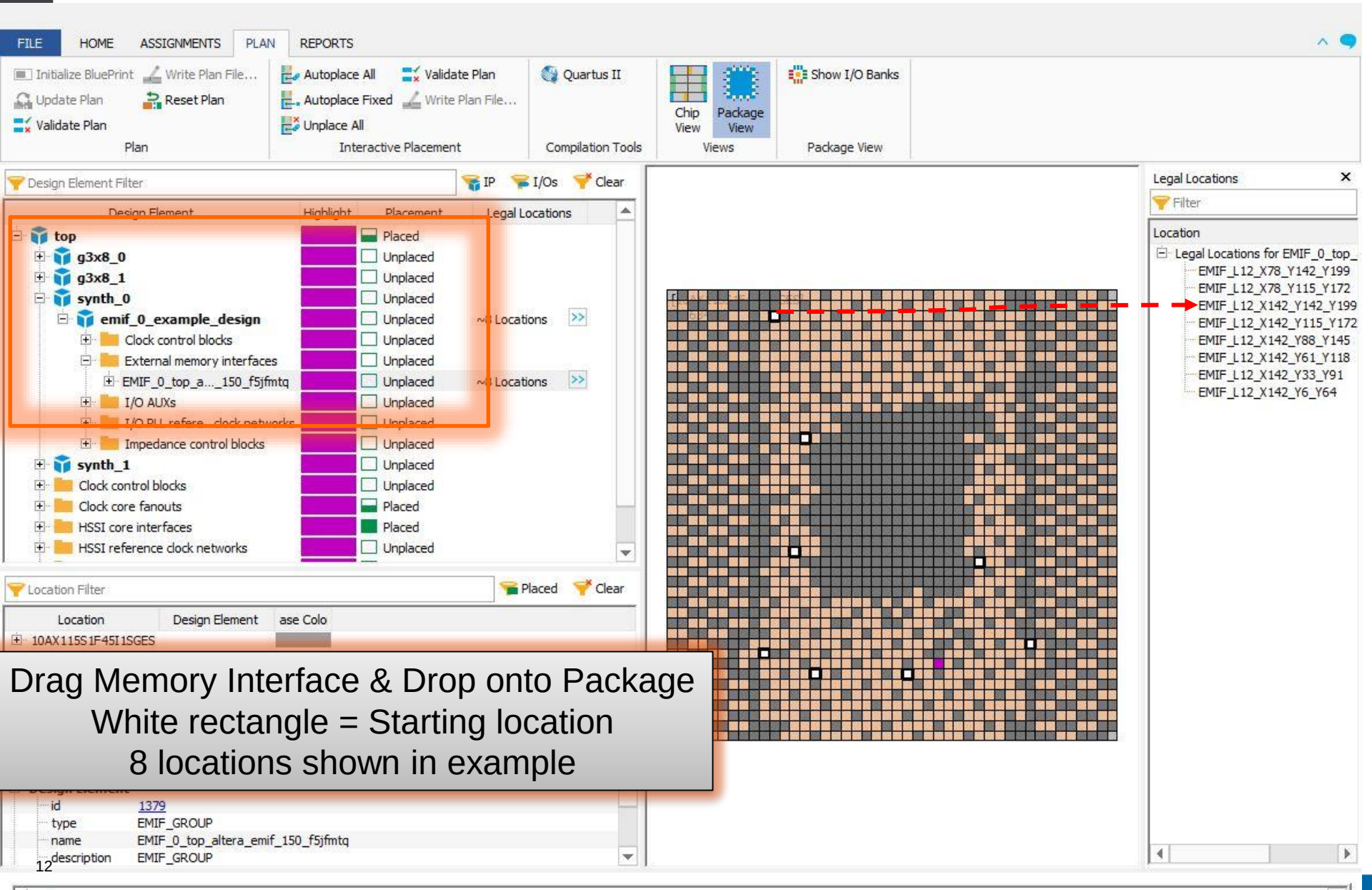
- BluePrint operates live with the Quartus Prime Fitter
- Legality reported in BluePrint comes from the Quartus Prime Fitter
- Different floorplanning scenarios can be evaluated using BluePrint
- Constraints generated from BluePrint can be used in a subsequent compile



BluePrint: Place whole interfaces using “drag-and-drop”

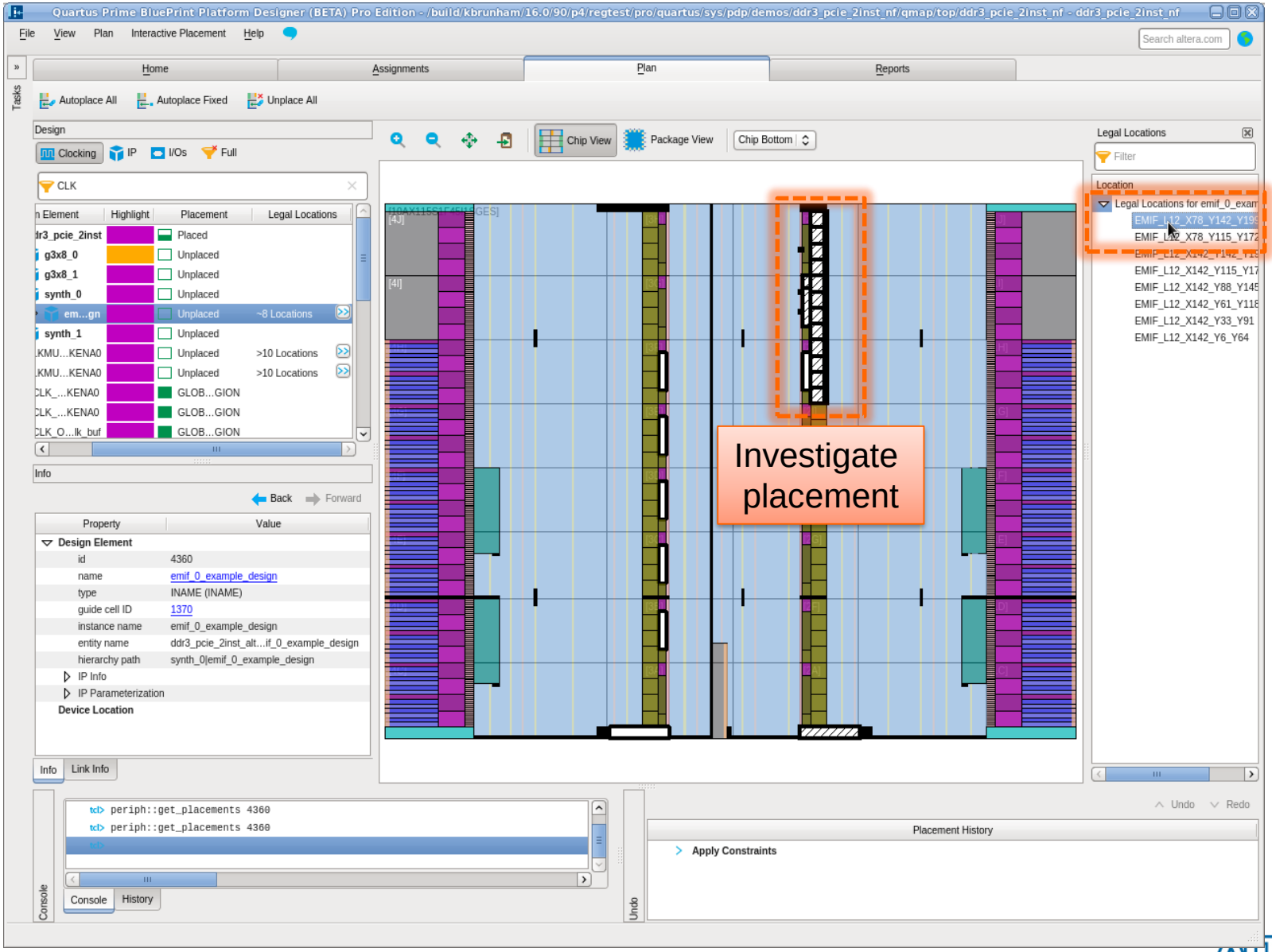


BluePrint Lab: Place interface on package view



Drag Memory Interface & Drop onto Package
White rectangle = Starting location
8 locations shown in example

BluePrint: Place whole interfaces using “drag-and-drop”



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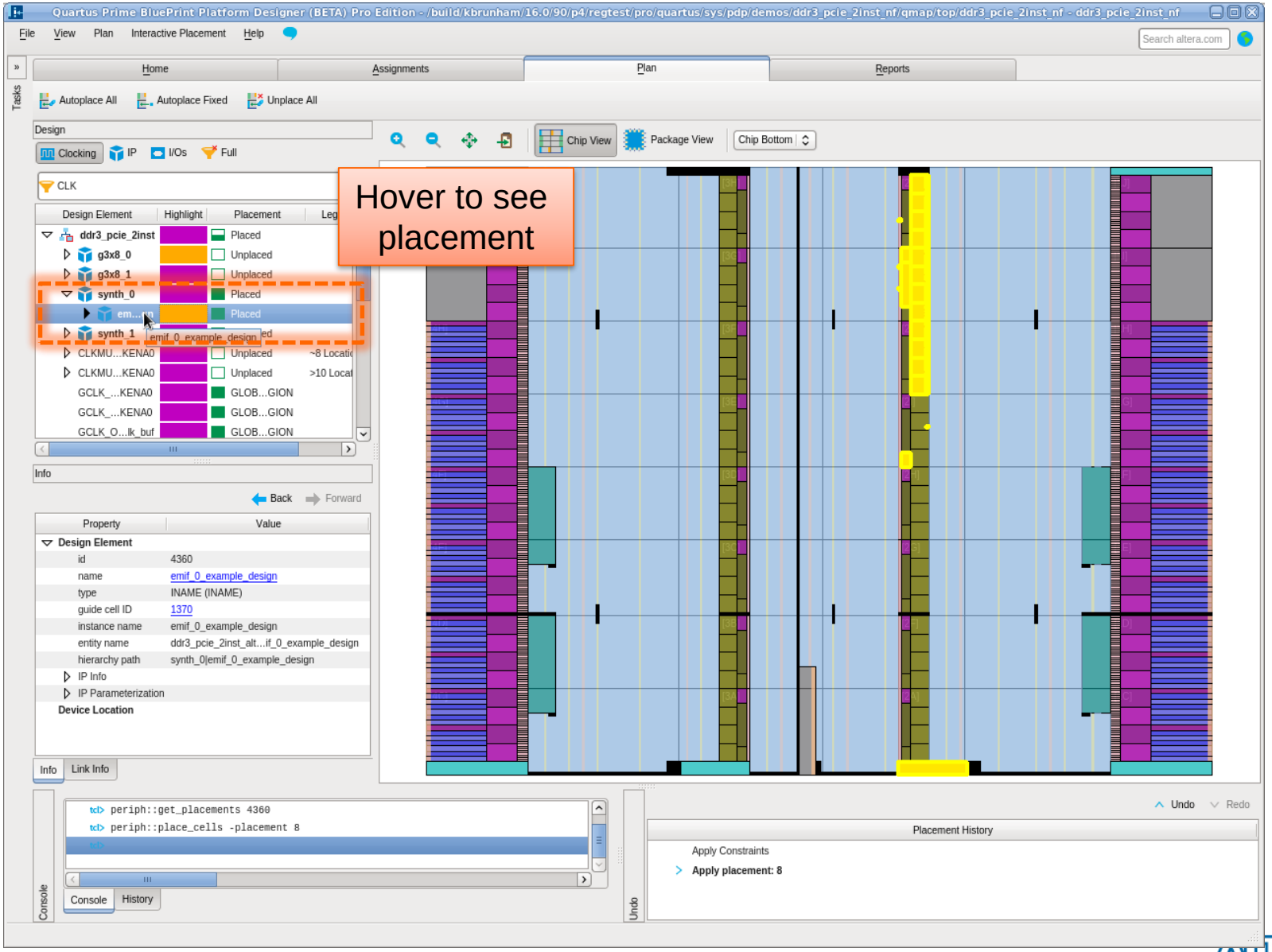

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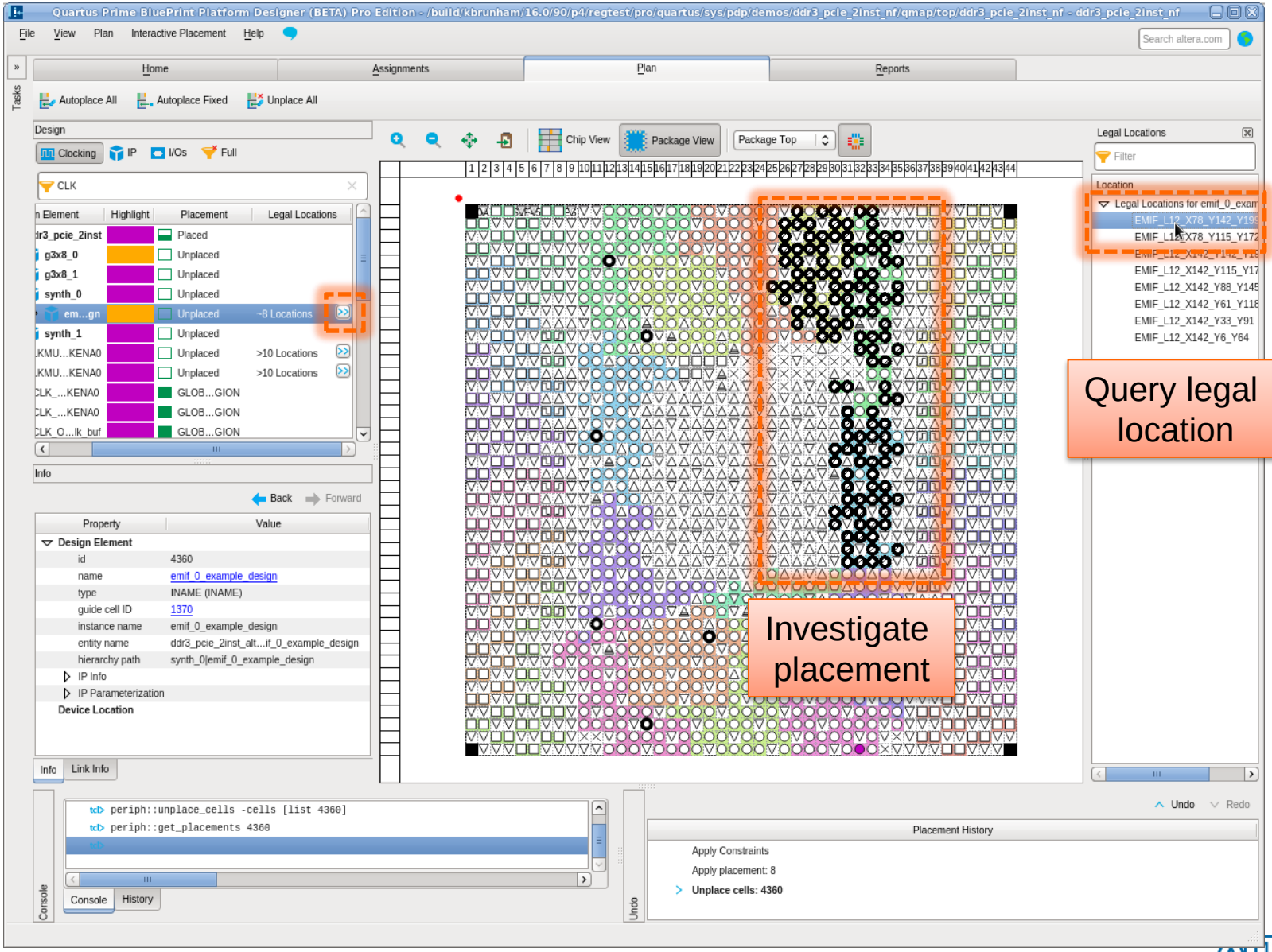
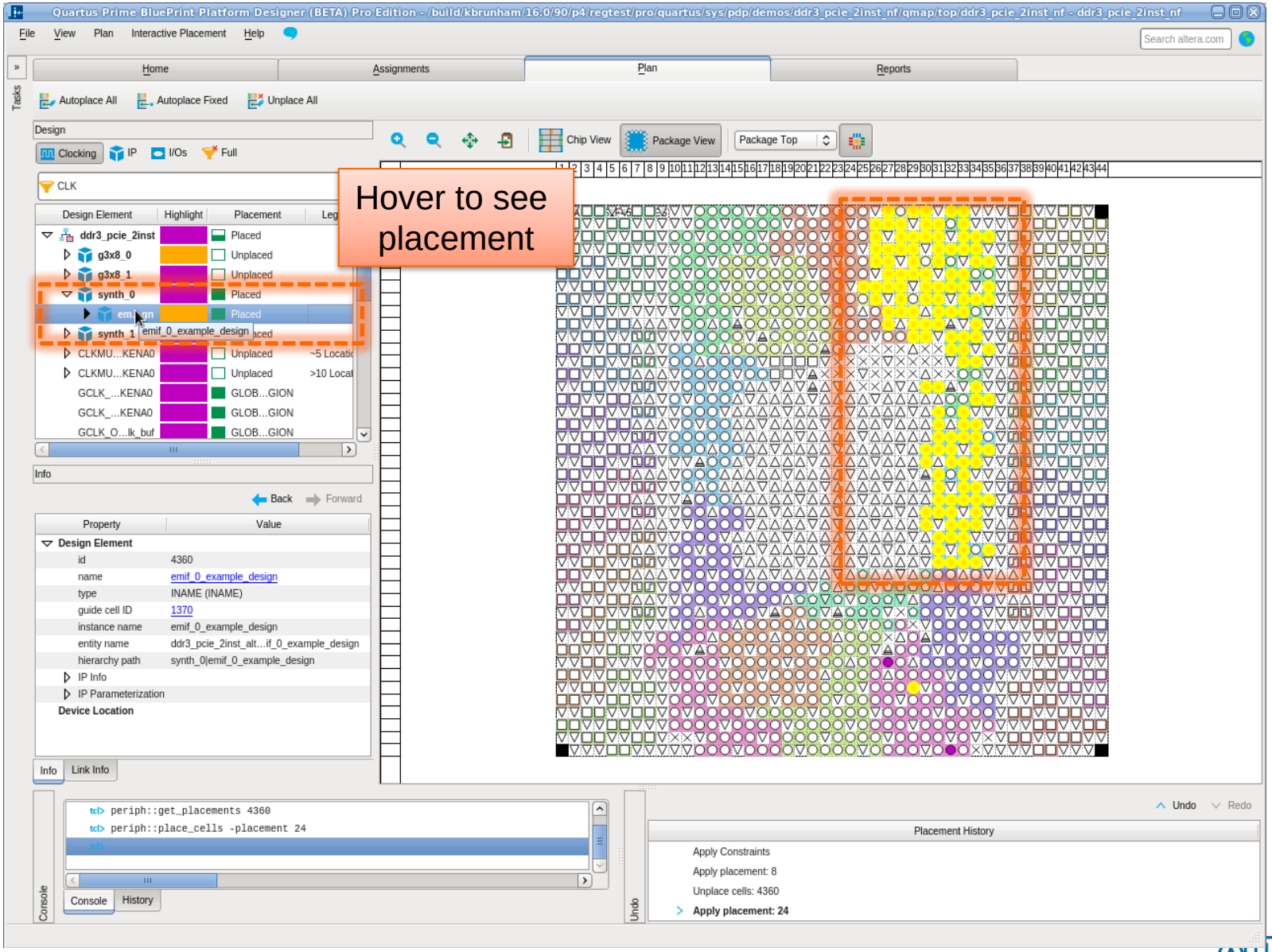
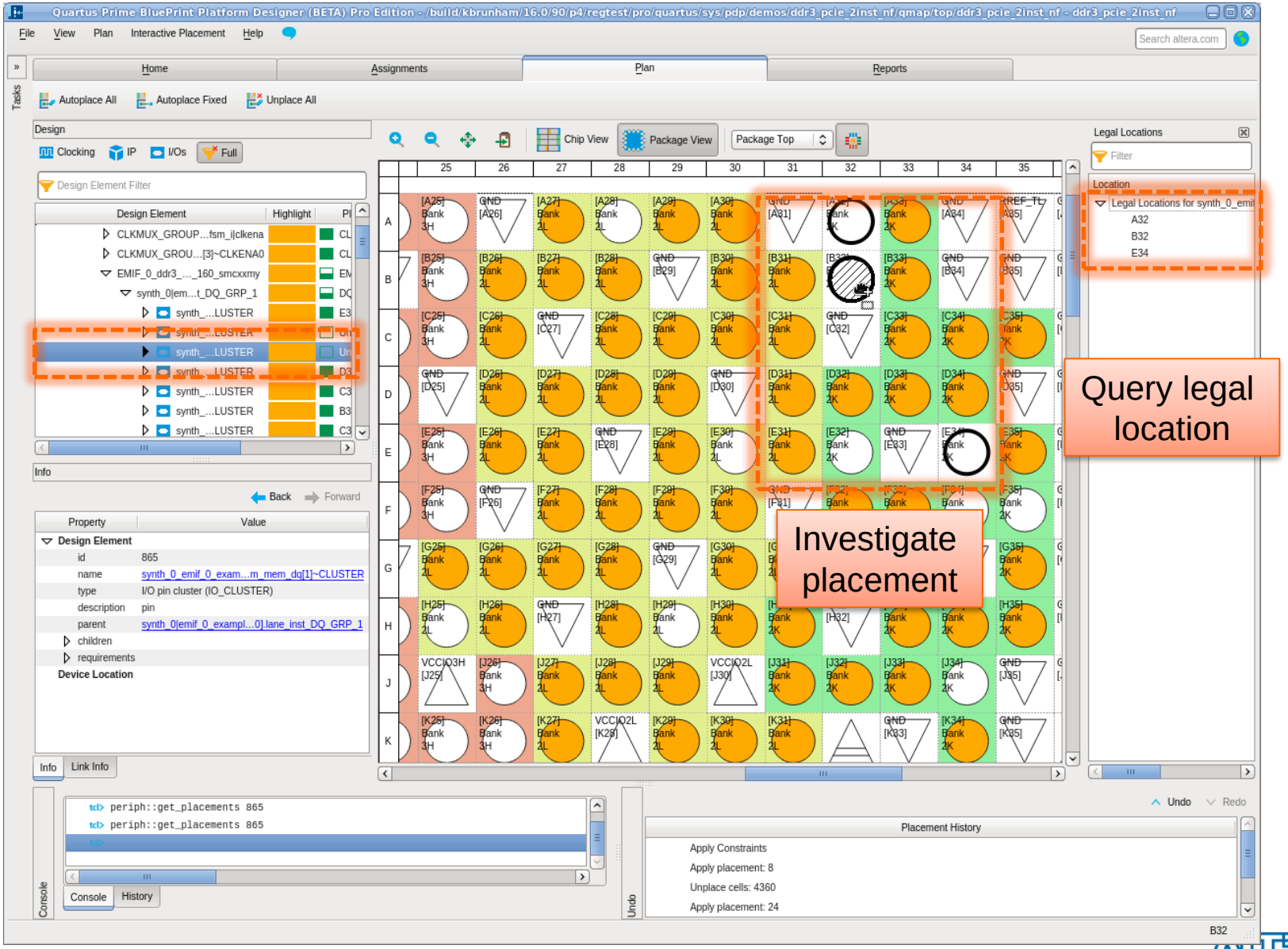


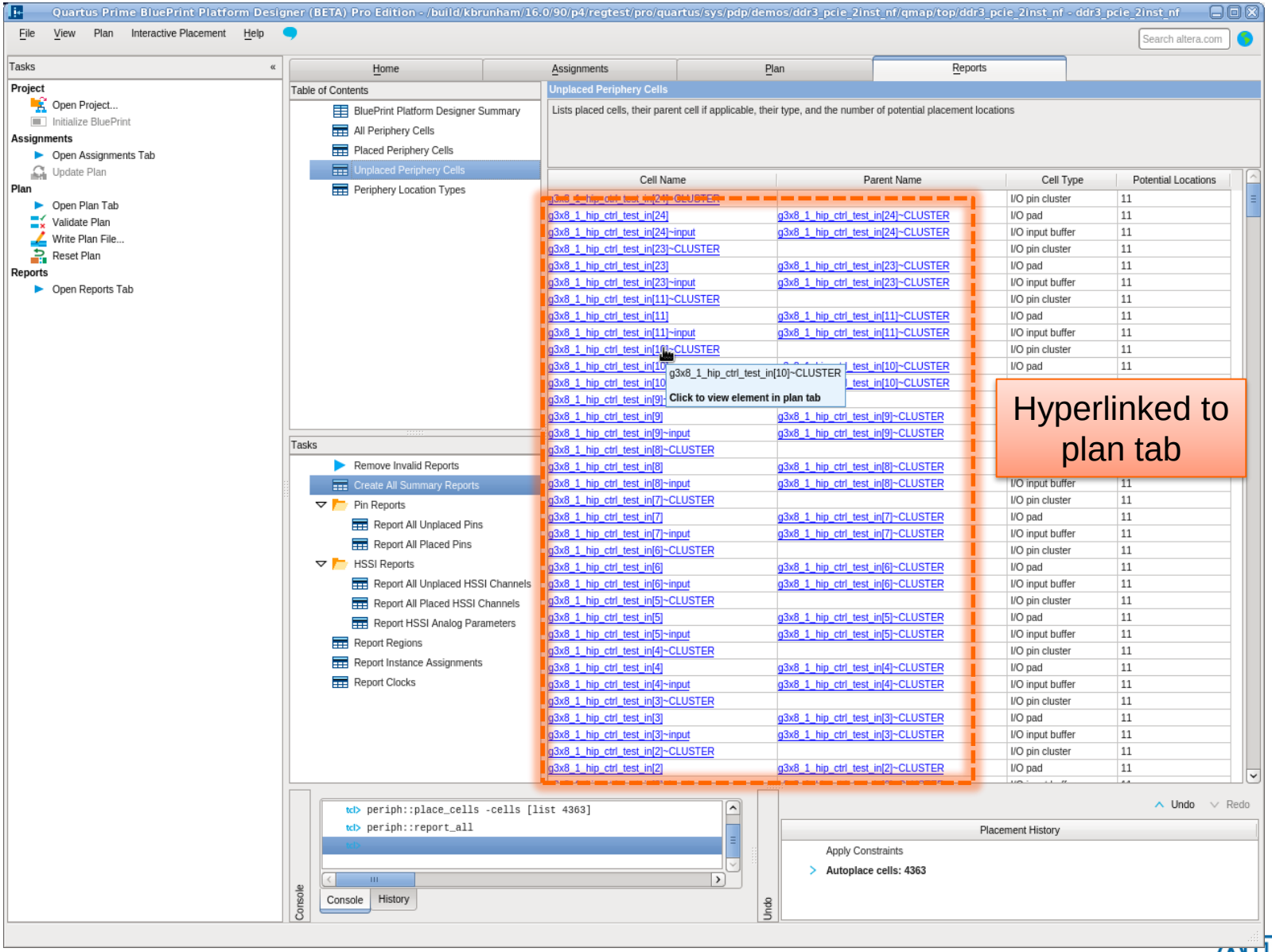
BluePrint: Place whole interfaces using “drag-and-drop”



BluePrint: Refine pins using “drag-and-drop”

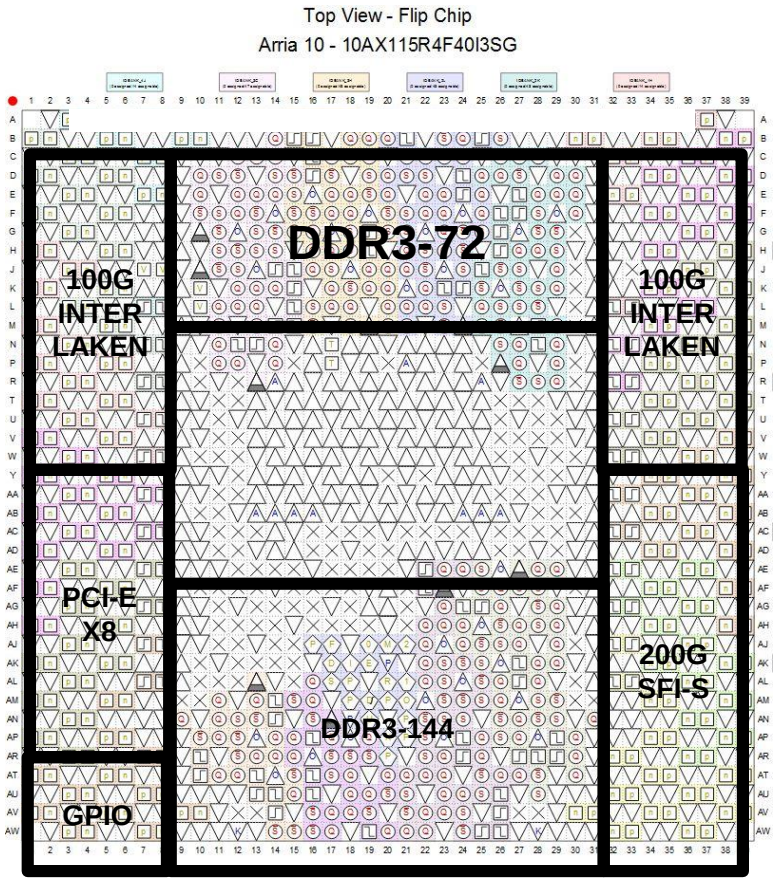


BluePrint: Rich reporting

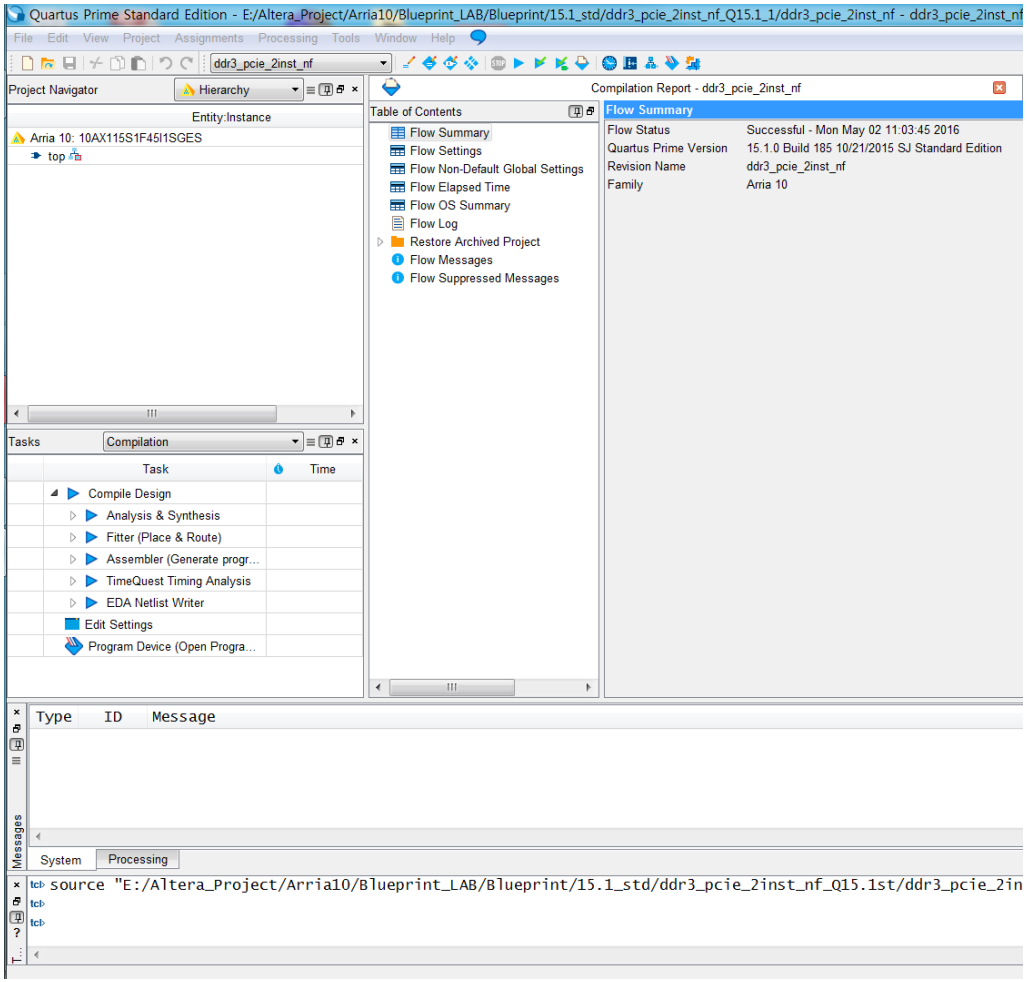


BluePrint Benefits: Reduce full compile iterations by 10x

- Generate **legal** pinout for board development at design start
  - BluePrint needs skeleton I/O netlist
  - Develop your fabric logic in parallel with board design
- Time to market due to iterations is reduced by 10x
  - Telecom customer example: 3 months to 1 week



BluePrint DEMO



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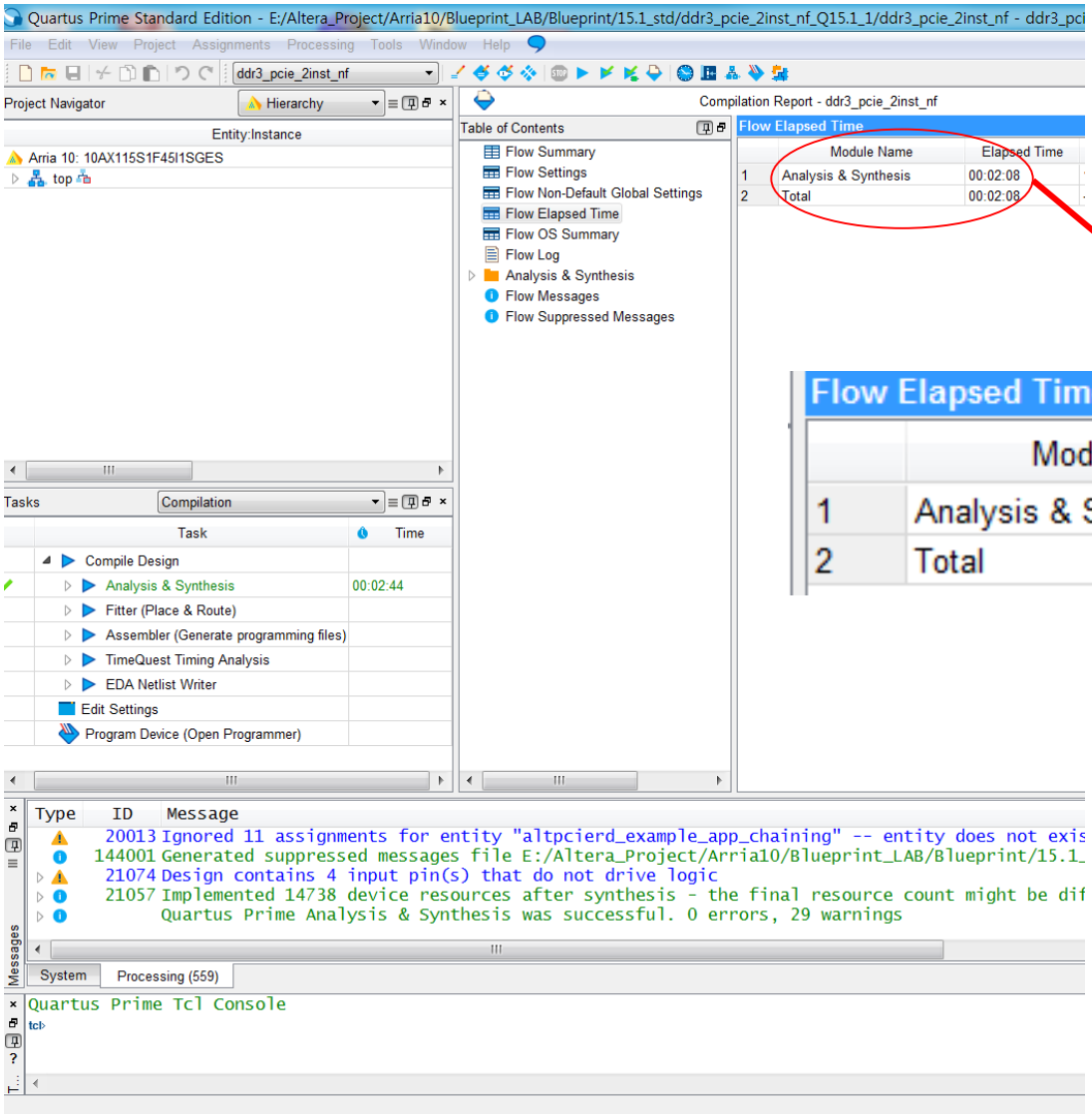

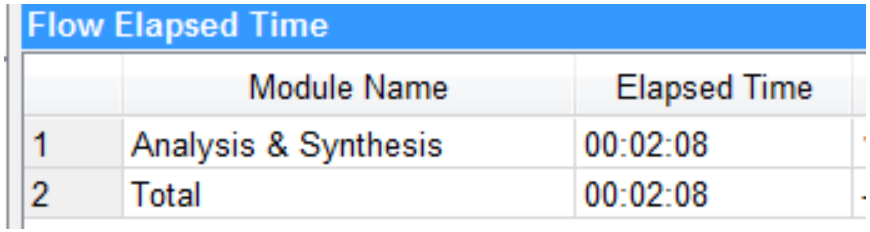

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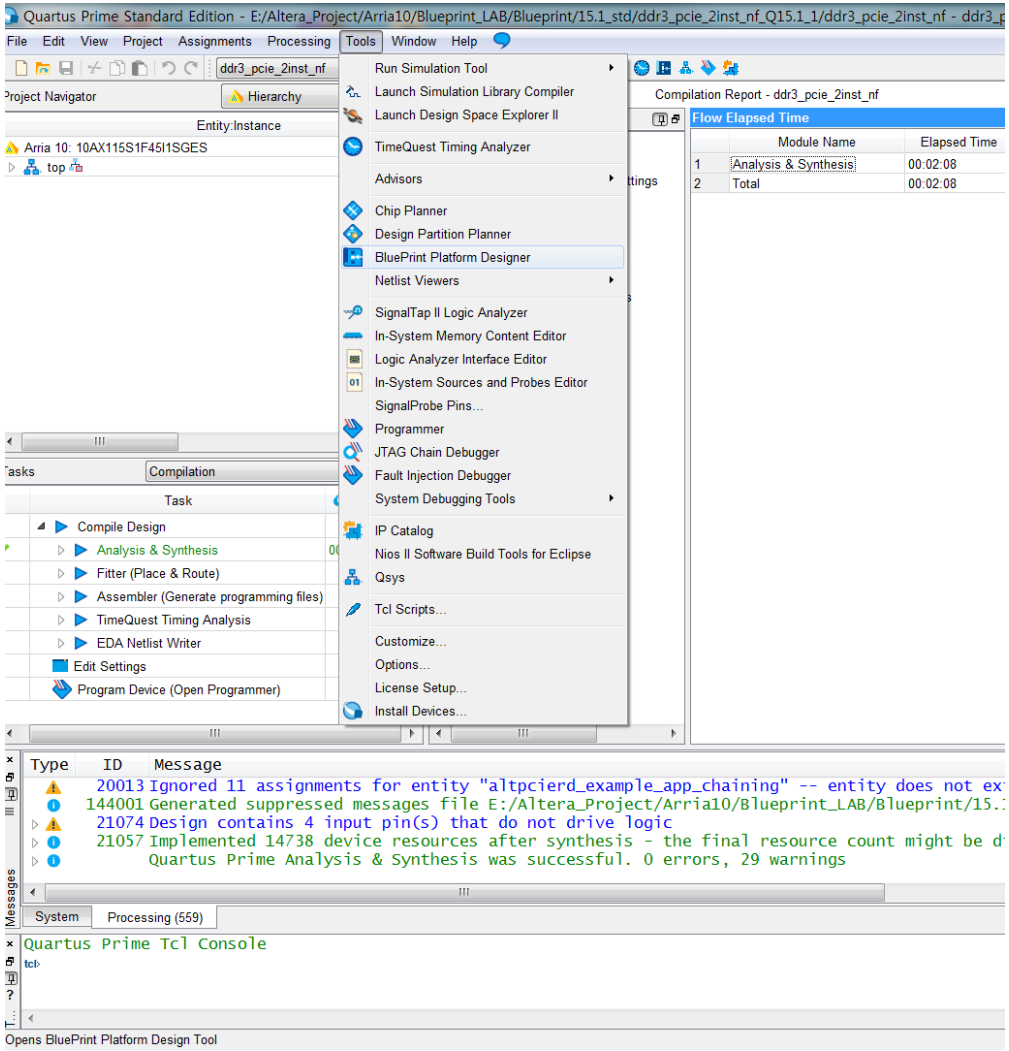

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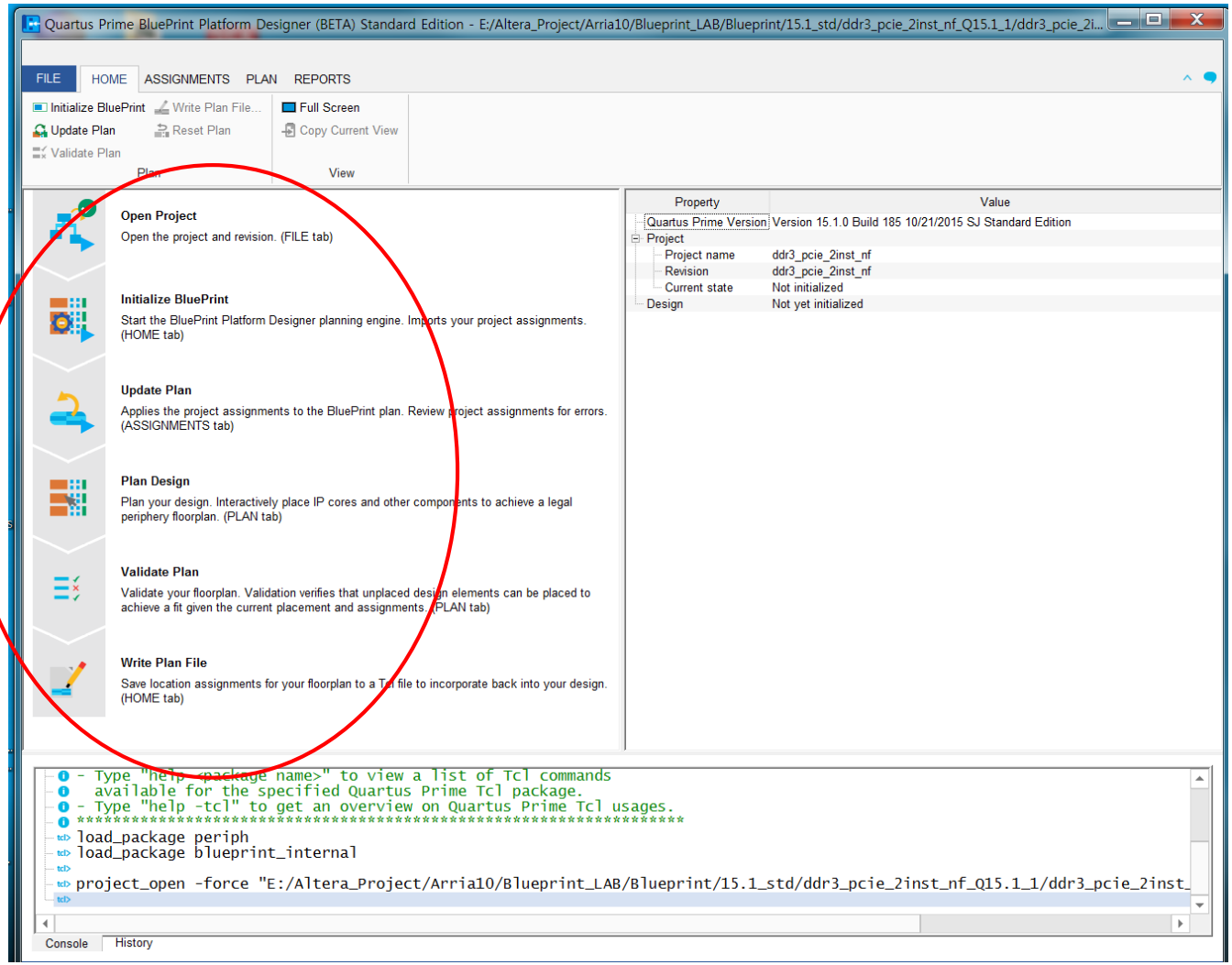

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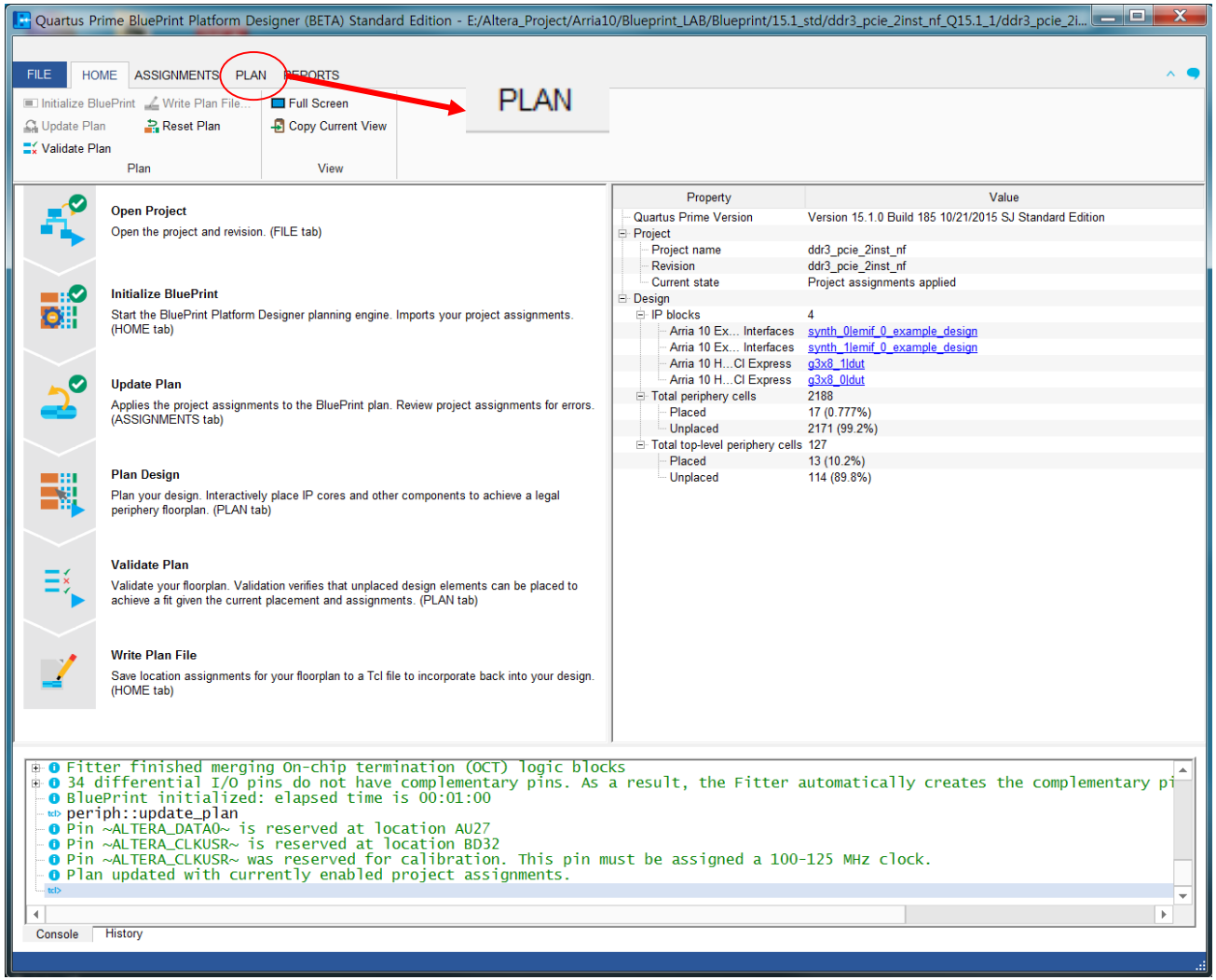

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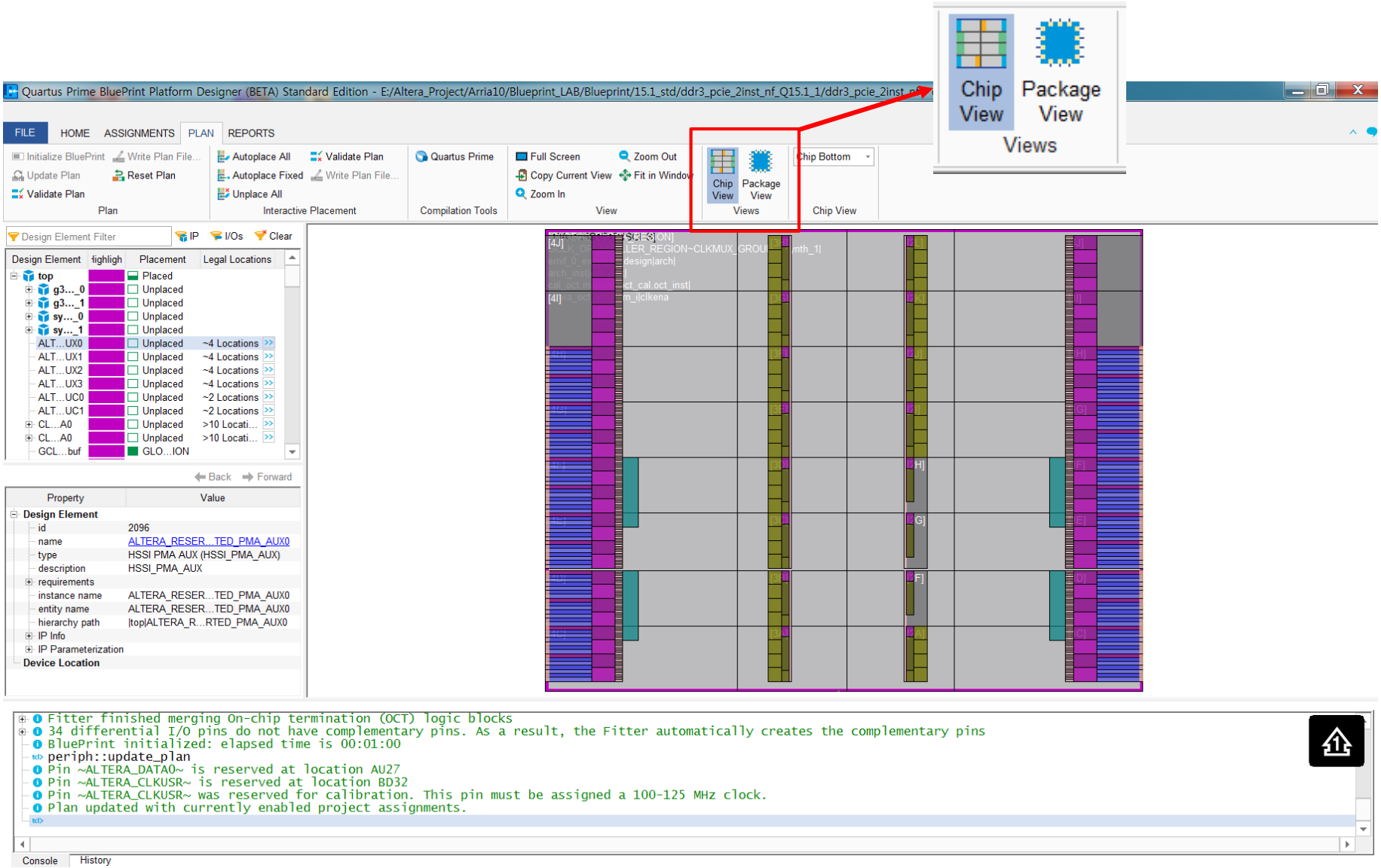
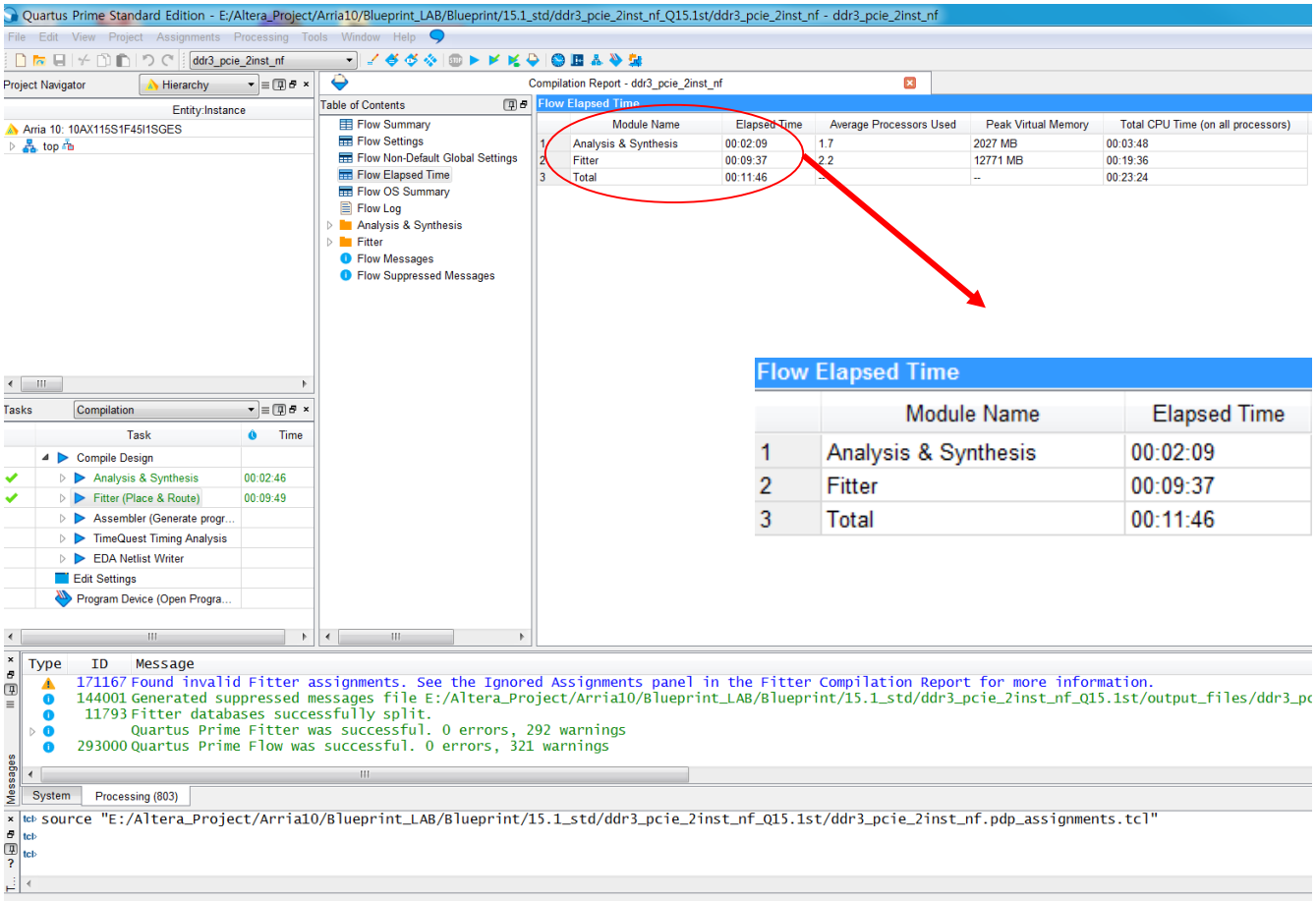


BluePrint DEMO

- 동영상

BluePrint DEMO



Thank You