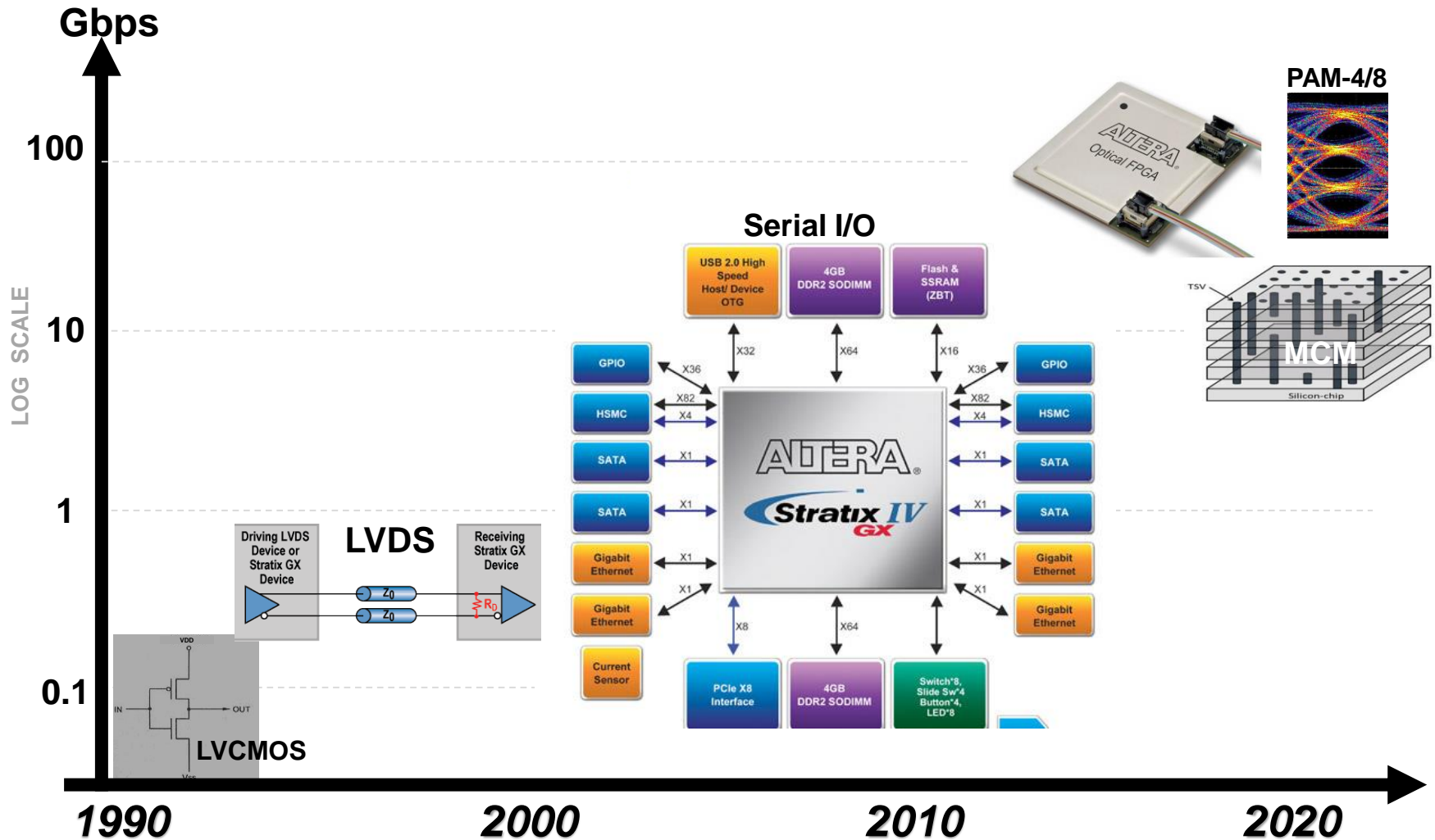


BluePrint Platform Designer



I/O evolution



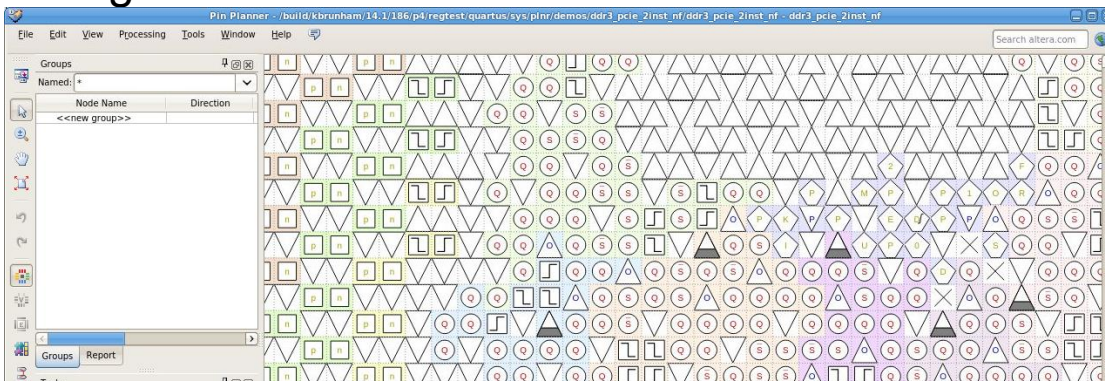
Floorplanning...Floorplanning...Floorplanning...

- ⤵ Floorplanning is hard to do...
- ⤵ Floorplanning makes my timing closure worse...
- ⤵ Floorplanning does not do what I expected...

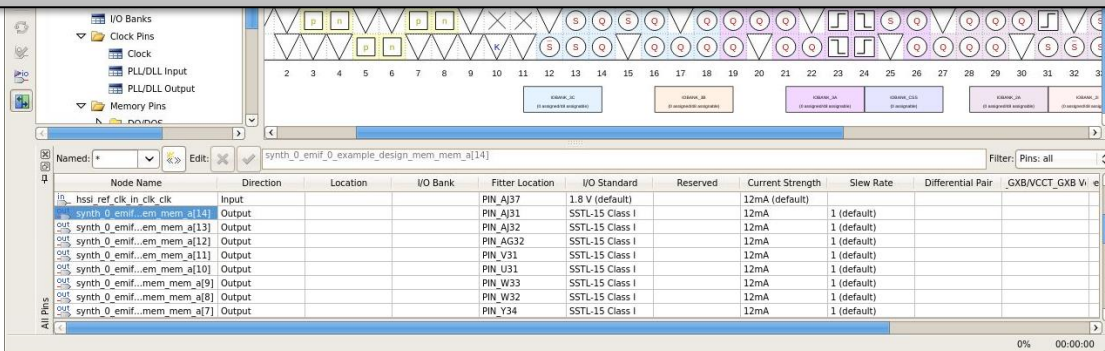
Shouldn't floorplanning be easy and intuitive?

Creating I/O assignments using the PinPlanner

- Traditionally the location for I/O elements can be done using the PinPlanner or Assignment Editor
 - These tools allow the creation of syntactically correct IO and location assignments

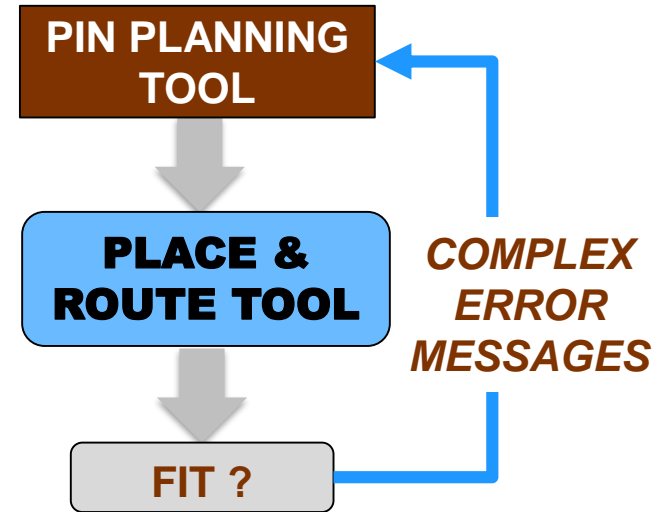


How do you use PinPlanner?



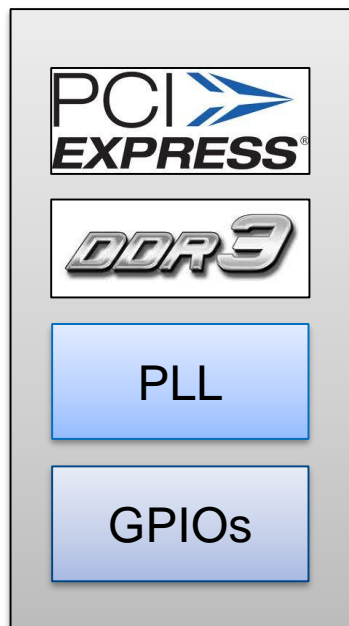
Current I/O Interface Placement Flow

- Current FPGA pin planners can assign locations, but cannot
 - Auto place pins
 - Accurately evaluate placement legality
 - Does not use the Fitter place and route engine
 - Report alternative placement to improve performance and resources
- Multiple, long iterations to resolve complex error messages**

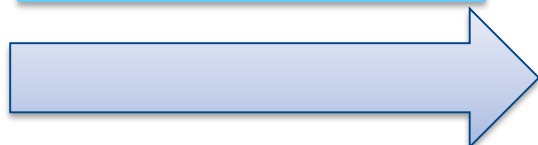


Note: FPGA tool = QUARTUS, VIVADO etc.,

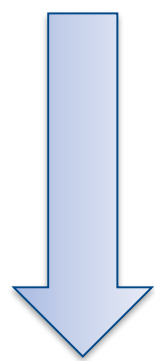
Problem: FPGA Placement is Complex



Input design with
illegal or incomplete
assignments



No Fit



What you want

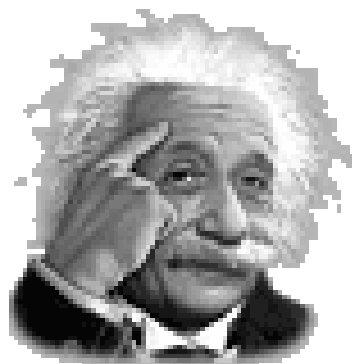
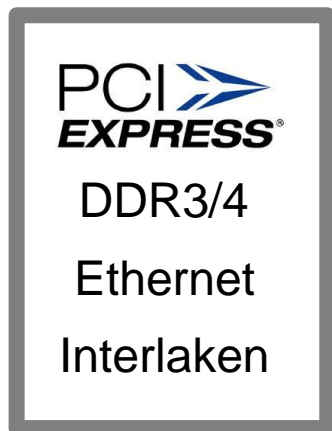
Error (175022): The auto-promoted clock driver could not be placed in any location to satisfy its connectivity requirements

Today, you need an expert on I/O Interface IP

IP Core Requirements



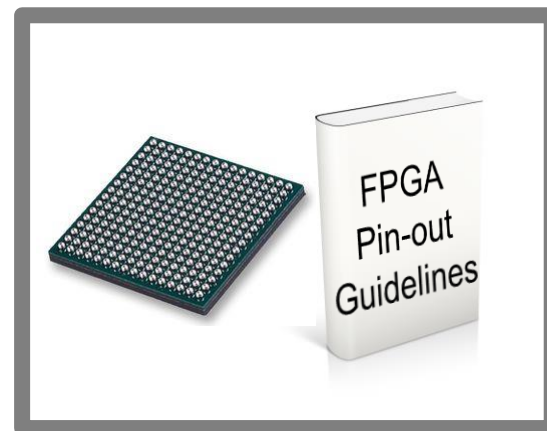
Interface Specification



Albert Einstein



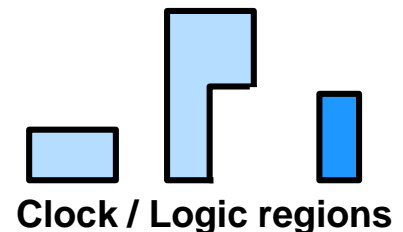
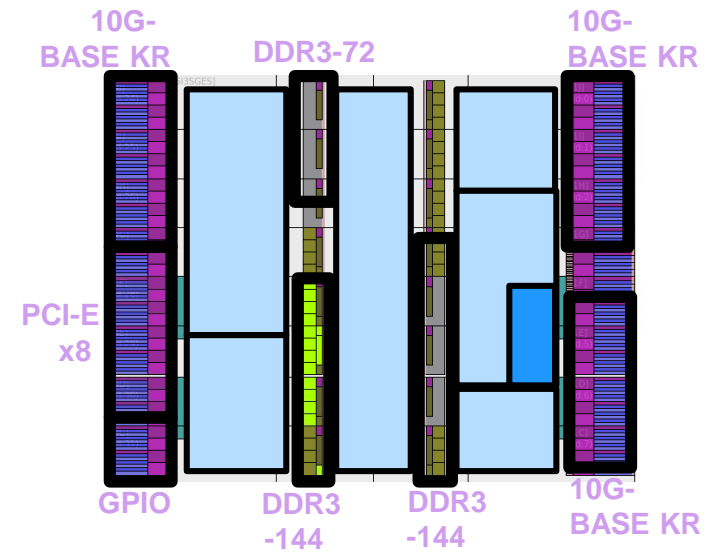
FPGA Specification



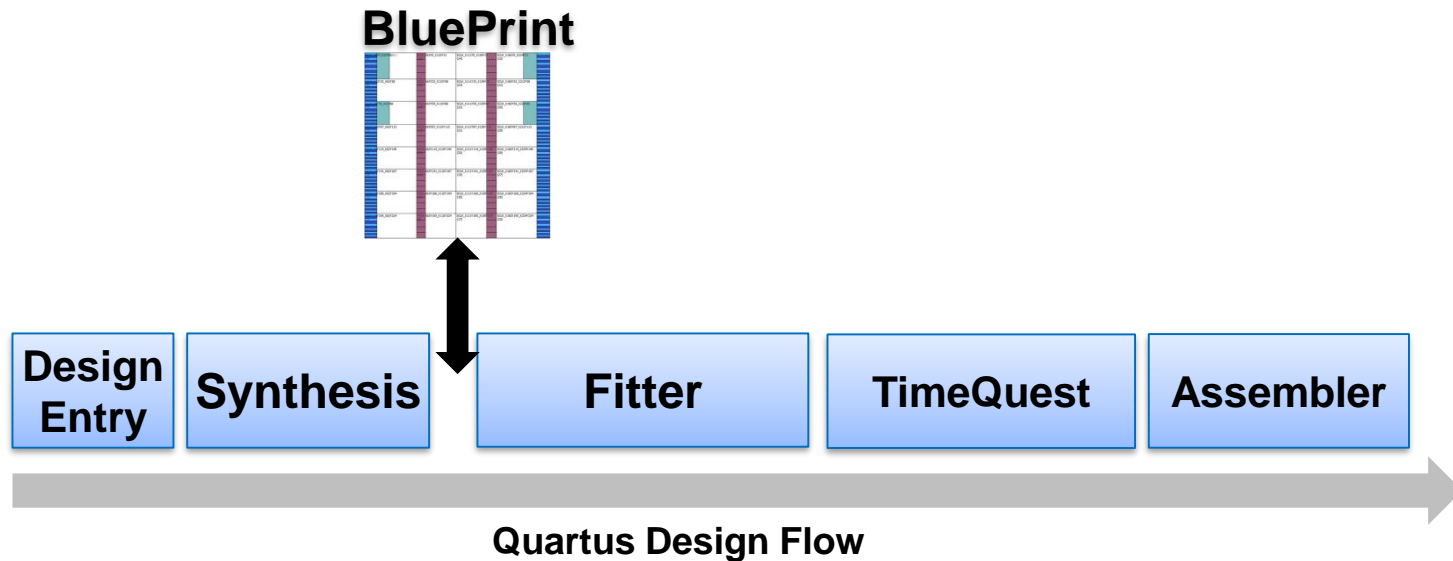
Let us re-capture the challenges

- Don't want to read tons of documents or debug of complex error messages
 - Instead, need legal & instantaneous I/O placement on package or chip floorplan
- Can we also avoid other legality issues such as clocks and floor-planning ?
 - Assign clock domains in FPGA fabric
 - Check quick fit of logic block partitions

Chip View



BluePrint Flow



◀ Synthesize design

- Create a skeletal system in Qsys, Megawizard or any other design entry method
- Fabric logic doesn't have to be complete

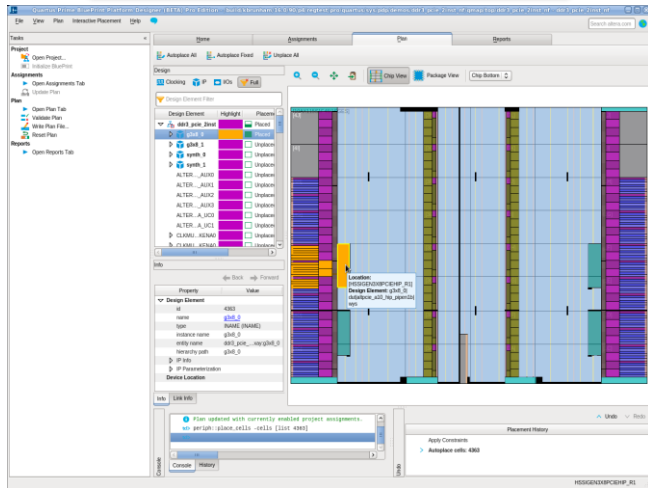
◀ Drag & drop I/O interface at top-level onto package, or chip floorplan

- Optionally, assign core clock domains

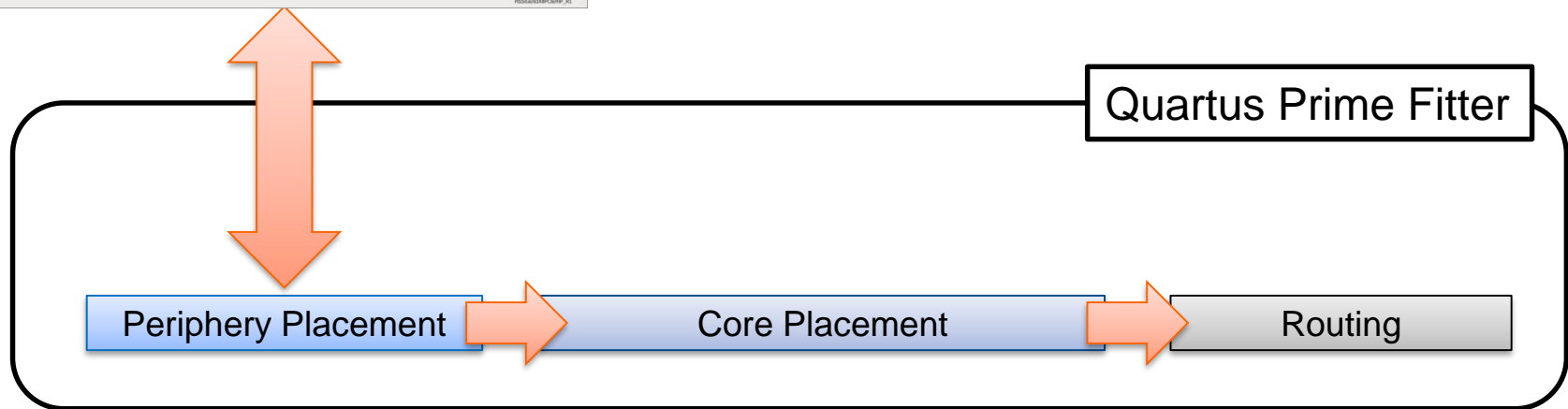
◀ Create a BluePrint in minutes (output Quartus assignment file)

BluePrint: Create legal assignments using the power of the Fitter

BluePrint Platform Designer



- BluePrint operates live with the Quartus Prime Fitter
- Legality reported in BluePrint comes from the Quartus Prime Fitter
- Different floorplanning scenarios can be evaluated using BluePrint
- Constraints generated from BluePrint can be used in a subsequent compile



Blueprint: Place whole interfaces using “drag-and-drop”

The screenshot displays the Quartus Prime Blueprint Platform Designer (BETA) Pro Edition interface. The main workspace shows a design grid with various components placed or ready to be placed. A table on the left lists design elements and their placement status.

Element	Highlight	Placement	Legal Locations
ddr3_pcie_2inst	Green	Placed	
g3x8_0	Yellow	Unplaced	
g3x8_1	Magenta	Unplaced	
synth_0	Light Blue	Unplaced	
emif_0	Light Blue	Unplaced	~8 Locations
synth_1	Light Blue	Unplaced	
KMU...KENAO	Magenta	Unplaced	>10 Locations
KMU...KENAO	Magenta	Unplaced	>10 Locations
CLK...KENAO	Green	GLOB...GION	
CLK...KENAO	Green	GLOB...GION	
CLK_O...lk_buf	Green	GLOB...GION	

The 'Legal Locations' panel on the right shows a list of locations for the selected component:

- EMIF_L12_X78_Y142_Y196
- EMIF_L12_X78_Y115_Y172
- EMIF_L12_X142_Y142_Y196
- EMIF_L12_X142_Y115_Y172
- EMIF_L12_X142_Y88_Y145
- EMIF_L12_X142_Y61_Y118
- EMIF_L12_X142_Y33_Y91
- EMIF_L12_X142_Y6_Y64

An orange callout box with the text "Query legal location" points to the 'Legal Locations' panel. Another orange box highlights the 'Legal Locations' column in the design element table.

The console at the bottom left shows the following commands:

```
tc> periph::get_placements 4360
tc> periph::get_placements 4360
```

Blueprint Lab: Place interface on package view

The screenshot displays the Quartus II software interface in Package View. The top menu bar includes FILE, HOME, ASSIGNMENTS, PLAN, and REPORTS. The PLAN tab is active, showing options like Initialize Blueprint, Write Plan File..., Update Plan, Reset Plan, Validate Plan, Autoplace All, Autoplace Fixed, Unplace All, and Validate Plan. The Package View is selected in the Views section, and Show I/O Banks is checked in the Package View section.

The Design Element Filter on the left shows a tree view of design elements. The 'emif_0_example_design' folder is highlighted with an orange box. It contains several sub-elements, including 'EMIF_0_top_altera_emif_150_f5jfmtq', which is currently unplaced. The Placement column shows 'Unplaced' for this element.

The Package View in the center shows a grid of package locations. A white rectangle highlights a starting location, and a red dashed line indicates the placement area. The Legal Locations panel on the right lists the legal locations for the EMIF_0_top element, with a red arrow pointing to the location EMIF_L12_X142_Y142_Y199.

The Location Filter at the bottom shows the current location: 10AX115S1F45I1SGES.

Drag Memory Interface & Drop onto Package
White rectangle = Starting location
8 locations shown in example

Design Element	Highlight	Placement	Legal Locations
top		Placed	
g3x8_0		Unplaced	
g3x8_1		Unplaced	
synth_0		Unplaced	
emif_0_example_design		Unplaced	
Clock control blocks		Unplaced	
External memory interfaces		Unplaced	
EMIF_0_top_altera_emif_150_f5jfmtq		Unplaced	
I/O AUXs		Unplaced	
I/O PLL refer. clock networks		Unplaced	
Impedance control blocks		Unplaced	
synth_1		Unplaced	
Clock control blocks		Unplaced	
Clock core fanouts		Placed	
HSSI core interfaces		Placed	
HSSI reference clock networks		Unplaced	

Location
EMIF_L12_X78_Y142_Y199
EMIF_L12_X78_Y115_Y172
EMIF_L12_X142_Y142_Y199
EMIF_L12_X142_Y115_Y172
EMIF_L12_X142_Y88_Y145
EMIF_L12_X142_Y61_Y118
EMIF_L12_X142_Y33_Y91
EMIF_L12_X142_Y6_Y64

Location	Design Element
10AX115S1F45I1SGES	ase Colo

```
id      1379
type    EMIF_GROUP
name    EMIF_0_top_altera_emif_150_f5jfmtq
description  EMIF_GROUP
```

BluePrint: Place whole interfaces using “drag-and-drop”

The screenshot displays the Quartus Prime BluePrint Platform Designer (BETA) Pro Edition interface. The main workspace shows a chip layout with various components. A central vertical interface is highlighted with an orange dashed box, and an orange callout box with the text "Investigate placement" points to it. The "Legal Locations" panel on the right lists several locations for the "emif_0_exan" component, with "EMIF_L12_X78_Y142_Y19" selected. The "Design" panel on the left shows a list of components, including "em...gn" which is currently unplaced. The "Info" panel at the bottom left shows the design element details for "emif_0_example_design". The "Console" at the bottom left shows the command "periph::get_placements 4360" being executed. The "Placement History" panel at the bottom right shows "Apply Constraints".

Property	Value
Design Element	
id	4360
name	emif_0_example_design
type	INAME (INAME)
guide cell ID	1370
instance name	emif_0_example_design
entity name	ddr3_pcie_2inst_alt...if_0_example_design
hierarchy path	synth_0emif_0_example_design
IP Info	
IP Parameterization	
Device Location	

```
periph::get_placements 4360
periph::get_placements 4360
```

BluePrint: Place whole interfaces using “drag-and-drop”

The screenshot displays the Quartus Prime BluePrint Platform Designer (BETA) Pro Edition interface. The main window shows a chip layout with various components placed on a grid. A callout box with the text "Hover to see placement" points to a specific component in the design element list. The design element list on the left shows a hierarchy of components, with "emif_0" highlighted. The Info panel below the list shows properties for the selected element. The Console at the bottom left shows the command "periph::place_cells -placement 8" being executed. The Placement History panel at the bottom right shows the command "Apply placement: 8".

Design Element List:

Design Element	Highlight	Placement	Legend
ddr3_pcie_2inst	Yellow	Placed	Green
g3x8_0	Orange	Unplaced	White
g3x8_1	Orange	Unplaced	White
synth_0	Blue	Placed	Green
emif_0	Blue	Placed	Green
synth_1	Blue	Placed	Green
emif_0_example_design	Blue	Placed	Green
CLKMU...KENA0	Green	Unplaced	White
CLKMU...KENA0	Green	Unplaced	White
GCLK...KENA0	Green	GLOB...GION	Green
GCLK...KENA0	Green	GLOB...GION	Green
GCLK_O...lk_buf	Green	GLOB...GION	Green

Info Panel:

Property	Value
Design Element	
id	4360
name	emif_0_example_design
type	INAME (INAME)
guide cell ID	1370
instance name	emif_0_example_design
entity name	ddr3_pcie_2inst_alt...if_0_example_design
hierarchy path	synth_0emif_0_example_design
IP Info	
IP Parameterization	
Device Location	

Console:

```
tc> periph::get_placements 4360
tc> periph::place_cells -placement 8
tc>
```

Placement History:

```
Apply Constraints
> Apply placement: 8
```

BluePrint: Place whole interfaces using “drag-and-drop”

The screenshot displays the Quartus Prime BluePrint Platform Designer (BETA) Pro Edition interface. The main workspace shows a grid of placement cells with a large orange dashed box highlighting a specific area. A text box labeled "Investigate placement" is overlaid on this area. On the left, the "Design" panel shows a list of elements, with "emif_0" selected and highlighted by an orange box. Below this, the "Info" panel displays properties for the selected element. On the right, the "Legal Locations" panel shows a list of locations, with "EMIF_L12_X78_Y142_Y19" selected and highlighted by an orange box. A text box labeled "Query legal location" is overlaid on this panel. The bottom of the interface features a console window with the following commands and output:

```
tc> periph::unplace_cells -cells [list 4360]
tc> periph::get_placements 4360
tc>
```

The console also shows the output: "Apply Constraints", "Apply placement: 8", and "Unplace cells: 4360".

BluePrint: Place whole interfaces using “drag-and-drop”

Quartus Prime BluePrint Platform Designer (BETA) Pro Edition - /build/kbrunham/16.0/90/p4/regtest/pro/quartus/sys/pdp/demos/ddr3_pcie_2inst_nf/qmap/top/ddr3_pcie_2inst_nf - ddr3_pcie_2inst_nf

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Tasks Autoplace All Autoplace Fixed Unplace All

Design

CLK

Design Element	Highlight	Placement	Leg
ddr3_pcie_2inst	[Yellow]	Placed	
g3x8_0	[Purple]	Unplaced	
g3x8_1	[Purple]	Unplaced	
synth_0	[Purple]	Placed	
emif_0	[Blue]	Placed	
synth_1	[Blue]	emif_0_example_design	Placed
CLKMU...KENA0	[Purple]	Unplaced	~5 Locat
CLKMU...KENA0	[Purple]	Unplaced	>10 Locat
GCLK...KENA0	[Purple]	GLOB...GION	
GCLK...KENA0	[Purple]	GLOB...GION	
GCLK_O...lk_buf	[Purple]	GLOB...GION	

Info

Back Forward

Property	Value
Design Element	
id	4360
name	emif_0_example_design
type	INAME (INAME)
guide cell ID	1370
instance name	emif_0_example_design
entity name	ddr3_pcie_2inst_alt...if_0_example_design
hierarchy path	synth_0emif_0_example_design
IP Info	
IP Parameterization	
Device Location	

Info Link Info

```
tc> periph::get_placements 4360
tc> periph::place_cells -placement 24
tc>
```

Console History

Undo Redo

Placement History

- Apply Constraints
- Apply placement: 8
- Unplace cells: 4360
- Apply placement: 24

BluePrint: Refine pins using “drag-and-drop”

The screenshot displays the Quartus Prime BluePrint Platform Designer (BETA) Pro Edition interface. The main workspace shows a grid of pins for a device, with columns numbered 25 to 35 and rows labeled A through K. A red dashed box highlights a specific area of the grid, and a callout box labeled "Investigate placement" points to it. Another red dashed box highlights a list of legal locations (A32, B32, E34) in the "Legal Locations" panel, with a callout box labeled "Query legal location" pointing to it. The interface includes a menu bar (File, View, Plan, Interactive Placement, Help), a toolbar with icons for Autoplace All, Autoplace Fixed, and Unplace All, and a Design Element Filter on the left. The Design Element Filter shows a tree view of design elements, with "synth_0...LUSTER" selected. The Info panel on the left shows the properties of the selected element, including its name, type, and device location. The Console at the bottom left shows the command `periph::get_placements 865` being executed. The Placement History panel at the bottom right shows the sequence of actions: Apply Constraints, Apply placement: 8, Unplace cells: 4360, and Apply placement: 24.

Quartus Prime BluePrint Platform Designer (BETA) Pro Edition - /build/kbrunham/16.0/90/p4/regtest/pro/quartus/sys/pdp/demos/ddr3_pcie_2inst_nf/qmap/top/ddr3_pcie_2inst_nf - ddr3_pcie_2inst_nf

File View Plan Interactive Placement Help

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Tasks Autoplace All Autoplace Fixed Unplace All

Design

Cloning IP I/Os Full

Design Element Filter

Design Element Highlight Pin

- CLKMUX_GROUP...ism_ijckena
- CLKMUX_GROUP...[3]-CLKENA0
- EMIF_0_ddr3...160_smcxomy
- synth_0lem...1_DQ_GRP_1
 - synth_...LUSTER
 - synth_...LUSTER
 - synth_...LUSTER
 - synth_...LUSTER
 - synth_...LUSTER
 - synth_...LUSTER

Info

Property Value

Design Element

- id 865
- name synth_0_emif_0_exam...m_mem_dq[1]-CLUSTER
- type I/O pin cluster (IO_CLUSTER)
- description pin
- parent synth_0lemif_0_exampl...0_lane_inst_DQ_GRP_1
- children
- requirements
- Device Location

Info Link Info

Console

```
tc> periph::get_placements 865
tc> periph::get_placements 865
```

Placement History

- Apply Constraints
- Apply placement: 8
- Unplace cells: 4360
- Apply placement: 24

Legal Locations

Filter

Location

- Legal Locations for synth_0_emif_0_exampl...0_lane_inst_DQ_GRP_1
 - A32
 - B32
 - E34

Query legal location

Investigate placement

B32

ALTERA

BluePrint: Rich reporting

Quartus Prime BluePrint Platform Designer (BETA) Pro Edition - /build/kbrunham/16.0/90/p4/regtest/pro/quartus/sys/pdp/demos/ddr3_pcie_21nst_nf/qmap/top/ddr3_pcie_21nst_nf - ddr3_pcie_21nst_nf

File View Plan Interactive Placement Help

Search altera.com

Tasks

Project

- Open Project...
- Initialize BluePrint

Assignments

- Open Assignments Tab
- Update Plan

Plan

- Open Plan Tab
- Validate Plan
- Write Plan File...
- Reset Plan

Reports

- Open Reports Tab

Home

Table of Contents

- BluePrint Platform Designer Summary
- All Periphery Cells
- Placed Periphery Cells
- Unplaced Periphery Cells**
- Periphery Location Types

Assignments

Plan

Reports

Unplaced Periphery Cells

Lists placed cells, their parent cell if applicable, their type, and the number of potential placement locations

Cell Name	Parent Name	Cell Type	Potential Locations
g3x8_1_hip_ctrl_test_in[24]-CLUSTER	g3x8_1_hip_ctrl_test_in[24]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[24]	g3x8_1_hip_ctrl_test_in[24]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[24]-input	g3x8_1_hip_ctrl_test_in[24]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[23]-CLUSTER	g3x8_1_hip_ctrl_test_in[23]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[23]	g3x8_1_hip_ctrl_test_in[23]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[23]-input	g3x8_1_hip_ctrl_test_in[23]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[11]-CLUSTER	g3x8_1_hip_ctrl_test_in[11]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[11]	g3x8_1_hip_ctrl_test_in[11]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[11]-input	g3x8_1_hip_ctrl_test_in[11]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[10]-CLUSTER	g3x8_1_hip_ctrl_test_in[10]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[10]	g3x8_1_hip_ctrl_test_in[10]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[10]	g3x8_1_hip_ctrl_test_in[10]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[9]	g3x8_1_hip_ctrl_test_in[9]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[9]	g3x8_1_hip_ctrl_test_in[9]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[9]-input	g3x8_1_hip_ctrl_test_in[9]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[8]-CLUSTER	g3x8_1_hip_ctrl_test_in[8]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[8]	g3x8_1_hip_ctrl_test_in[8]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[8]-input	g3x8_1_hip_ctrl_test_in[8]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[7]-CLUSTER	g3x8_1_hip_ctrl_test_in[7]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[7]	g3x8_1_hip_ctrl_test_in[7]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[7]-input	g3x8_1_hip_ctrl_test_in[7]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[6]-CLUSTER	g3x8_1_hip_ctrl_test_in[6]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[6]	g3x8_1_hip_ctrl_test_in[6]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[6]-input	g3x8_1_hip_ctrl_test_in[6]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[5]-CLUSTER	g3x8_1_hip_ctrl_test_in[5]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[5]	g3x8_1_hip_ctrl_test_in[5]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[5]-input	g3x8_1_hip_ctrl_test_in[5]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[4]-CLUSTER	g3x8_1_hip_ctrl_test_in[4]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[4]	g3x8_1_hip_ctrl_test_in[4]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[4]-input	g3x8_1_hip_ctrl_test_in[4]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[3]-CLUSTER	g3x8_1_hip_ctrl_test_in[3]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[3]	g3x8_1_hip_ctrl_test_in[3]-CLUSTER	I/O pad	11
g3x8_1_hip_ctrl_test_in[3]-input	g3x8_1_hip_ctrl_test_in[3]-CLUSTER	I/O input buffer	11
g3x8_1_hip_ctrl_test_in[2]-CLUSTER	g3x8_1_hip_ctrl_test_in[2]-CLUSTER	I/O pin cluster	11
g3x8_1_hip_ctrl_test_in[2]	g3x8_1_hip_ctrl_test_in[2]-CLUSTER	I/O pad	11

Click to view element in plan tab

Hyperlinked to plan tab

Tasks

- Remove Invalid Reports
- Create All Summary Reports
- Pin Reports
 - Report All Unplaced Pins
 - Report All Placed Pins
- HSSI Reports
 - Report All Unplaced HSSI Channels
 - Report All Placed HSSI Channels
 - Report HSSI Analog Parameters
- Report Regions
- Report Instance Assignments
- Report Clocks

Console

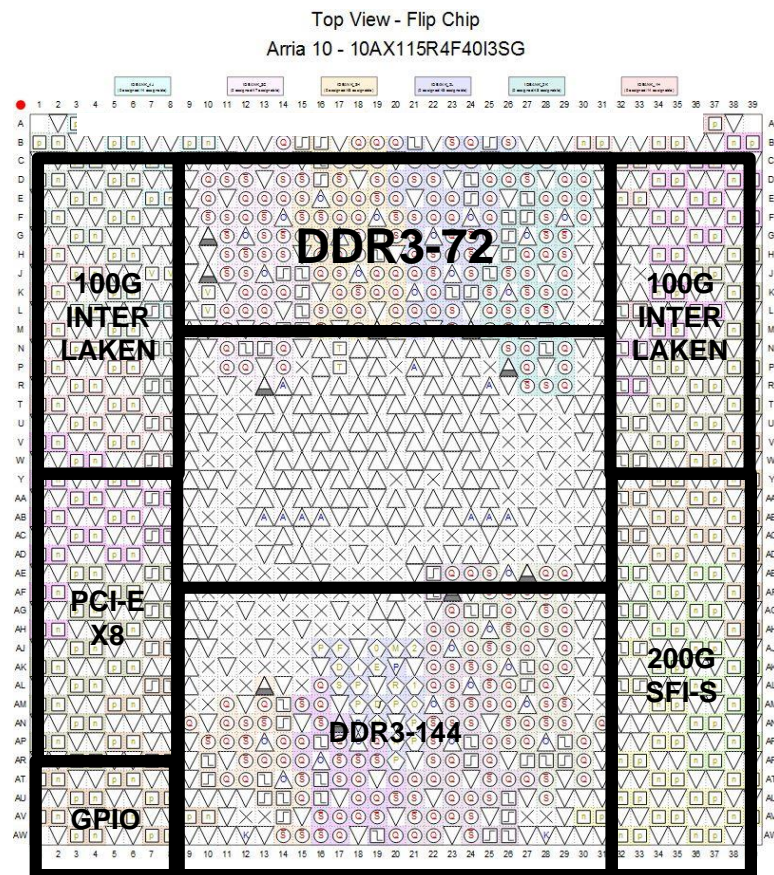
```
td> periph::place_cells -cells [list 4363]
td> periph::report_all
```

Placement History

- Apply Constraints
- Autoplace cells: 4363

BluePrint Benefits: Reduce full compile iterations by 10x

- Generate **legal** pinout for board development at design start
 - BluePrint needs skeleton I/O netlist
 - Develop your fabric logic in parallel with board design
- Time to market due to iterations is reduced by 10x
 - Telecom customer example: 3 months to 1 week



Blueprint DEMO

The screenshot displays the Quartus Prime Standard Edition interface. The main window shows the 'Compilation Report - ddr3_pcie_2inst_nf' with a 'Flow Summary' tab selected. The report indicates a successful compilation on Monday, May 02, 2016, at 11:03:45. The Quartus Prime version is 15.1.0 Build 185, and the revision name is 'ddr3_pcie_2inst_nf' for the 'Arria 10' family.

The 'Table of Contents' pane on the left lists the following sections:

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Restore Archived Project
- Flow Messages
- Flow Suppressed Messages

The 'Tasks' pane at the bottom left shows the compilation process:

Task	Time
Complete Design	
Analysis & Synthesis	
Filter (Place & Route)	
Assembler (Generate progr...	
TimeQuest Timing Analysis	
EDA Netlist Writer	
Edit Settings	
Program Device (Open Progra...	

The 'Messages' pane at the bottom shows a system message:

```
System Processing  
tc: source "E:/Altera_Project/Arria10/Blueprint_LAB/Blueprint/15.1_std/ddr3_pcie_2inst_nf_Q15.1st/ddr3_pcie_2in
```

Blueprint DEMO

The screenshot shows the Quartus Prime Standard Edition interface. The top window is the 'Compilation Report - ddr3_pcie_2inst_nf'. The 'Table of Contents' pane on the left lists various report sections, with 'Flow Elapsed Time' selected. The 'Flow Elapsed Time' report is displayed in a table:

	Module Name	Elapsed Time
1	Analysis & Synthesis	00:02:08
2	Total	00:02:08

A red circle highlights the 'Analysis & Synthesis' row, and a red arrow points from it to a larger, detailed view of the 'Flow Elapsed Time' report on the right. The 'Tasks' pane shows the 'Compile Design' task with a sub-task 'Analysis & Synthesis' taking 00:02:44. The 'Messages' pane at the bottom shows several messages, including a warning about ignored assignments and a success message for the synthesis process.

Flow Elapsed Time		
	Module Name	Elapsed Time
1	Analysis & Synthesis	00:02:08
2	Total	00:02:08

Blueprint DEMO

The screenshot displays the Quartus Prime Standard Edition interface. The 'Tools' menu is open, highlighting 'BluePrint Platform Designer'. The 'Tasks' window shows the 'Compile Design' task, with 'Analysis & Synthesis' selected. The 'Messages' window shows the following output:

```
Type ID Message
[Warning] 20013 Ignored 11 assignments for entity "altpciard_example_app_chaining" -- entity does not exist
[Info] 144001 Generated suppressed messages file E:/Altera_Project/Arria10/Blueprint_LAB/Blueprint/15.1/
[Warning] 21074 Design contains 4 input pin(s) that do not drive logic
[Info] 21057 Implemented 14738 device resources after synthesis - the final resource count might be different
[Info] Quartus Prime Analysis & Synthesis was successful. 0 errors, 29 warnings
```

The 'Compilation Report - ddr3_pcie_2inst_nf' window shows the following 'Flow Elapsed Time' table:

	Module Name	Elapsed Time
1	Analysis & Synthesis	00:02:08
2	Total	00:02:08

BluePrint DEMO

Quartus Prime BluePrint Platform Designer (BETA) Standard Edition - E:/Altera_Project/Arria10/Blueprint_LAB/Blueprint/15.1_std/ddr3_pcie_2inst_nf_Q15.1.1/ddr3_pcie_2inst...

FILE HOME ASSIGNMENTS PLAN REPORTS

Initialize BluePrint Write Plan File... Full Screen
Update Plan Reset Plan Copy Current View
Validate Plan

Plan View

Open Project
Open the project and revision. (FILE tab)

Initialize BluePrint
Start the BluePrint Platform Designer planning engine. Imports your project assignments. (HOME tab)

Update Plan
Applies the project assignments to the BluePrint plan. Review project assignments for errors. (ASSIGNMENTS tab)

Plan Design
Plan your design. Interactively place IP cores and other components to achieve a legal periphery floorplan. (PLAN tab)

Validate Plan
Validate your floorplan. Validation verifies that unplaced design elements can be placed to achieve a fit given the current placement and assignments. (PLAN tab)

Write Plan File
Save location assignments for your floorplan to a Tcl file to incorporate back into your design. (HOME tab)

Property	Value
Quartus Prime Version	Version 15.1.0 Build 185 10/21/2015 SJ Standard Edition
Project	
Project name	ddr3_pcie_2inst_nf
Revision	ddr3_pcie_2inst_nf
Current state	Not initialized
Design	Not yet initialized

```
1 - Type "help package name;" to view a list of Tcl commands
1 - available for the specified Quartus Prime Tcl package.
1 - Type "help -tcl" to get an overview on Quartus Prime Tcl usages.
1 *****
tcl load_package periph
tcl load_package blueprint_internal
tcl project_open -force "E:/Altera_Project/Arria10/Blueprint_LAB/Blueprint/15.1_std/ddr3_pcie_2inst_nf_Q15.1.1/ddr3_pcie_2inst_
tcl
```

Console History

BluePrint DEMO

Quartus Prime BluePrint Platform Designer (BETA) Standard Edition - E:/Altera_Project/Arria10/Blueprint_LAB/Blueprint/15.1_std/DDR3_PCIE_2inst_nf_Q15.1_1/DDR3_PCIE_2I...

FILE HOME ASSIGNMENTS **PLAN** REPORTS

Initialize Blueprint Write Plan File... Full Screen
Update Plan Reset Plan Copy Current View
Validate Plan

Plan View

PLAN

Open Project
Open the project and revision. (FILE tab)

Initialize Blueprint
Start the BluePrint Platform Designer planning engine. Imports your project assignments. (HOME tab)

Update Plan
Applies the project assignments to the BluePrint plan. Review project assignments for errors. (ASSIGNMENTS tab)

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Plan your design. Interactively place IP cores and other components to achieve a legal periphery floorplan. (PLAN tab)

Validate Plan
Validate your floorplan. Validation verifies that unplaced design elements can be placed to achieve a fit given the current placement and assignments. (PLAN tab)

Write Plan File
Save location assignments for your floorplan to a Tcl file to incorporate back into your design. (HOME tab)

Property	Value
Quartus Prime Version	Version 15.1.0 Build 185 10/21/2015 SJ Standard Edition
Project	
Project name	DDR3_PCIE_2inst_nf
Revision	DDR3_PCIE_2inst_nf
Current state	Project assignments applied
Design	
IP blocks	4
Arria 10 Ex... Interfaces	synth_0lemif_0_example_design
Arria 10 Ex... Interfaces	synth_1lemif_0_example_design
Arria 10 H... CI Express	g3x8_1ldut
Arria 10 H... CI Express	g3x8_0ldut
Total periphery cells	2188
Placed	17 (0.777%)
Unplaced	2171 (99.2%)
Total top-level periphery cells	127
Placed	13 (10.2%)
Unplaced	114 (89.8%)

```

Fitter finished merging On-chip termination (OCT) logic blocks
34 differential I/O pins do not have complementary pins. As a result, the Fitter automatically creates the complementary pi
BluePrint initialized: elapsed time is 00:01:00
periph:update_plan
Pin ~ALTERA_DATA0~ is reserved at location AU27
Pin ~ALTERA_CLKUSR~ is reserved at location BD32
Pin ~ALTERA_CLKUSR~ was reserved for calibration. This pin must be assigned a 100-125 MHz clock.
Plan updated with currently enabled project assignments.

```

Console History

Blueprint DEMO

The screenshot displays the Quartus Prime Blueprint Platform Designer (BETA) Standard Edition interface. The main window shows a grid-based design layout with various components and connections. A red box highlights the 'Chip View' and 'Package View' buttons in the top toolbar, with a red arrow pointing to a larger inset window titled 'Views' that shows both options side-by-side.

On the left side, there is a 'Design Element Filter' and a list of design elements. The 'top' element is expanded, showing several sub-elements with their placement status:

Design Element	highligh	Placement	Legal Locations
top		Placed	
g3..._0		Unplaced	
g3..._1		Unplaced	
sy..._0		Unplaced	
sy..._1		Unplaced	
ALT...UX0		Unplaced	~4 Locations >>
ALT...UX1		Unplaced	~4 Locations >>
ALT...UX2		Unplaced	~4 Locations >>
ALT...UX3		Unplaced	~4 Locations >>
ALT...UC0		Unplaced	~2 Locations >>
ALT...UC1		Unplaced	~2 Locations >>
CL...A0		Unplaced	>10 Locati... >>
CL...A0		Unplaced	>10 Locati... >>
GCL...buf		GLO...ION	

Below the list is a 'Property' table for the selected design element:

Property	Value
Design Element	
id	2096
name	ALTERA_RESER...TED_PMA_AUX0
type	HSSI PMA AUX (HSSI_PMA_AUX)
description	HSSI_PMA_AUX
requirements	
instance name	ALTERA_RESER...TED_PMA_AUX0
entity name	ALTERA_RESER...TED_PMA_AUX0
hierarchy path	top ALTERA_R...RTED_PMA_AUX0
IP Info	
IP Parameterization	
Device Location	

At the bottom, the console log shows the following messages:

```

Fitter finished merging On-chip termination (OCT) logic blocks
34 differential I/O pins do not have complementary pins. As a result, the Fitter automatically creates the complementary pins
Blueprint initialized: elapsed time is 00:01:00
periph::update_plan
Pin ~ALTERA_DATA0~ is reserved at location AU27
Pin ~ALTERA_CLKUSR~ is reserved at location BD32
Pin ~ALTERA_CLKUSR~ was reserved for calibration. This pin must be assigned a 100-125 MHz clock.
Plan updated with currently enabled project assignments.
    
```

BluePrint DEMO

◀ 동영상

BluePrint DEMO

The screenshot displays the Quartus Prime Standard Edition interface. The main window shows a 'Compilation Report - ddr3_pcie_2inst_nf' with a 'Flow Elapsed Time' table. A red circle highlights the 'Flow Elapsed Time' table in the report, and a red arrow points from it to a larger, simplified version of the same table below. The 'Tasks' window on the left shows the compilation process, and the 'Messages' window at the bottom shows the output of the compilation.

Flow Elapsed Time (from report)

Module Name	Elapsed Time	Average Processors Used	Peak Virtual Memory	Total CPU Time (on all processors)
1 Analysis & Synthesis	00:02:09	1.7	2027 MB	00:03:48
2 Fitter	00:09:37	2.2	12771 MB	00:19:36
3 Total	00:11:46	--	--	00:23:24

Flow Elapsed Time (simplified)

	Module Name	Elapsed Time
1	Analysis & Synthesis	00:02:09
2	Fitter	00:09:37
3	Total	00:11:46

Tasks Window

Task	Time
Compile Design	
Analysis & Synthesis	00:02:46
Fitter (Place & Route)	00:09:49
Assembler (Generate progr...)	
TimeQuest Timing Analysis	
EDA Netlist Writer	
Edit Settings	
Program Device (Open Progra...)	

Messages Window

```

Type ID Message
171167 Found invalid Fitter assignments. See the Ignored Assignments panel in the Fitter Compilation Report for more information.
144001 Generated suppressed messages file E:/Altera_Project/Arria10/Blueprint_LAB/Blueprint/15.1_std/ddr3_pcie_2inst_nf_Q15.1st/output_files/ddr3_p
11793 Fitter databases successfully split.
Quartus Prime Fitter was successful. 0 errors, 292 warnings
293000 Quartus Prime Flow was successful. 0 errors, 321 warnings
    
```

Thank You

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