USB2.0/3.0 Physical Layer Test Challenges

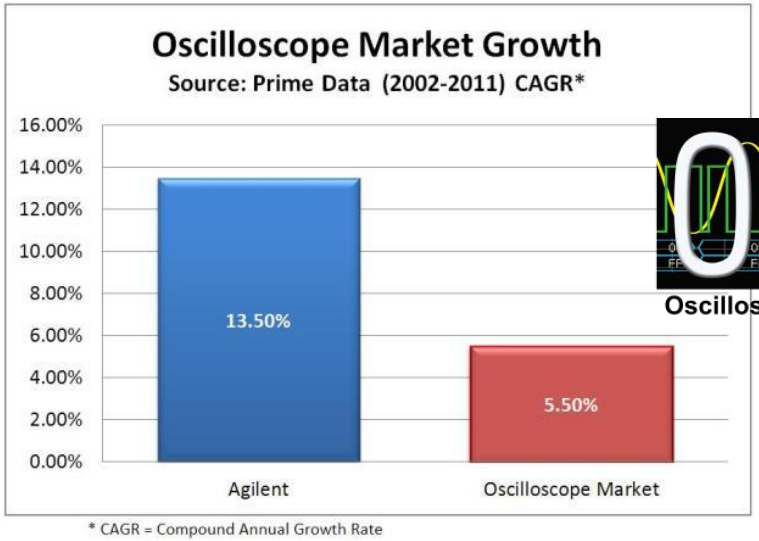
Industry and Testing Challenges Update

Jung-Chan Kim
Agilent Technologies

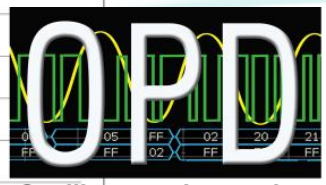
Agenda

- Overview
  - Agilent Digital Standards
  - USBIF Compliance Program Status
- Physical Layer Testing
  - USB2.0 Compliance test and low price test option(New)
  - USB3.0 Tx/Rx compliance test
  - USB Specification Updates
- Additional debug and productivity tools
- 10G SuperSpeed Overview
- USB Protocol Solution Overview
- Summary
- Questions

Agilent Oscilloscope Portfolio

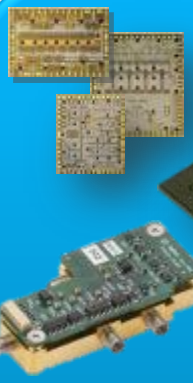


* CAGR = Compound Annual Growth Rate



Oscilloscope Innovation

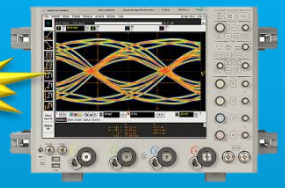
Taking Share as the Fastest Growing Scope Company



New

DCA-X Sampling

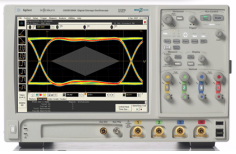
New



90000 Q-Series

Agilent custom ASIC technology designed for market leading performance

90000 X-Series

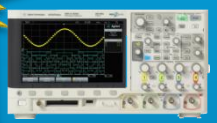


90000-Series

Agilent custom ASIC technology designed for market leading value.

New

New



New

2000 X-Series

3000 X-Series

4000 X-Series

9000-Series

Agilent Digital Standards Program

- Our solutions are driven and supported by Agilent experts involved in international standards committees:
  - Joint Electronic Devices Engineering Council (JEDEC)
  - PCI Special Interest Group (PCI-SIG®)
  - Video Electronics Standards Association (VESA)
  - Serial ATA International Organization (SATA-IO)
  - USB-Implementers Forum (USB-IF)
  - Mobile Industry Processor Interface (MIPI) Alliance
  - And many others
- We're active in standards meetings, workshops, plugfests, and seminars

  .
- We get involved so you benefit with the right solutions when you need them

We understand your future requirements, because we help shape them

Rick Eads
PCI-Sig Board Member

Brian Fetz
DisplayPort Phy CTS Editor
VESA Board Member

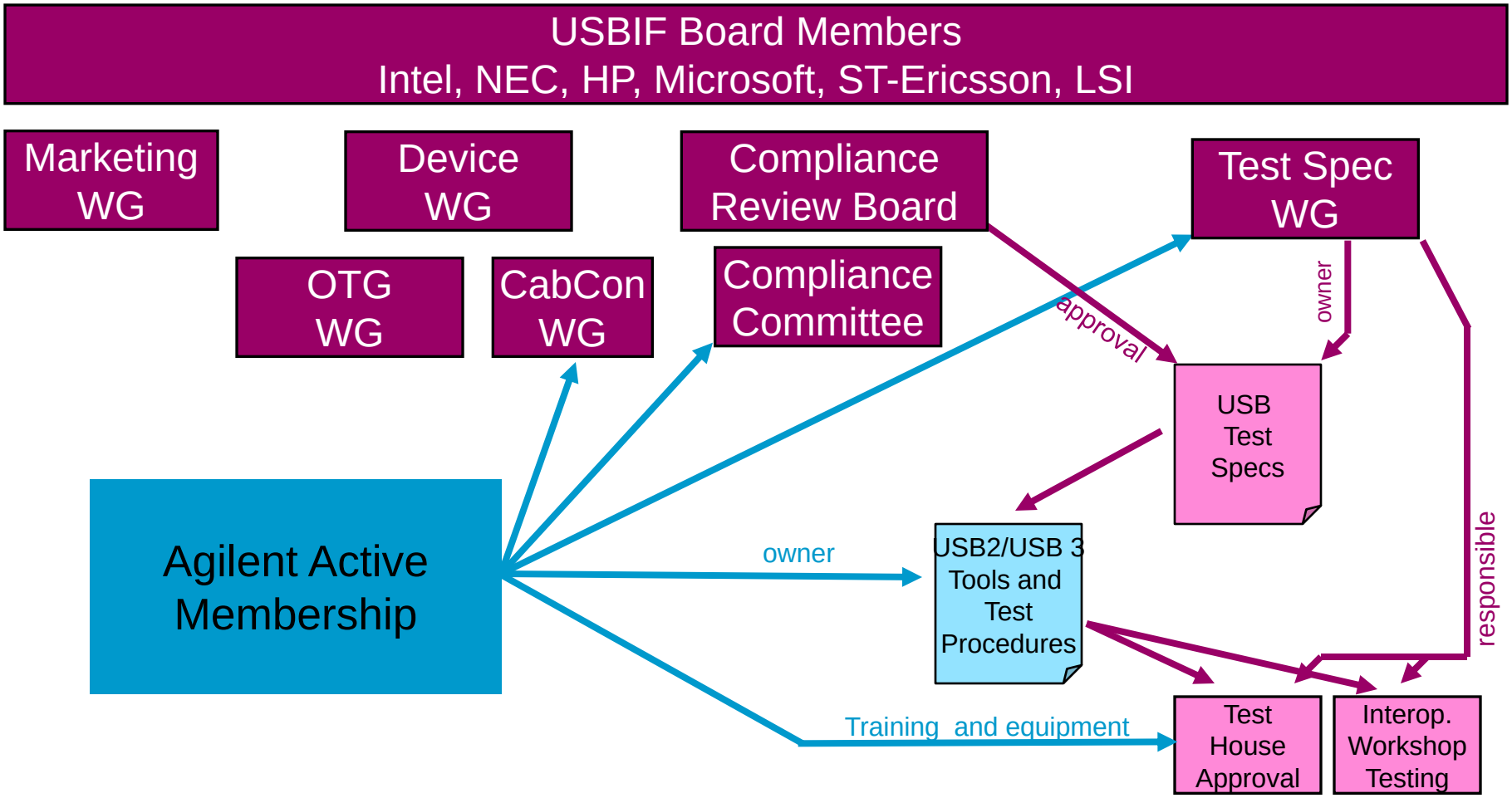
Jim Choate
USB-IF Compliance Committee
USB 3.0 Electrical Test Spec WG

Min-Jie Chong
SATA 6G / PHY / LOGO Contributor
SATA-IO Gold Suite Lead

Perry Keller
JEDEC Board Member

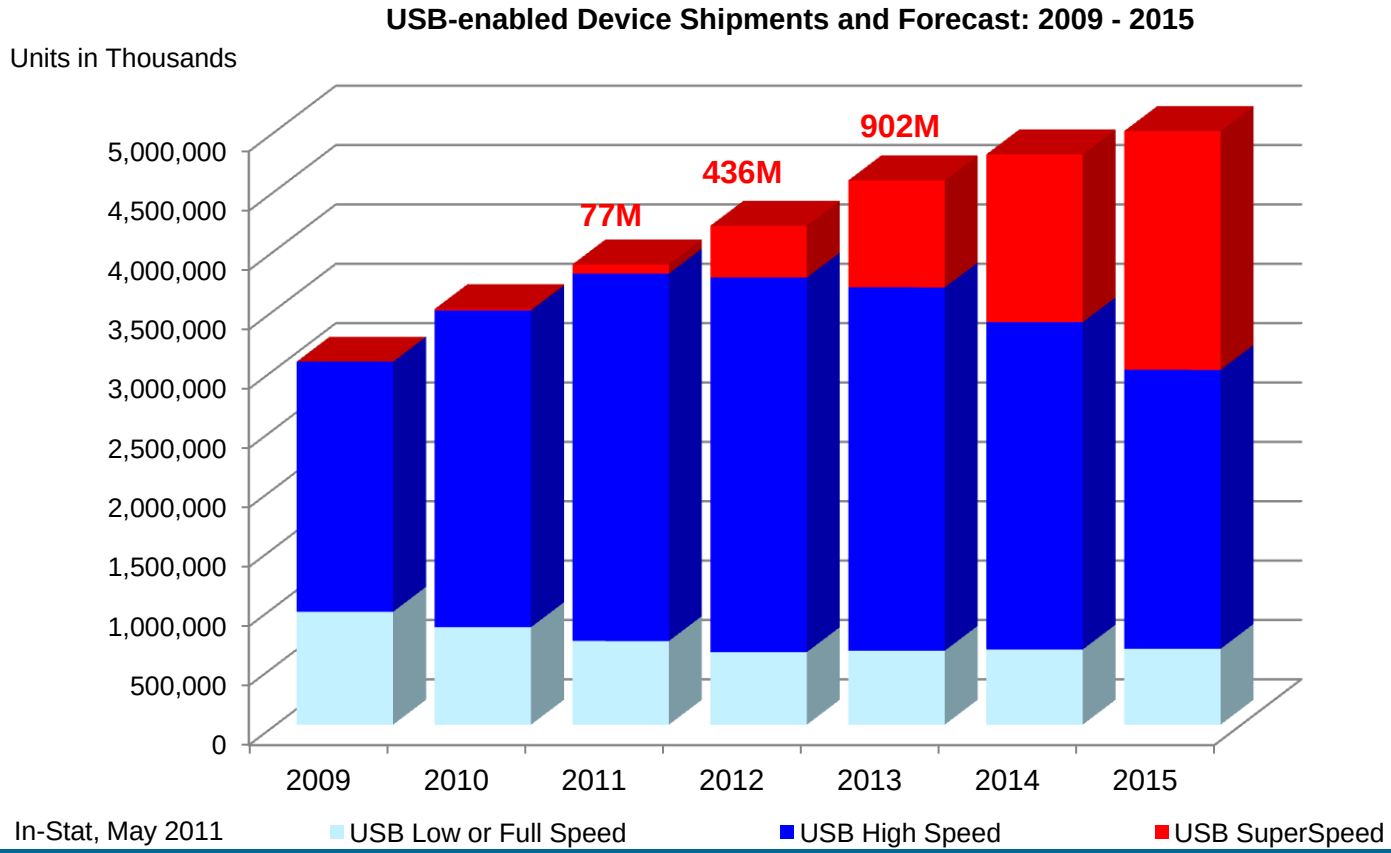
The Agilent Infiniium Scopes team maintains engagement in the top high tech standards organizations

USB Implementers Forum, inc (USB-IF)



Worldwide Shipment of USB-enabled Devices

- USB is the most successful interface in the history of PC
- Device charging over USB has become a major consumer feature
- USB installed base is 10+ billion units and growing at 3+ billion units a year
- Adoption is virtually 100% in PC and peripheral categories



Source: In-Stat, May 2011

Agilent USB Workshop Testing solutions

USB 3.0 Electrical Gold Suite

Tx Testing
•DSA91304A/X Oscilloscopes

RX Testing
•N4903B J-BERT
•N4916A/B D-box

Protocol Testing

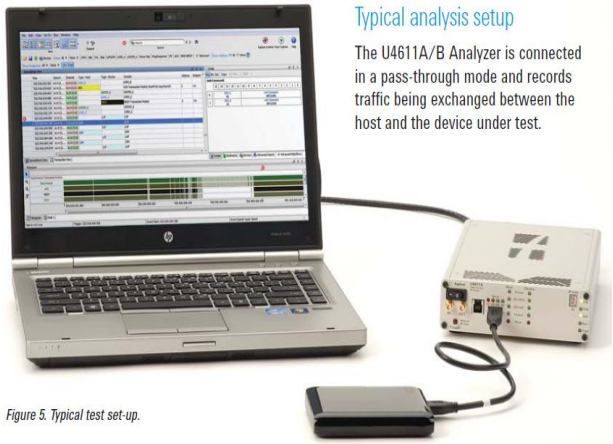


Figure 5. Typical test set-up.

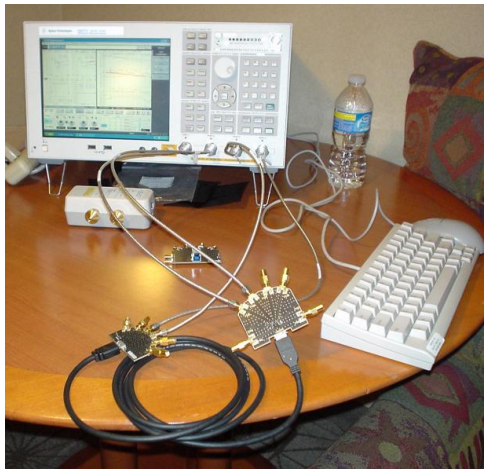
Test and debug Interop issues, Backward compatibility, software and firmware

USB 2.0 Electrical Gold Suite

Tx Testing
•DSA9254A

RX Testing
•81134A or 81130A

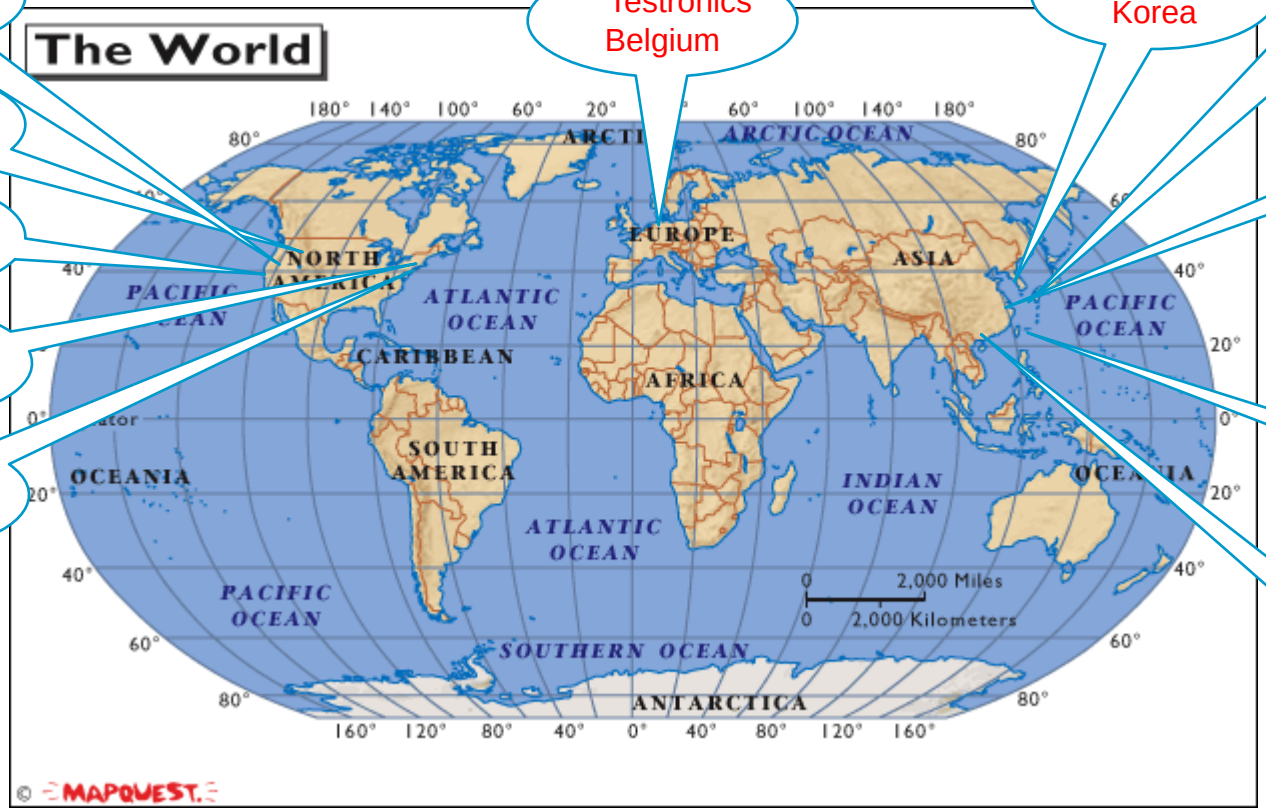
ENA TDR Cable Testing



ENA 5071C with option TDR

Informational
•Cable Testing
•Connector Testing
•Device, hub and host testing

Agilent is the USB2 and USB3 leading solution provider to test labs worldwide



GRL USA

Allion USA

NTS USA

NSTL USA

MCCI USA

Testronics Belgium

TTA Korea

Allion Japan Shanghai Taiwan

XXCAL Japan

SGS Taiwan

Hong Kong STC

*Test Labs Currently Qualified for USB 3.0 Certification

Approved labs are listed at http://www.usb.org/developers/compliance/labs

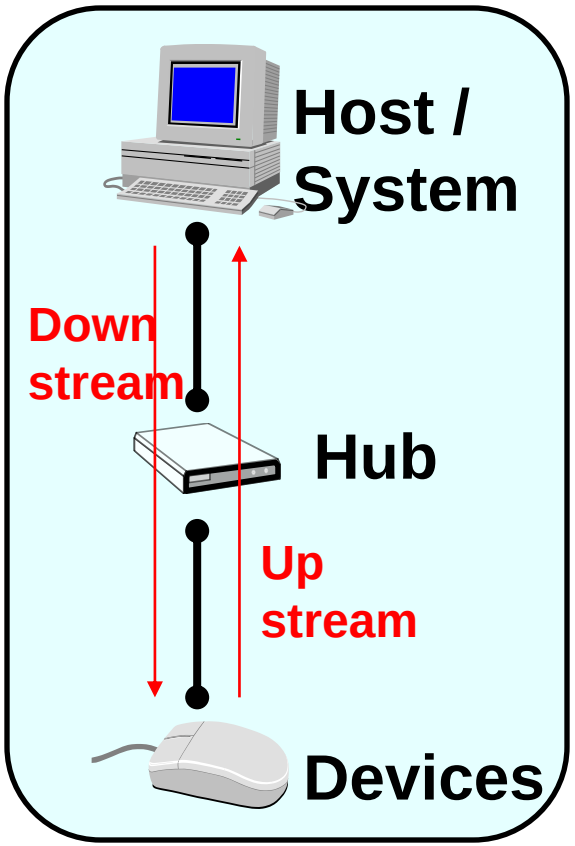
USB Protocol History

USB Protocol	Release Data	Supported Speeds
USB 1.0	Jan 1996	Low Speed (1.5 Mbps) Full Speed (12 Mbps)
USB 1.1	Aug 1998	Fixed problems identified in 1.0, mostly relating to hubs.
USB 2.0	April 2000	High Speed (480 Mbps)
USB 3.0	Nov 2008	SuperSpeed (5.0 Gbps)

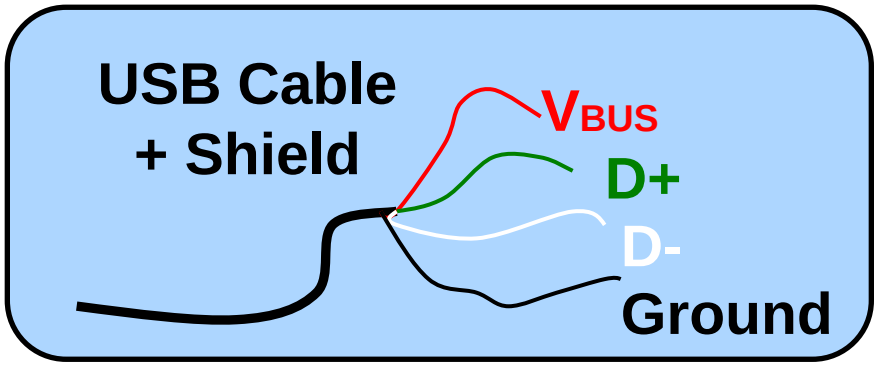
All USB specifications are backward compatible.

USB2.0 Basics - Architecture

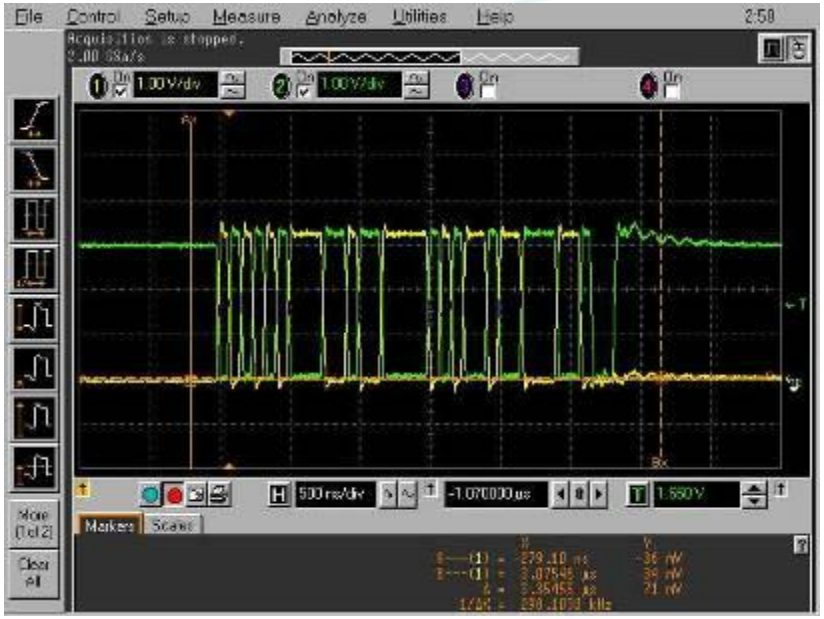
USB Architecture

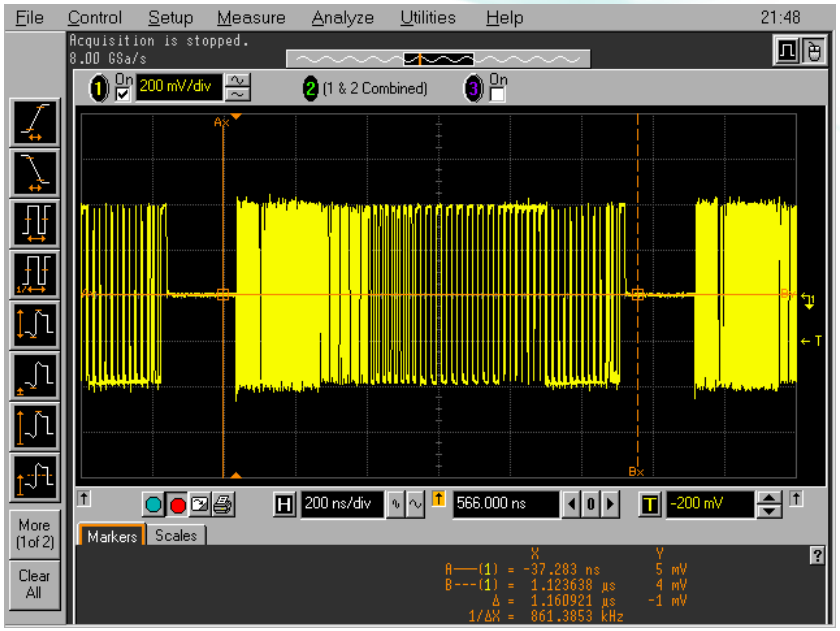


- Differential Signal
- Max USB cable length of 5m
- Up to 5 Hubs
- Data from PC to the device is called Downstream
- Data from device to PC is called Upstream



USB2.0 Basics - Signal Rates & Levels





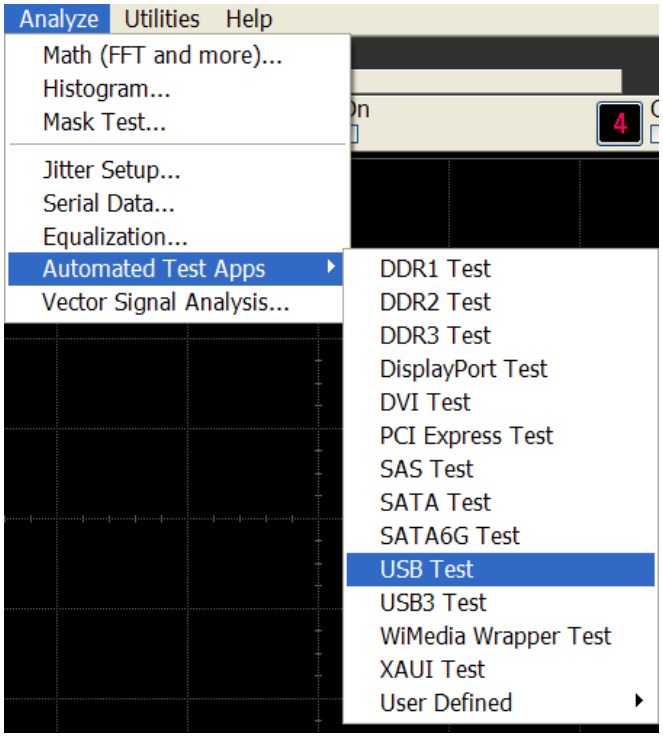
	Low Speed	Full Speed	Hi-Speed
Sig Rate	1.5Mbps	12Mbps	480Mbps
Sig Level	3.3V	3.3V	400mV
Rise and Fall Times	75ns < Tr <300ns	4ns < Tr < 20ns	Tr > 500ps*

*High Speed USB edge rate compliance measurement method and pass/fail criteria have been changed.

Agilent USB 2.0 Compliance Test Solution

Test all aspects of your USB product using Agilent USB test solutions

N5416A USB 2.0 Compliance Test Software



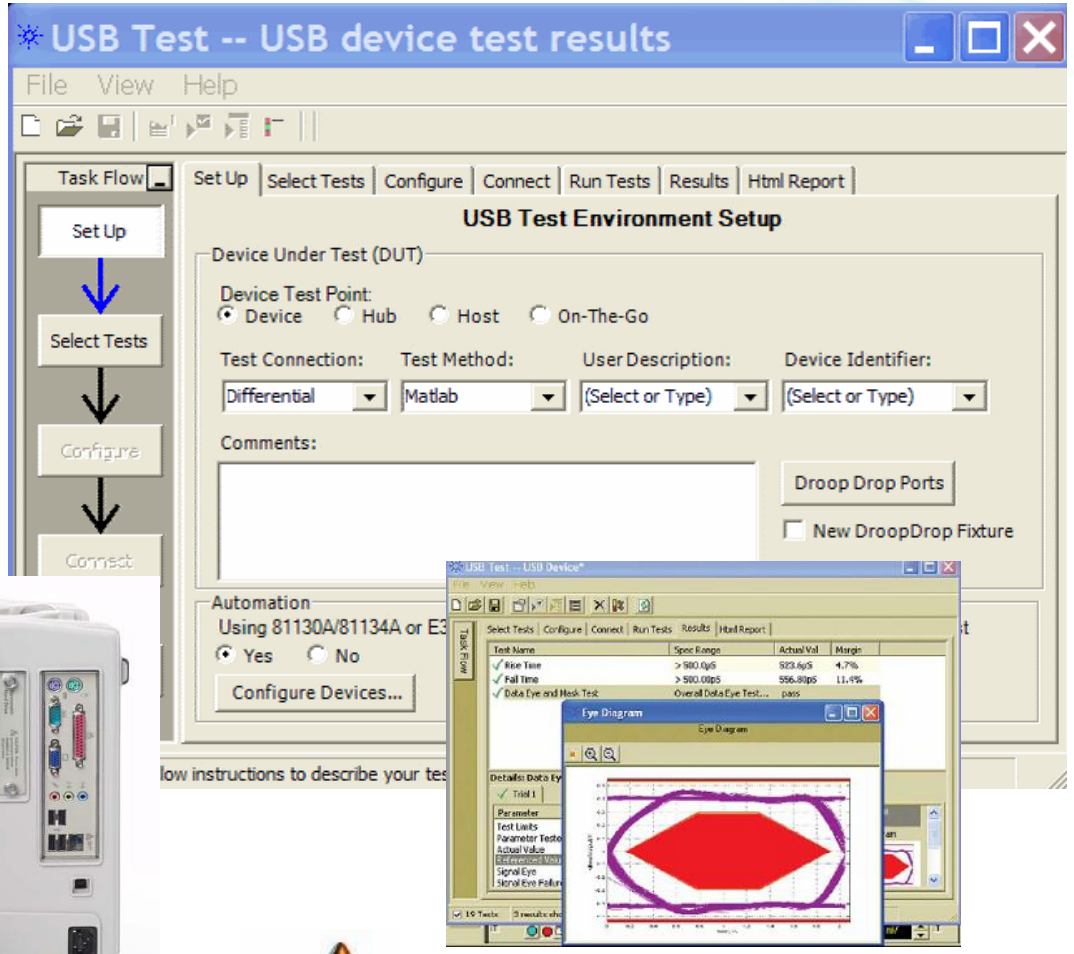
Additional USB testing products:

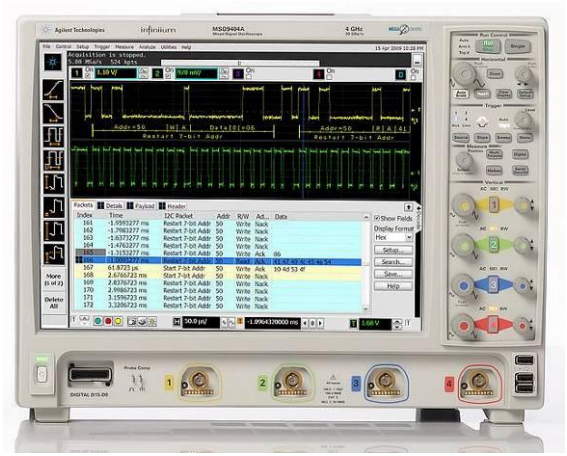
- N5464A/B USB Protocol Triggering and Decode
- N5417A USB OTG Test Fixture
- E2649A High speed test fixtures
- E2646A Low/Full speed test fixture
- InfiniiMax probes
- Infiniium 90000 and 9000 series scopes

USB2.0 Transmitter Compliance Testing

- Same automation and ease of use
- Protocol analysis and triggering

N5416A USB 2.0 Compliance Test Application

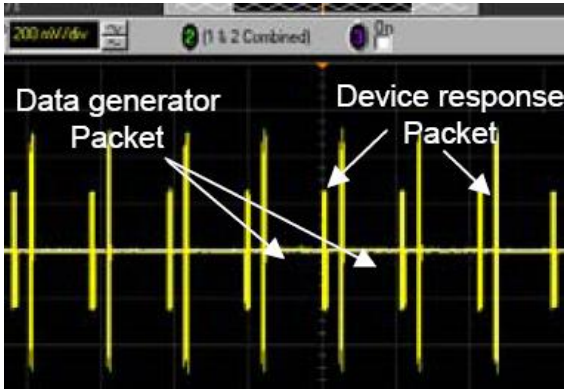




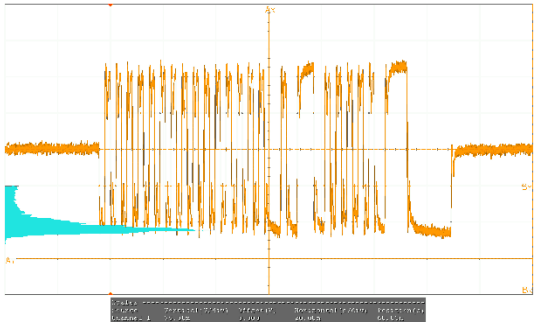
gilent USB-IF approved compliance test with Matlab scripts

Receiver Sensitivity Testing

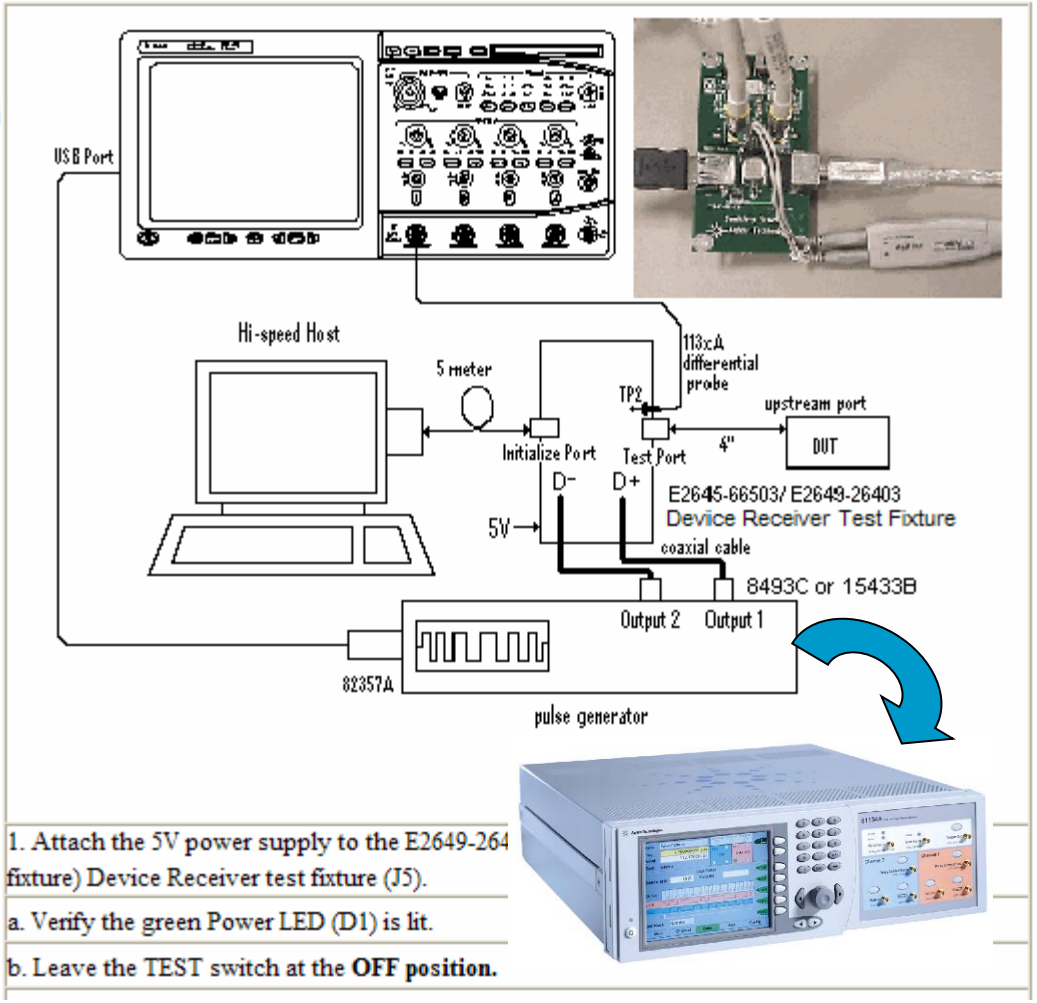
SE0_NAK Mode



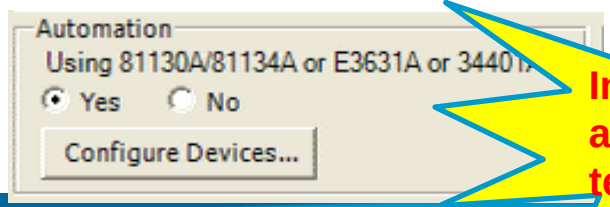
- Test mode SW places DUT into RX test mode
- Scope application auto adjusts amplitude and packet types to test RX



- N5416A USB test application measures results automatically with histogram



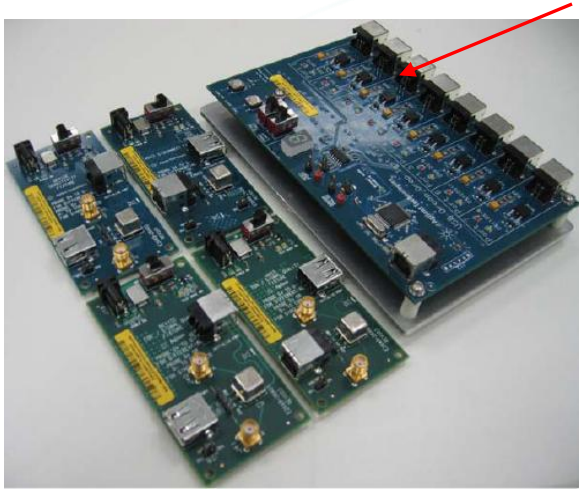
Connection diagrams and integrated test procedures make setup and execution of testing simple



Industries only automated RX test solution

Completing the Solution: Fixtures and probing

Automated drop/droop

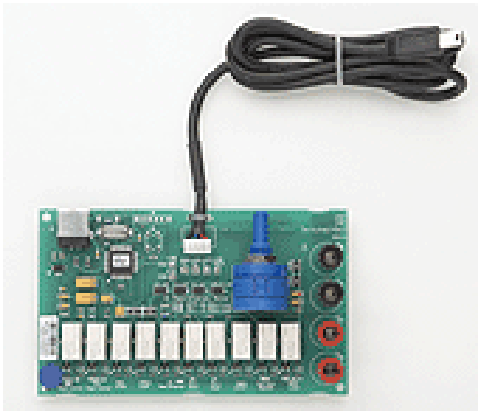


E2649B High speed USB compliance test fixture set

InfiniiMax Differential Probes:
- The world's best probing system
- The right BW for the job

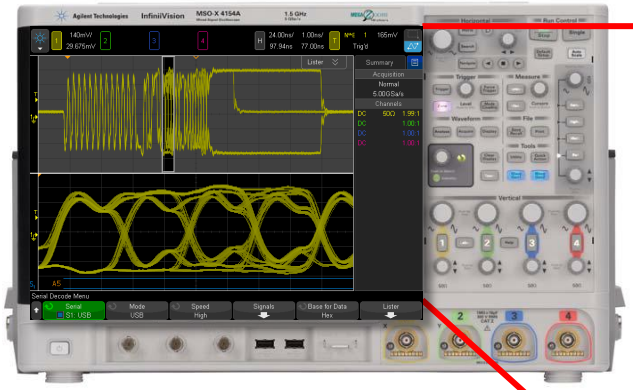
For 9000 Series scopes which support 1M ohm input

E2646A SQiDD fixture
- FS/LS Signal quality, Inrush

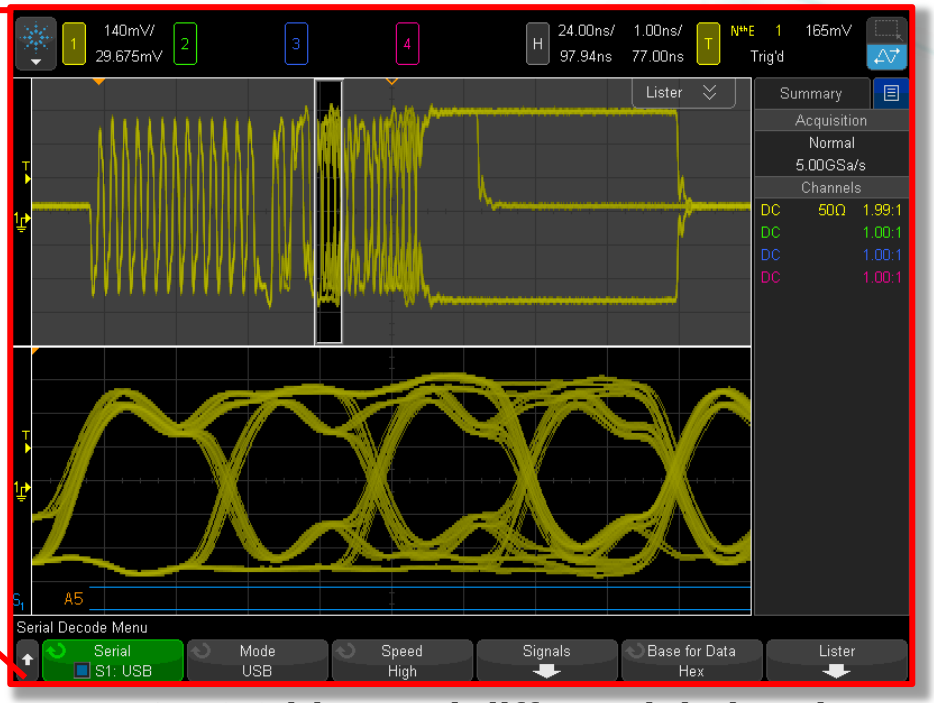


N5417A USB OET

Industry's Lowest-Priced USB 2.0 Test Option



InfiniiVision 4000 X-Series



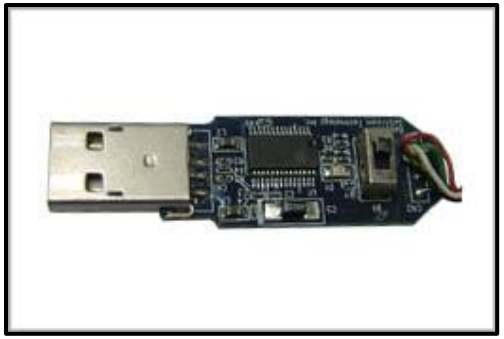
USB 2.0 hi-speed differential signal

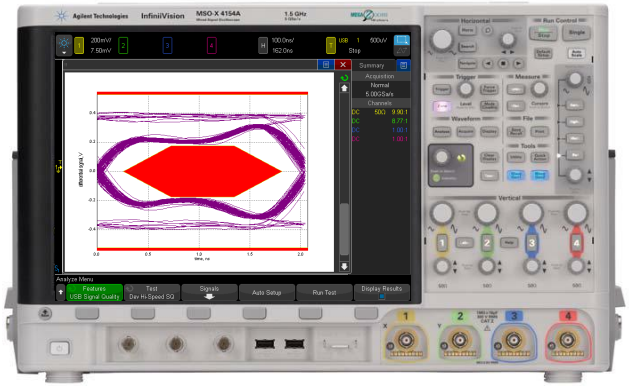
A licensed measurement option that performs a series of automated signal quality pass/fail tests on low-speed, full-speed, and hi-speed USB 2.0 differential signals.

What does it do?

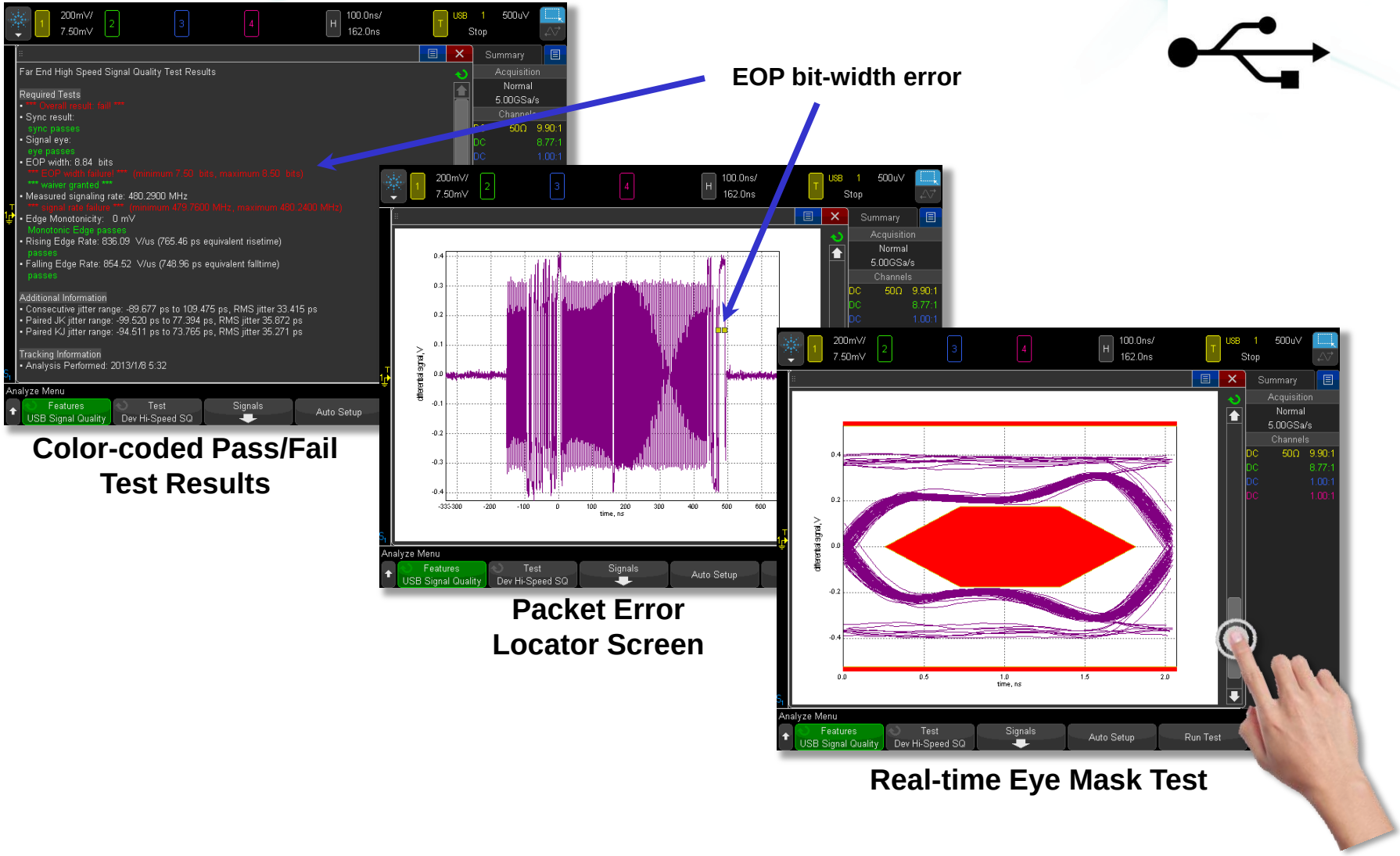
Performs the following pass/fail tests on USB hosts and devices based on USB-IF physical layer compliance standards:

- **Real-time Eye Test**
- **Consecutive, Paired JK, and Paired KJ Jitter**
- **Sync Test**
- **Cross-over Voltage (low- & full-speed only)**
- **EOP Bit-width**
- **Signaling Rate**
- **Edge Monotonicity**
- **Rise/Fall Edge Rate**
- **Edge Rate Match (low- & full-speed only)**
- **HTML Pass/Fail Report Generation**





What do test results look like?

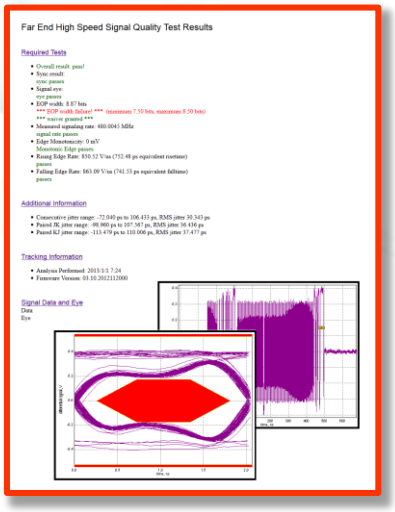


Color-coded Pass/Fail Test Results

Packet Error Locator Screen

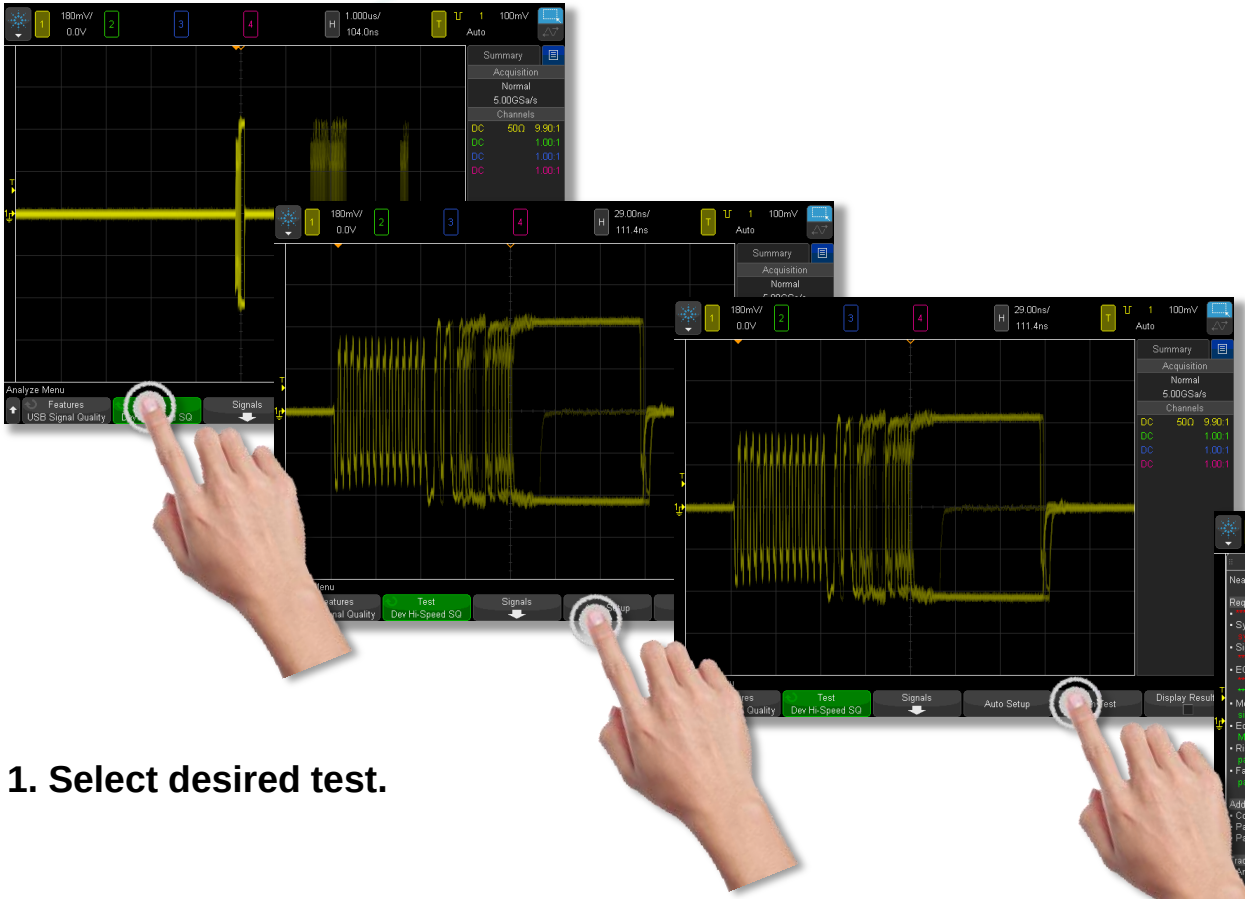
Real-time Eye Mask Test

How easy is it to use?



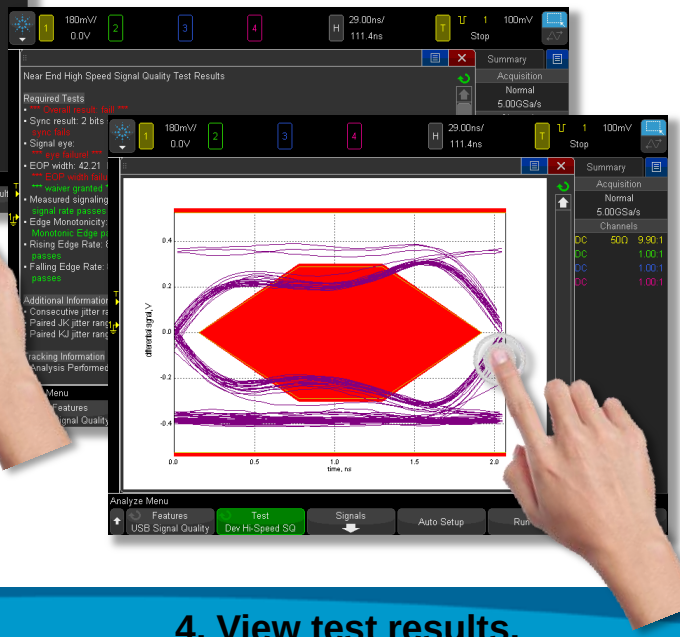
Test Report

-HTML and BMP



1. Select desired test.

2. Press “Auto Setup”.



3. Press “Run Test”.

4. View test results.

Who needs it?

1. ***Hardware designers of embedded products with USB 2.0 interfaces (USB-IF compliance certification typically not required).***

   Embedded hardware designers often need to characterize their designs based on USB-IF standards as a "reality check" to insure reliable operation.

2. ***Hardware designers of USB 2.0 hosts, devices, and hubs in the traditional computer/peripheral industry (USB-IF compliance testing and certification typically is required).***

   The DSOX4USBSQ option provides a more affordable test solution so that engineers can perform pre-compliance testing prior to attending a USB-IF compliance workshop for certification testing.

What are they doing now?

If purchasing a complete suite of USB 2.0 pre-compliance test equipment is cost prohibitive…

Embedded Designs:

1. ***If it functions, then ship it.***

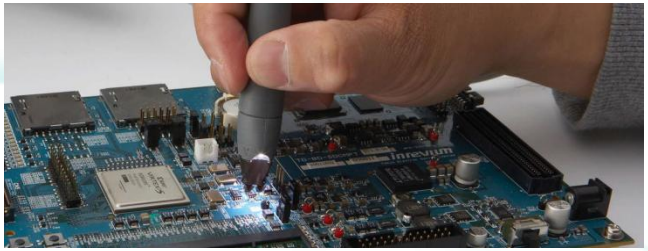
   But it might be functioning unreliably!

Computer/Peripheral Designs:

1. ***Test at a USB-IF compliance workshop with the assistance of oscilloscope vendors.***
2. ***If it fails, then return to the lab bench.***
3. ***Begin a trial & error debug process to fix the issues.***
4. ***Test again at the next USB-IF compliance workshop.***
5. ***Hope that it passes the next time!***

What else is required?

To perform non-compliance testing on "live traffic"…



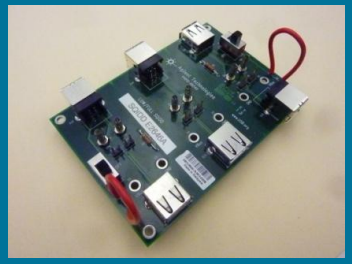
For low- & full-speed applications, just two 10:1 passive probes are required (ships as standard accessories with the scope).

For hi-speed applications, a differential active probe is required. Agilent recommends the N2750A InfiniiMode Series.

What else is required?

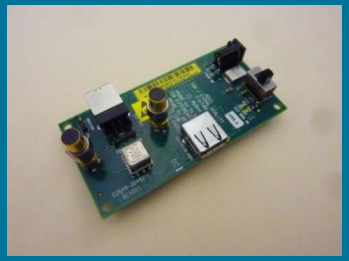
To perform testing based on USB-IF compliance standards with an input test pattern….

For low- & full-speed applications, two10:1 passive probes and the E2646B Squid" test fixture is required.



For hi-speed device applications, two SMA cables and the E2649-60001 test fixture is required.

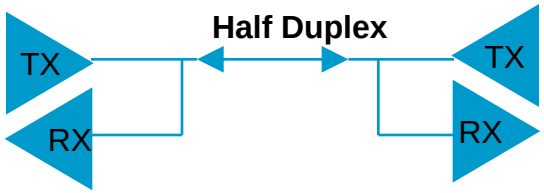
For hi-speed host applications, two SMA cables and the E2649-60002 test fixture is required.



What is different for USB 3.0

USB 2.0 High Speed

- ✓ 480Mbps
- ✓ NRZI, Half Duplex
- ✓ 4 signals
  - Dp, Dm, VCC, GND
- ✓ Cable Lmax= 5meter
- ✓ $I_{configLP/FP}$ = 100mA/500mA
- ✓ $I_{suspend}$ = 2.5mA
- ✓ No SSC
- ✓ TX SQ at Near End
- ✓ No Host RX testing



USB 3.0 SuperSpeed

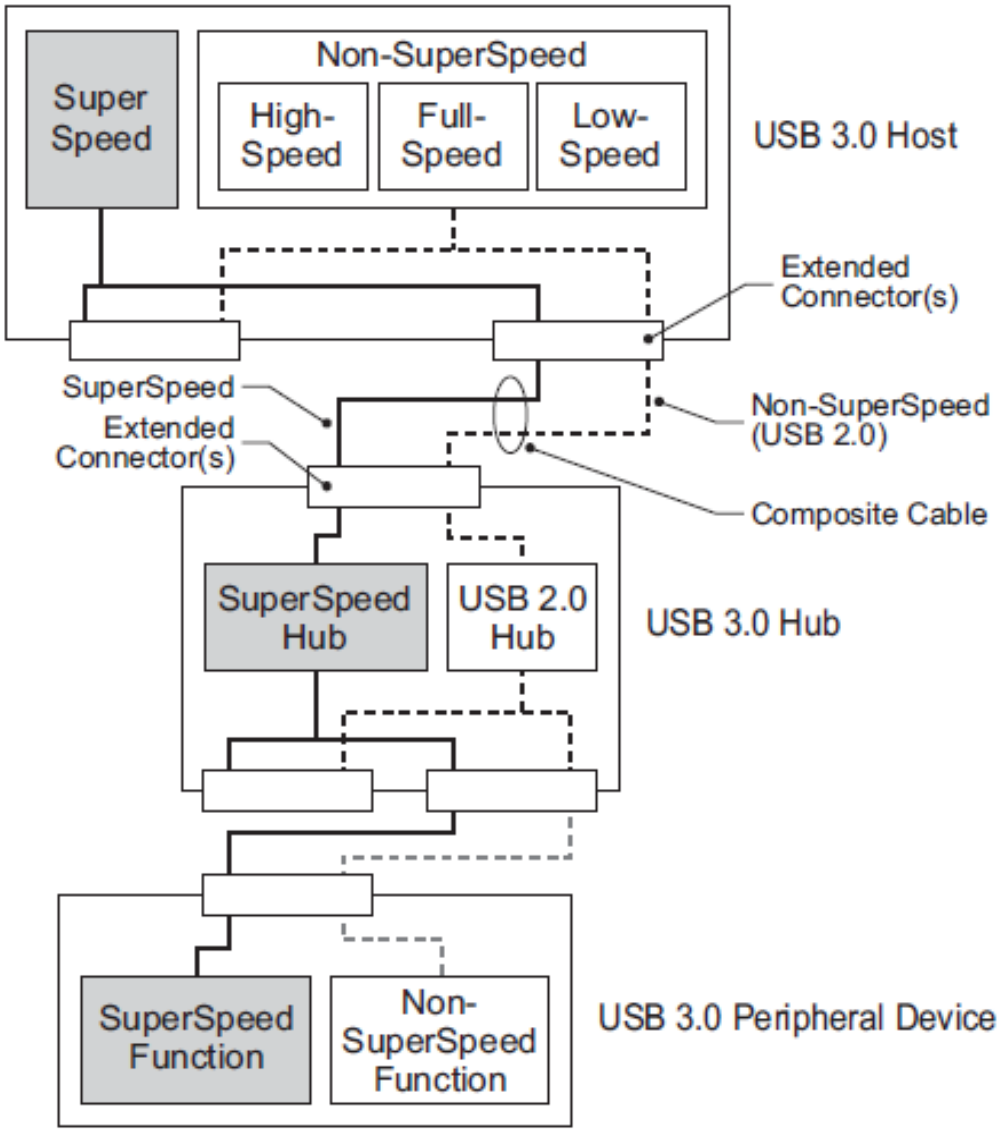
- ✓5 Gbps
- ✓8B/10B PRBS, Full Simplex
- ✓8 signals
  - 4 USB2 , 4 SS Signals
- ✓Cable L_{max}= 3 meters
- ✓$I_{configLP/FP}$ = 150mA/900mA
- ✓$I_{suspend}$ = 2.5mA
- ✓SSC (New ECN)
- ✓TX at End of Channel (Far end)
- ✓RX Jitter tolerance

USB 3.0 Bus Structure

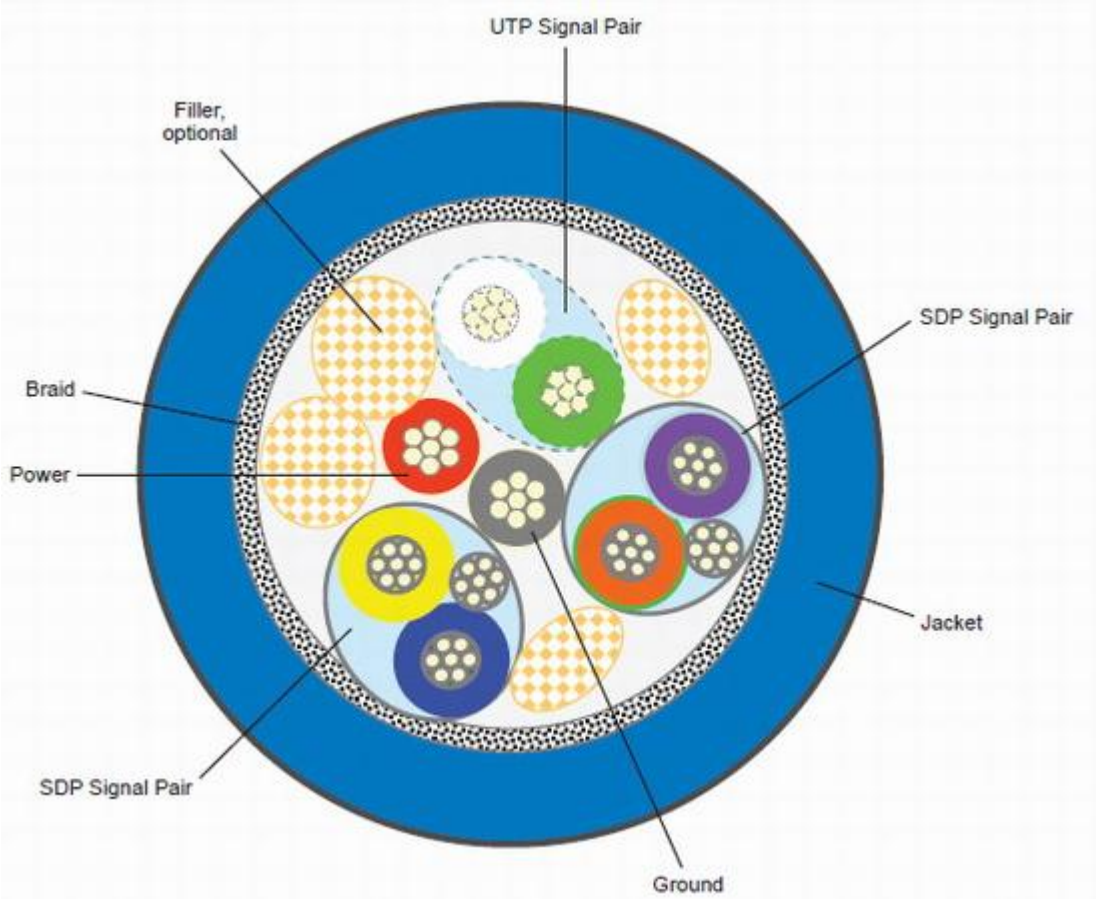
• USB 3.0 utilizes a dual Bus Architecture to provide simultaneous operation of SuperSpeed and non-SuperSpeed.

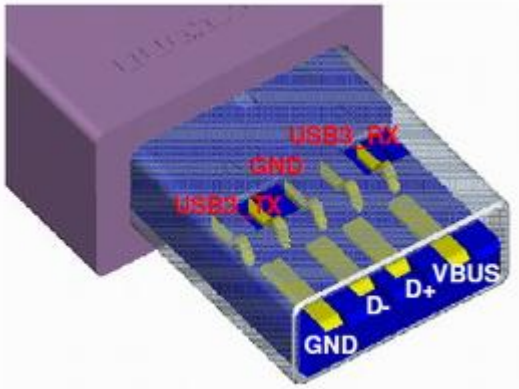
• The USB 3.0 connection model accommodates backwards and forward compatibility for connecting USB 3.0 or USB 2.0 devices into a USB 3.0 bus.

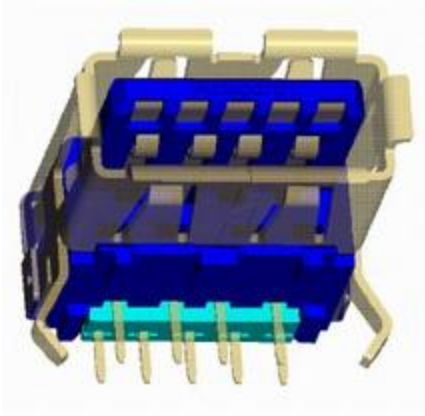
• Similarly, USB 3.0 devices can be attached to a USB 2.0 bus.



USB 3.0 Cable Structure



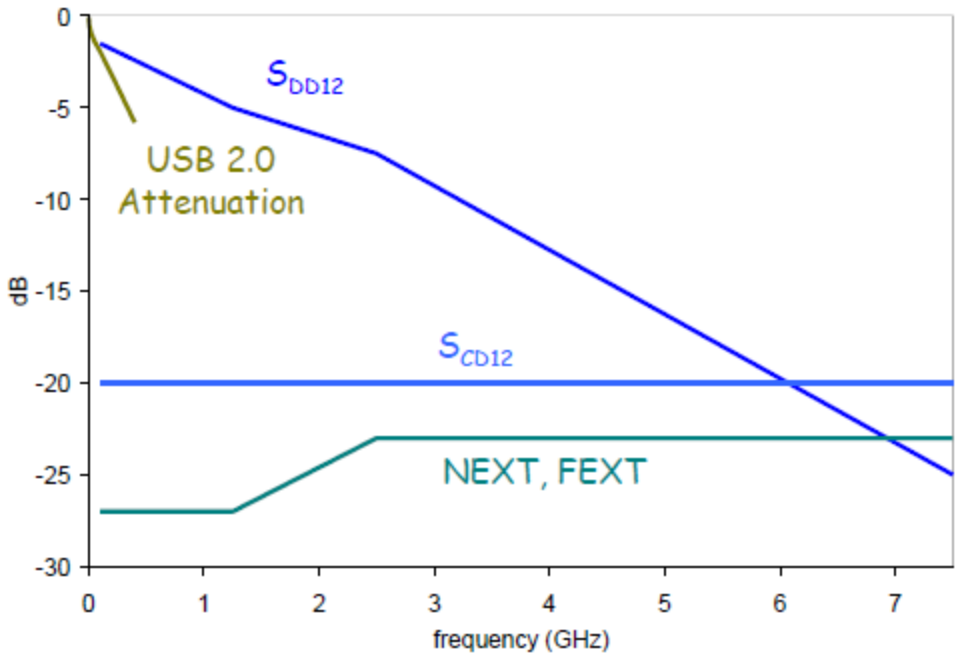




UTP : Unshielded Twist Pair

SDP : Shielded Differential Pair

USB3.0 Cable Assembly

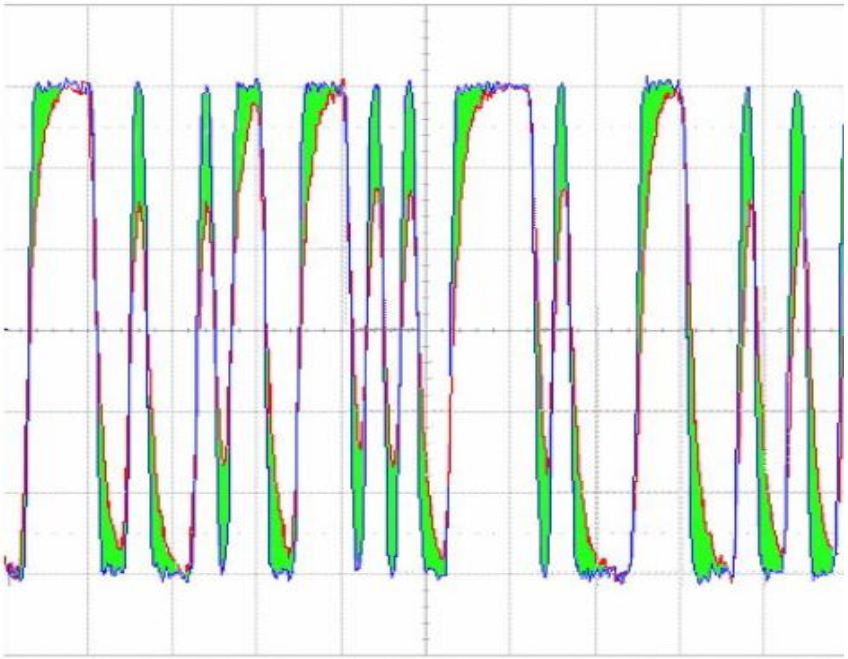


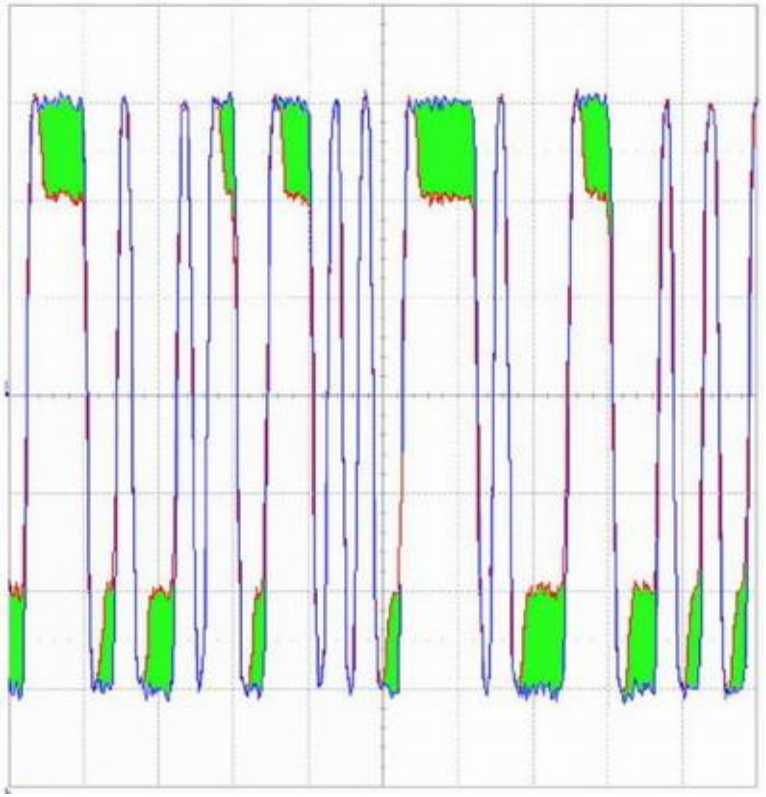
SuperSpeed USB specs:

- Attenuation (S_{DD12})
- Crosstalk (NEXT, FEXT)
- Differential-to-Common mode conversion (S_{CD12})
- Characteristic Impedance

USB 3.0 specs make sure cable assemblies support 5 Gb/s transfer rate

Transmitter De-emphasis - ISI

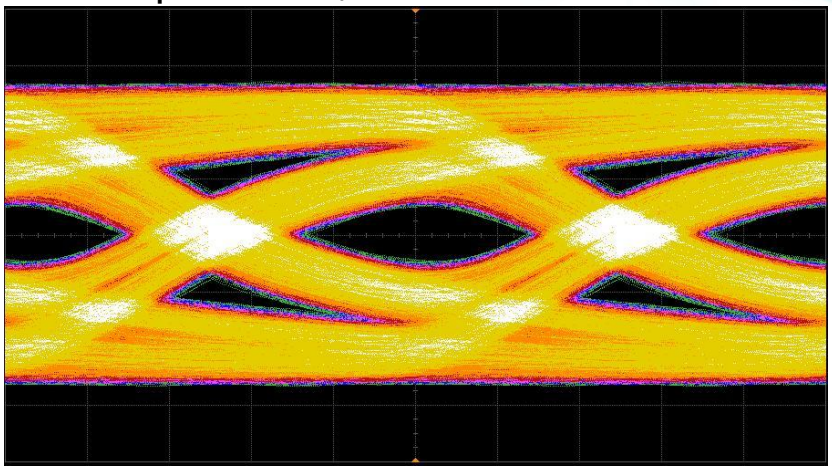




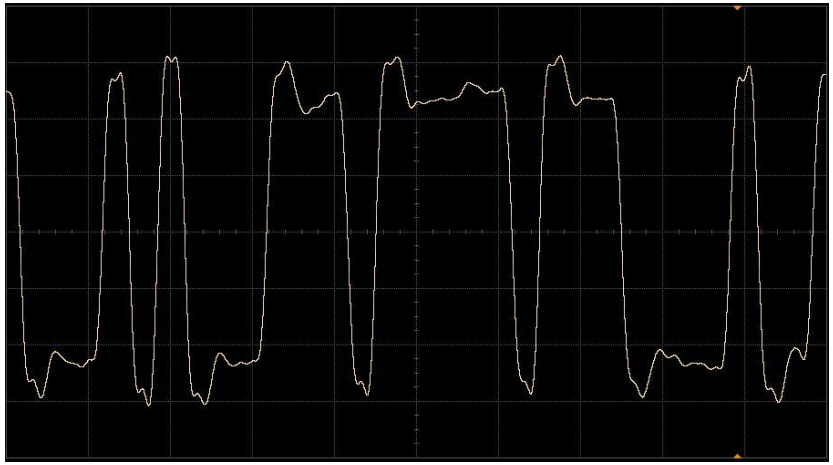
Transmitter De-emphasis

- We can account for loss through the channel at the transmitter with transmitter de-emphasis.
- De-emphasis is also called pre-emphasis.
- The amount of de-emphasis may be programmable.

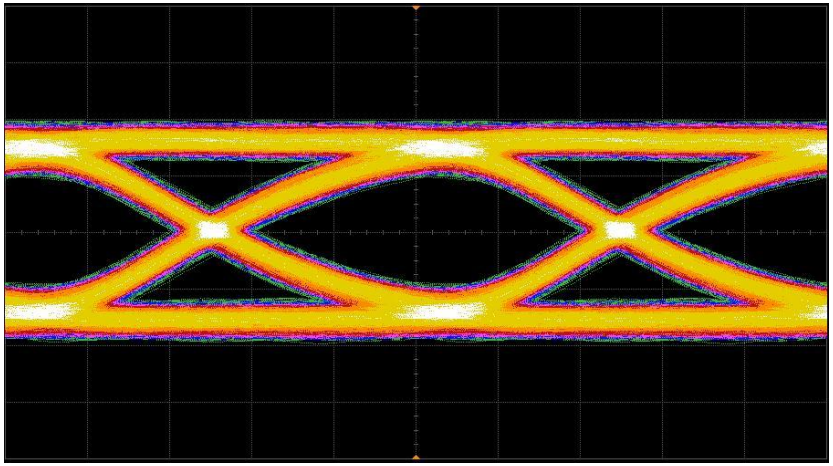
De-emphasis off, measured at receiver



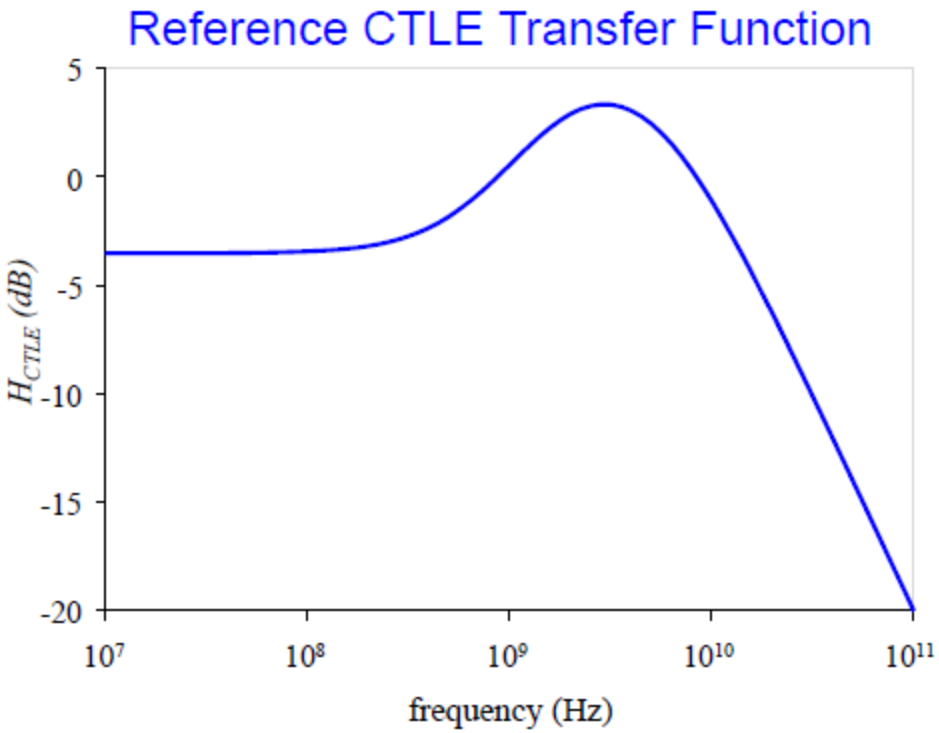
De-emphasis on, measured at transmitter



De-emphasis on, measured at receiver



Receiver Equalization



Continuous Time Linear Equalizer (CTLE)

TSEQ is transmitted 2^{16} times at initialization to allow optimization of equalizer settings

Receiver Equalization

Around 3GHz

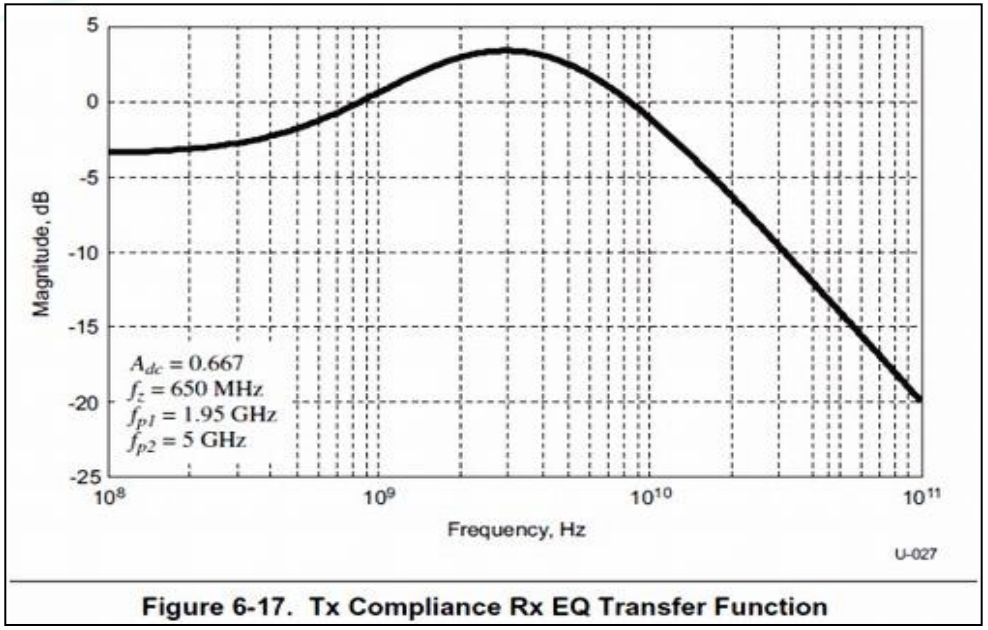
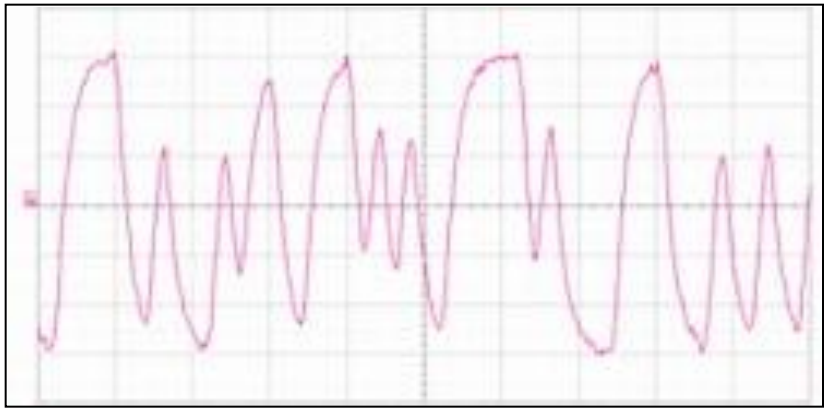
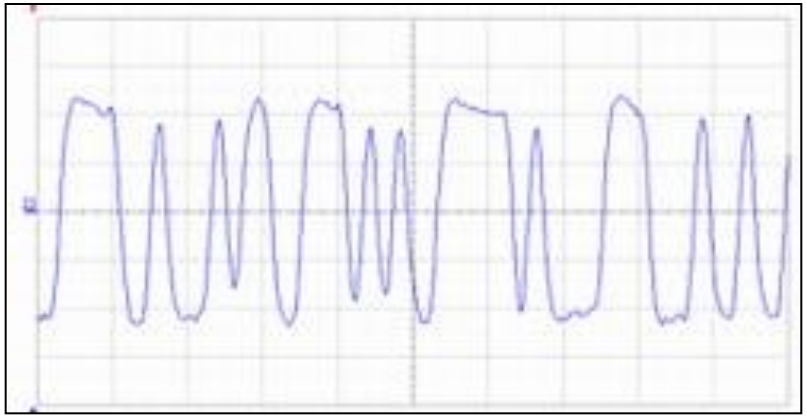


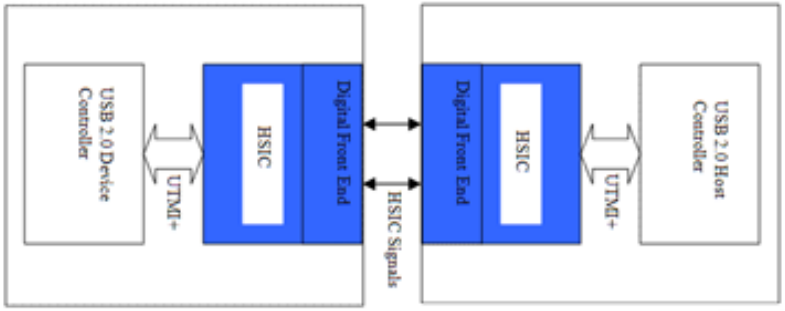
Figure 6-17. Tx Compliance Rx EQ Transfer Function





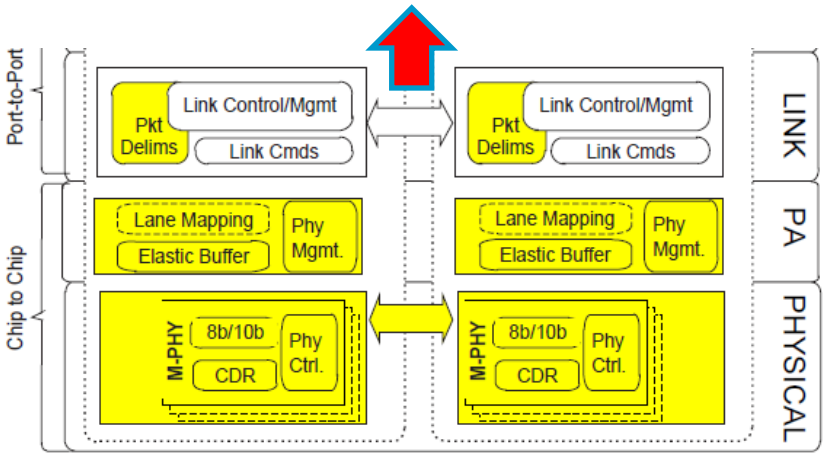
USB-IF Specification updates and additions

- HSIC – a low power USB chip to chip solution designed for mobile applications



- SSIC – USB 3.0 performance extension for chip to chip solution designed for mobile applications (download with USB 3.0 spec). Uses M-PHY for physical layer.

USB 3.0 SuperSpeed above Link Layer



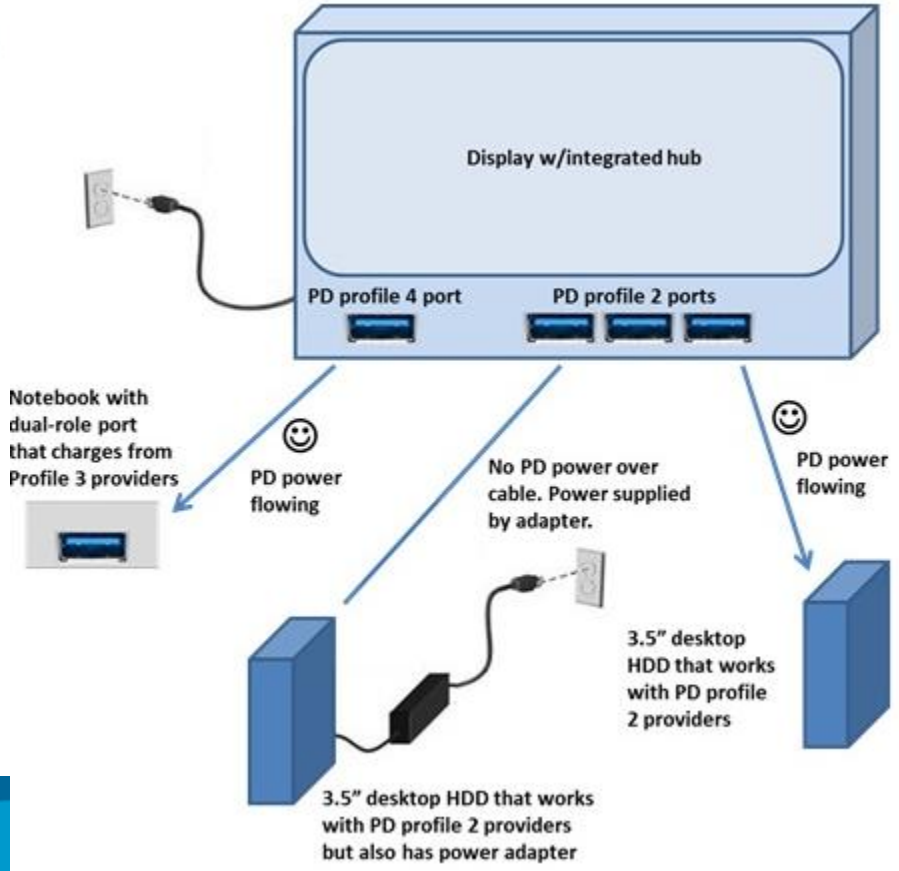
- USB Power Delivery Spec– an expansion of USB power delivery to allow more flexible power delivery up to 100W. Power direction is no longer fixed.
  http://www.usb.org/developers/powerdelivery/

- All USB-IF specifications are available at http://www.usb.org/developers/docs/

Key Features of the USB Power Delivery Spec

USB Power Delivery offers the following features:

- **Increased power levels from existing USB standards** up to 100W.
- **Power direction is no longer fixed.** This enables the product with the power (Host or Peripheral) to provide the power.
- **Optimize power management across multiple peripherals** by allowing each device to take only the power it requires, and to get more power when required for a given application.
- **Intelligent and flexible system level management of power** via optional hub communication with the PC.
- **Allows low power cases** such as headsets



USBIF – USB 3.0 Certification Test Requirements

USB 3.0 Product Test Matrix

		USB 3.0 xHCI /SuperSpeed Testing									USB 2.0 LS/FS/HS Testing			
		USBCV Chap 9 Tests	USBCV Class Tests	xHCI Host Tests	3.0 Electrical	3.0 Interop with U1/U2 enabled	3.0 Backwards Compat-ibility with U1/U2	Link Testing	SS Hub CV	Current Test Measure ment	USBCV Chap 9	USBCV Class Tests	2.0 Gold Tree Interop using EHCI	2.0 Electrical
xHCI Host	Silicon and IP	All SS Silicon	All tests, all SS silicon	Full Test Suite	✓	✓	✓	✓	n/a	n/a	All speeds	All	n/a	✓
	End Product	All SS Silicon	All tests, all SS silicon	Subset	✓	✓	✓	✓	n/a	n/a	All speeds	All	n/a	✓
USB 3.0 Devices: Silicon, IP, End Product	Device	✓	MSC UASP HID UVC PHDC OTG	n/a	✓	✓	n/a	✓	n/a	✓	Run for all 2.0 supported speeds	MSC UASP HID UVC PHDC OTG	✓	✓
	Hub	✓	Hub tests + all devices DS	SS loop-backs behind SS hub	Up-stream and down-stream ports	✓	Hub Si Only	✓	✓	✓	All speeds, all device classes DS	Hub tests + all devices DS	✓	Up-stream and down-stream ports

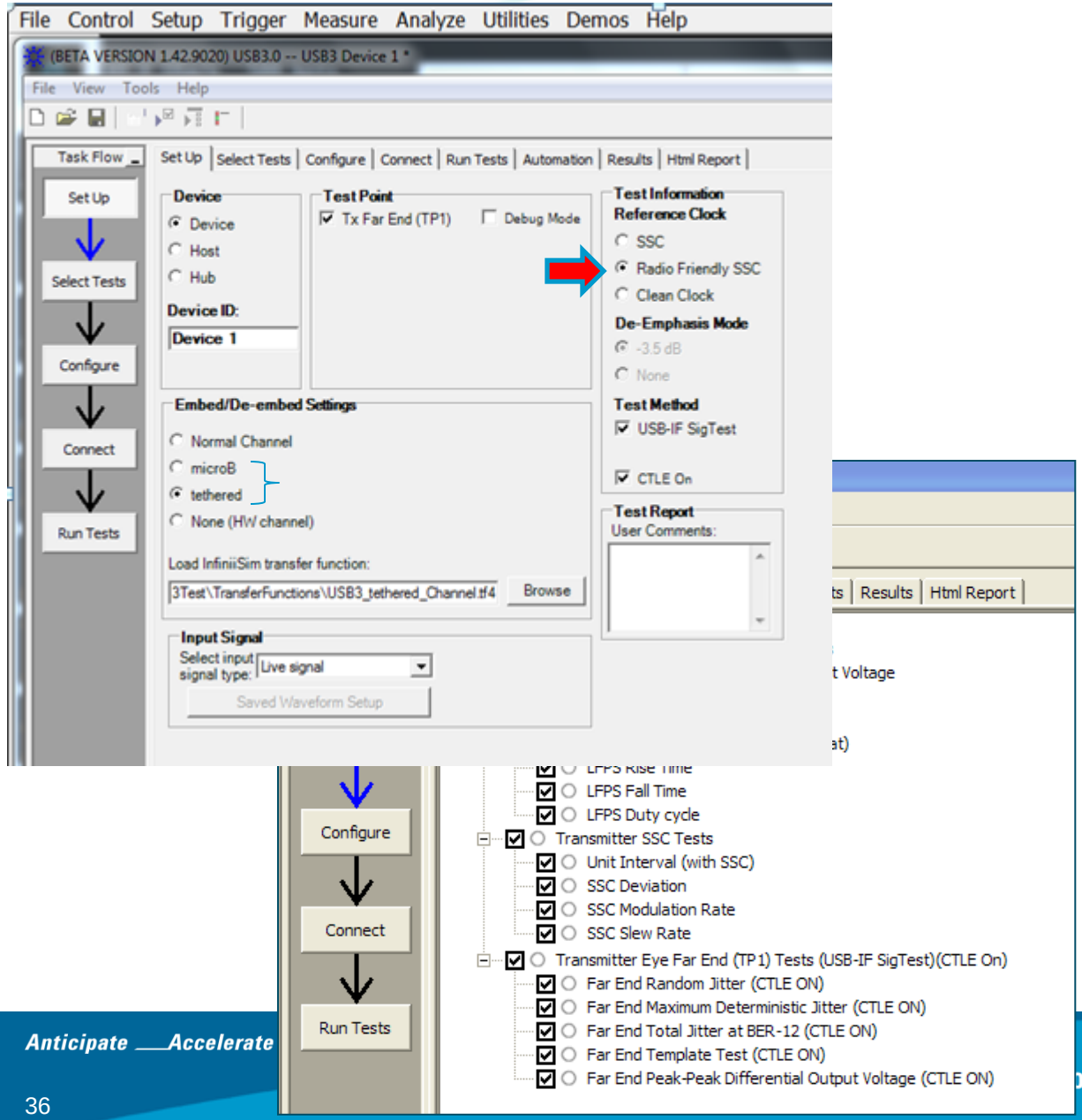
Updated 8/1/2011

Test Notes:	
	Host Si: xHCI Loopback Tests and xHCI Interface Tests. Host End Products: xHCI Interface Tests for End Products only.
	3.0 Electricals on Agilent or LeCroy or Tek using external BERT
	Backwards Compatibility includes testing 150 popular 2.0 devices for Host silicon and IP. End product will test a subset of 150
	Chapter 9 CV tests must be run at the root port for SS and also behind a SS hub.
	3.0 Hubs must have Hub TT tests run on the HS portion of the hub if the hub is not a separate, certified 2.0 hub chip.
	Current measurement with CV : unconfigured, U1, U2, U3. Current measurement with host driver stack: Operating current.
	Peripherals must pass all applicable class tests in USB30CV and USB20CV

Electrical Test Equipment and USBIF test software

Protocol Test Equipment and USBIF test software

U7243A USB 3.0 TX Compliance Application



Agilent's U7243A TX compliance test application

TX tests:
- LFPS (Near end)
- SSC (Near end)
- TX (Far End: TP1)
  - Eye Pattern
  - Tj, Rj, Dj
  - Amplitude

"Embedded channel" automatically tested using Agilent U7243A compliance software
- Normal channel
- Micro channel
- Tethered channel

Transmitter test requirements

The eye diagrams are to be measured into 50-Ω single-ended loads.

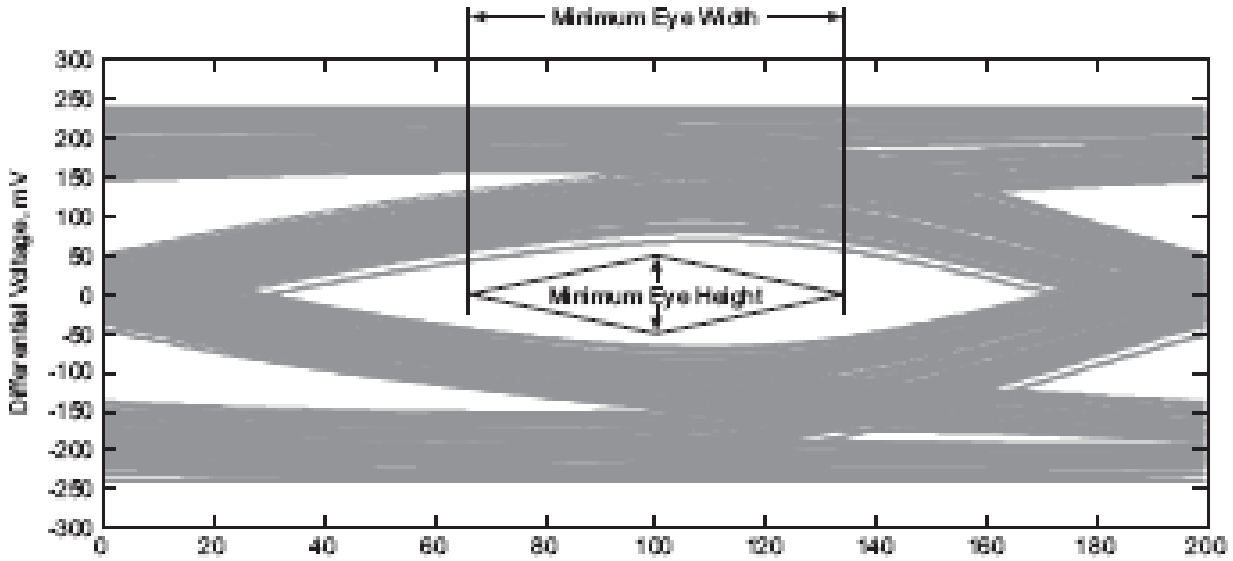
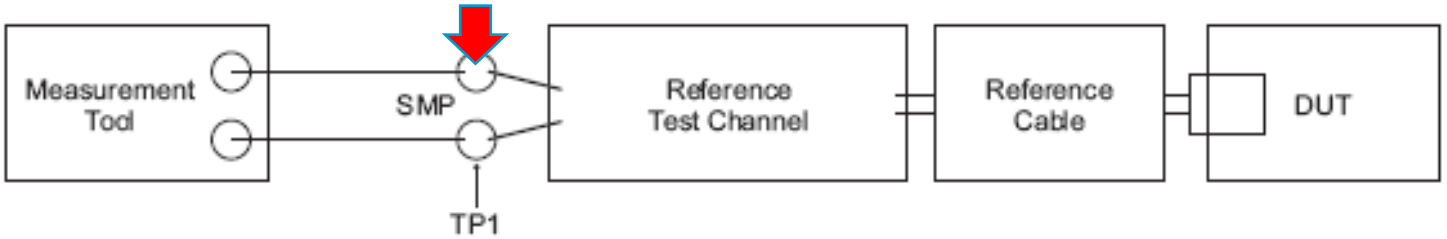


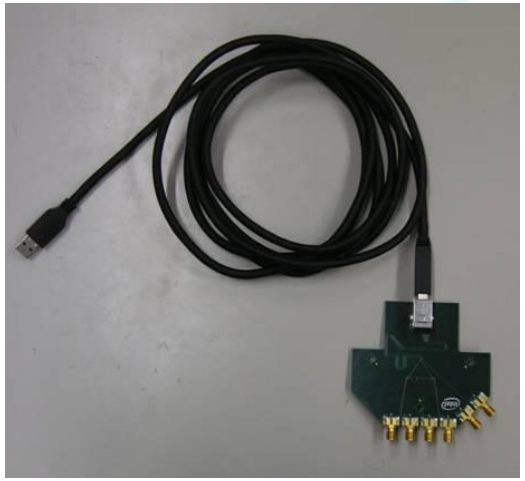
Table 6-12. Normative Transmitter Eye Mask at Test Point TP1

Signal Characteristic	Minimal	Nominal	Maximum	Units	Note
Eye Height	100		1200	mV	2, 4
Dj			0.43	UI	1,2,3
Rj			0.23	UI	1,2,3, 5
Tj			0.66	UI	1,2,3

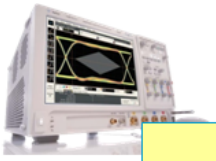
(TX Far End)



Tx testing emulated through s-parameters



Embed Channel File
"DEVICE_3MCABLE.s4p"



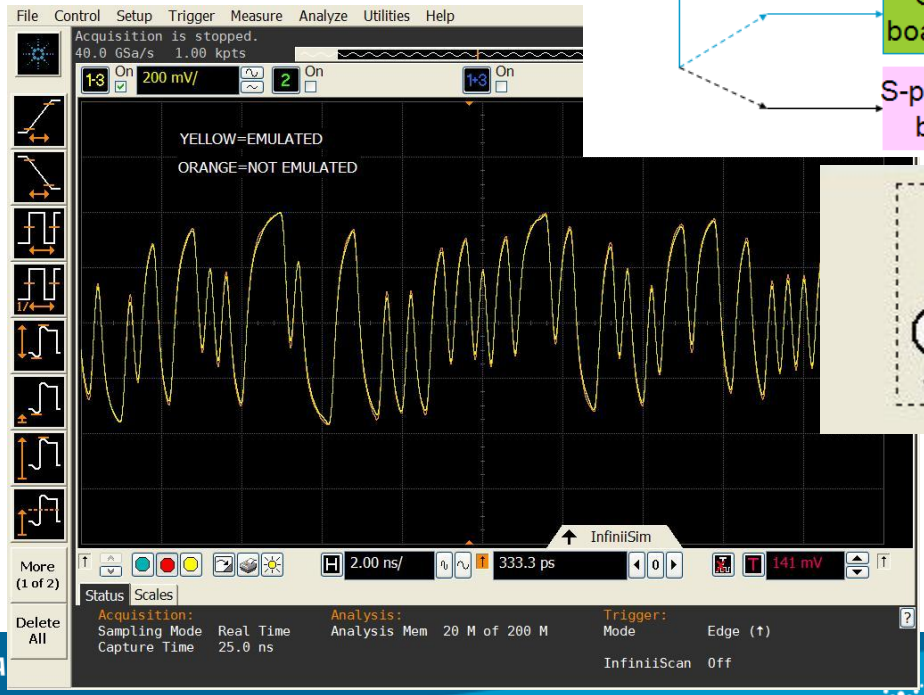
Agilent J-BERT
N4903B
5Gbps Output

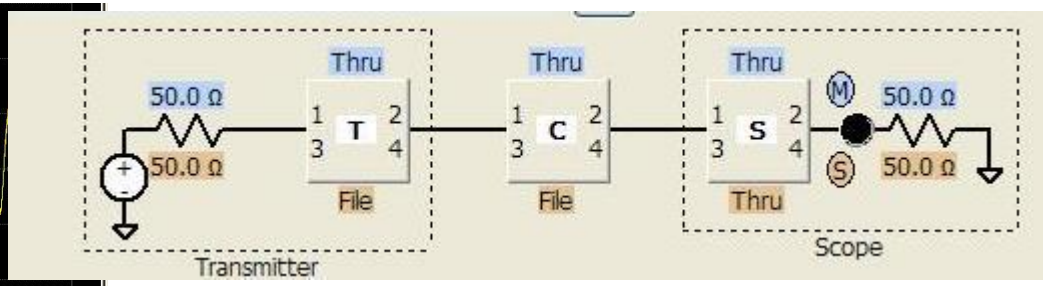
Compare!

Agilent T-Rex
DSA91304A

Compliance board and cable

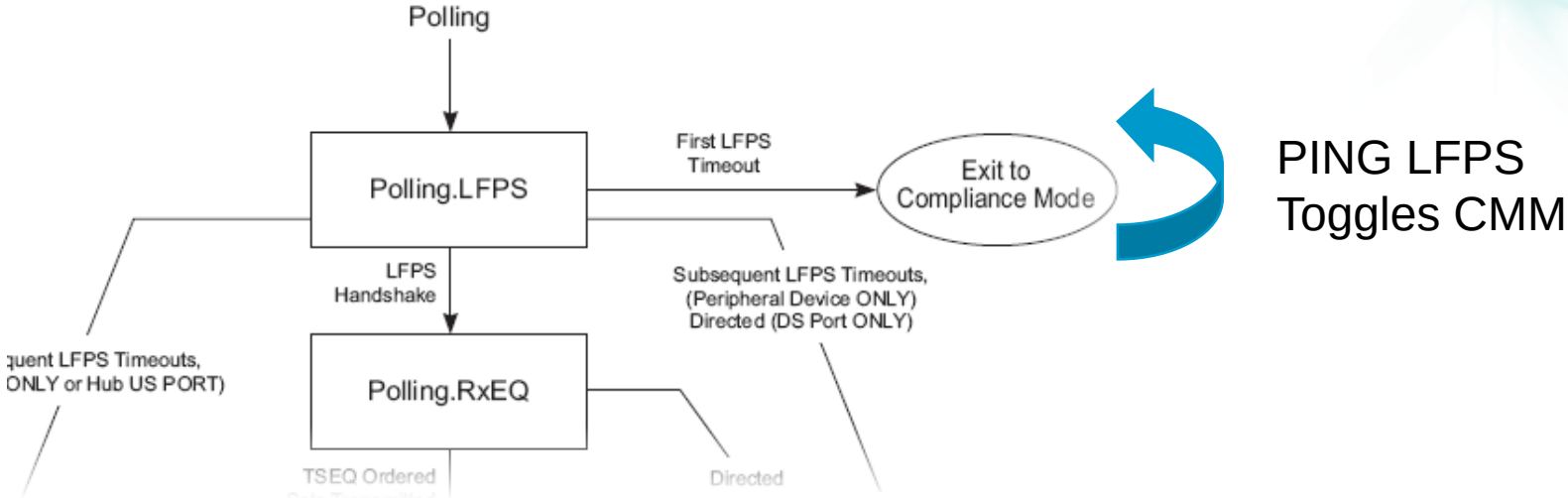
S-para Emulation by Infiniisim





Validation with InfiniiSim of DSA91304A

TX Testing Requirements: Polling.LFPS to compliance mode



PING LFPS
Toggles CMM

CP0
Dj

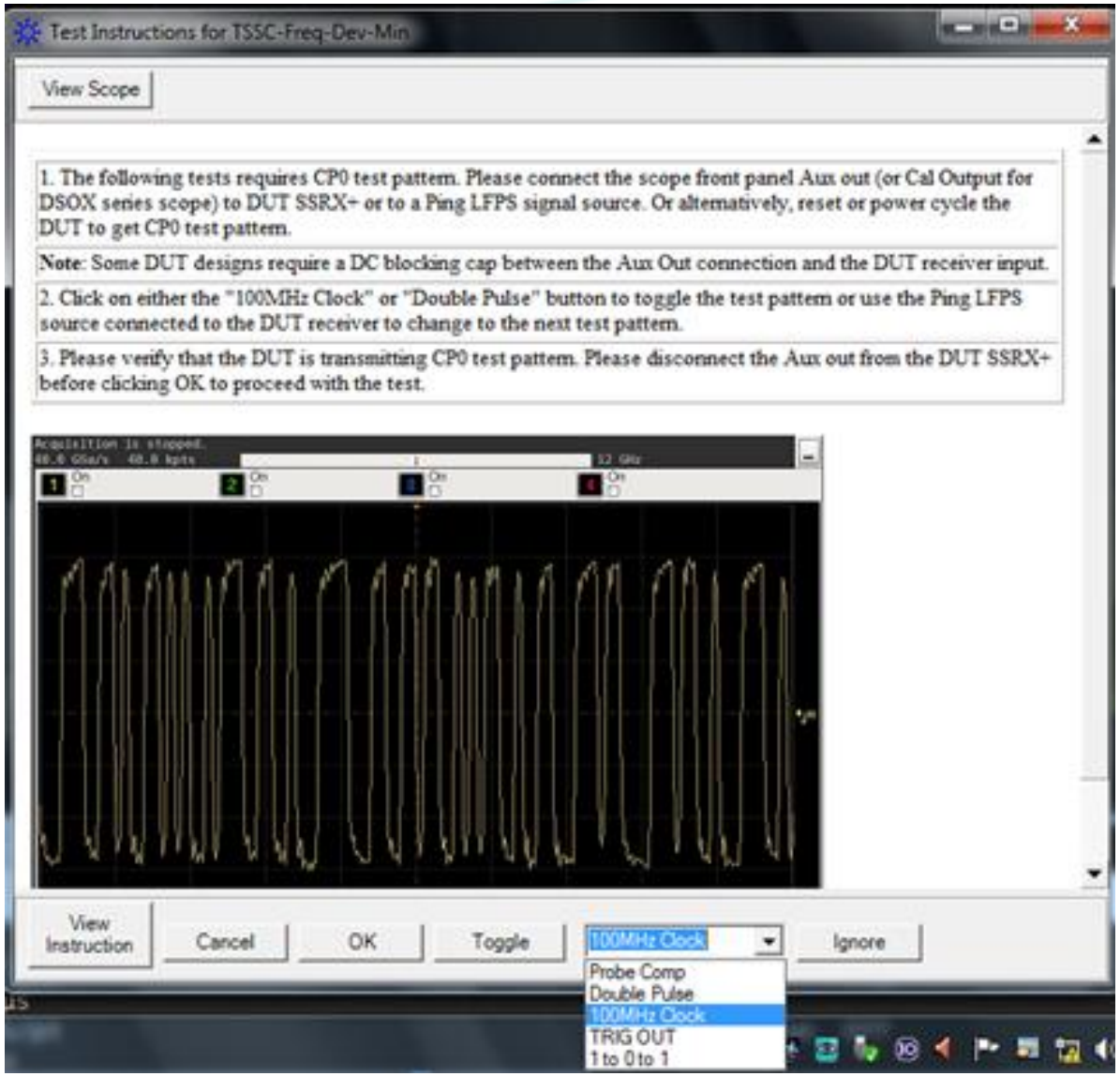
CP1
Rj

Table 6-7. Compliance Pattern Sequences

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	With without de-emphasis. Repeating 50-250 1's and then 50-250 0's.

Note: Unless otherwise noted, scrambling is disabled for compliance patterns.

Toggling USB 3.0 TX test modes



- Connect Aux Out to DUT SSRX+ to toggle test modes
- For DSOX use Cal Out

Transmitter testing uses embedded compliance channel

USB 3.0 Superspeed PHY Test Report

Overall Results: 2 of 14 Tests Failed

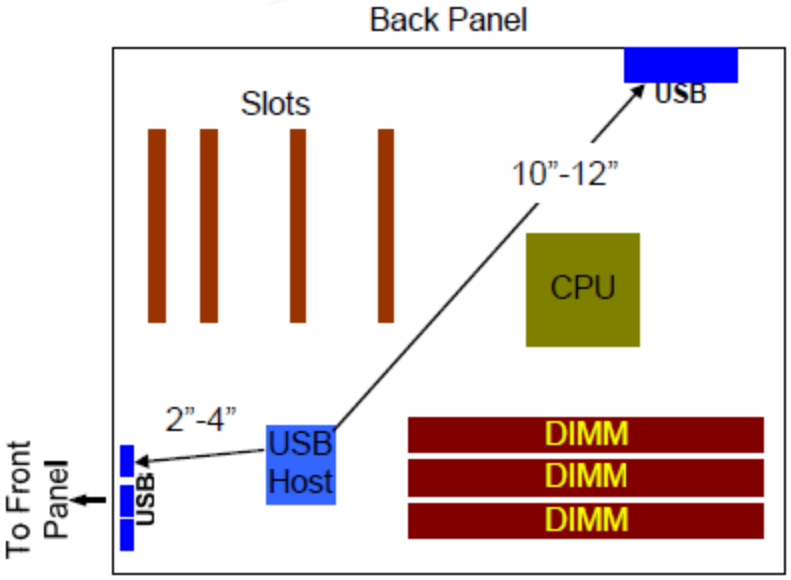
Test Configuration Details	
Device Description	
De-embed Settings	Embed
Input Signal Type	Live signal
Reference Clock	SSC
De-emphasis Mode	-3.5 dB
Device	Device
Test Session Details	
Infiniium SW Version	02.10.0004
Infiniium Model Number	DSO91304A
Infiniium Serial Number	No Serial
Application SW Version	1.19.9020
Compliance Limits (official)	USB 3.0 Specification version 1.0
Last Test Date	3/24/2010 10:08:33 AM

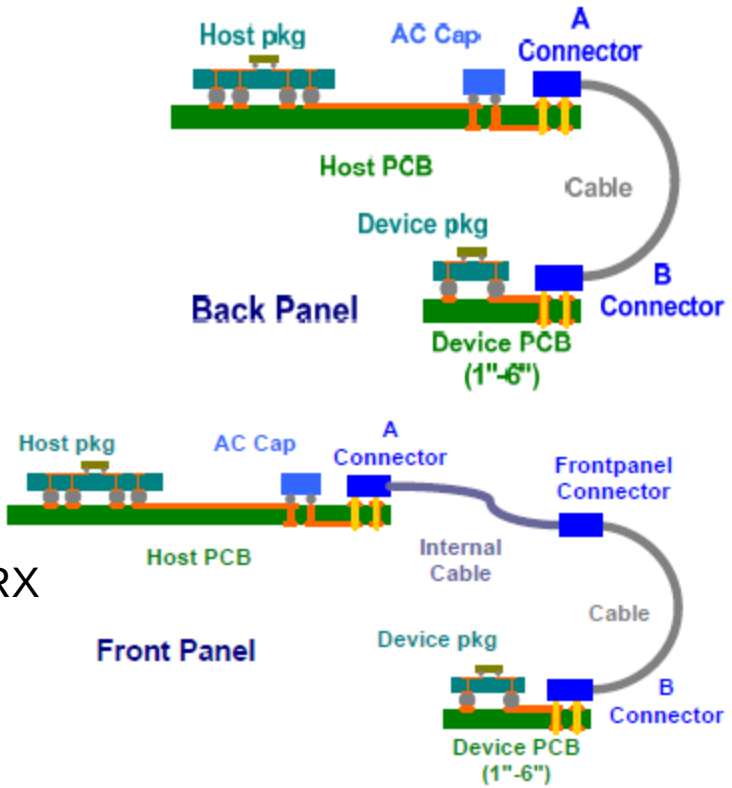
Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	LFPS Peak-Peak Differential Output Voltage	1.1022V	24.5 %	800.0mV <= VALUE <= 1.2000V
✓	0	1	LFPS Period (tPeriod)	51.1841ns	39.0 %	20.0000ns <= VALUE <= 100.0000ns
✓	0	1	LFPS Burst Width (tBurst)	1.2348µs	20.7 %	600.0ns <= VALUE <= 1.4000µs
✓	0	1	LFPS Repeat Time Interval (tRepeat)	10.2417µs	47.0 %	6.0000µs <= VALUE <= 14.0000µs
✓	0	1	LFPS Rise Time	136.3ps	96.6 %	VALUE <= 4.0000ns
✓	0	1	LFPS Fall Time	140.6ps	96.5 %	VALUE <= 4.0000ns
✓	0	1	LFPS Duty cycle	49.9876%	49.9 %	40.0000% <= VALUE <= 60.0000%
✗	1	1	Unit Interval (with SSC)	201.068ps	-0.7 %	199.940ps <= VALUE <= 201.060ps
✗	1	1	SSC Deviation	5.339964kppm	-2.5 %	3.700000kppm <= VALUE <= 5.300000kppm
✓	0	1	Far End Random Jitter	170mUI	26.1 %	VALUE <= 230mUI
✓	0	1	Far End Maximum Deterministic Jitter	302mUI	29.8 %	VALUE <= 430mUI
✓	0	1	Far End Total Jitter at BER-12	472mUI	28.5 %	VALUE <= 660mUI
✓	0	1	Far End Template Test	0.000	100.0 %	VALUE = 0.000
✓	0	1	Far End Peak-Peak Differential Output Voltage	926.9mV	24.8 %	100.0mV <= VALUE <= 1.2000V

Compliance Channel





- Compliance Channels are used to test TX and RX
- Emulating worst case channel conditions
- Back panel USB route solution
  - Channel loss will dominate
  - Host 5” of trace
  - Device 11” of trace
  - 3 meter USB 3.0 cable

Compliance Channels

Compliance Channels are used to test TX and RX for worst case channel conditions

Standard connector:

- Channel loss will dominate
- 11” PCB trace for device testing
- 5” PCB trace for host testing
- 3 meter USB 3.0 cable

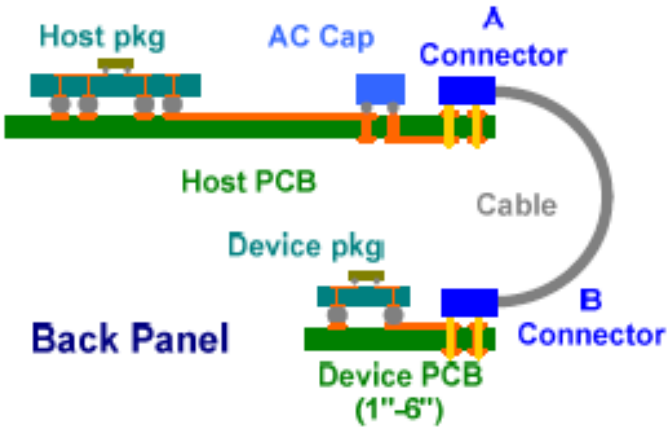
Micro connector:

- Channel loss will dominate
- 11” PCB trace for device testing
- 5” PCB trace for host testing
- 1 meter USB 3.0 cable

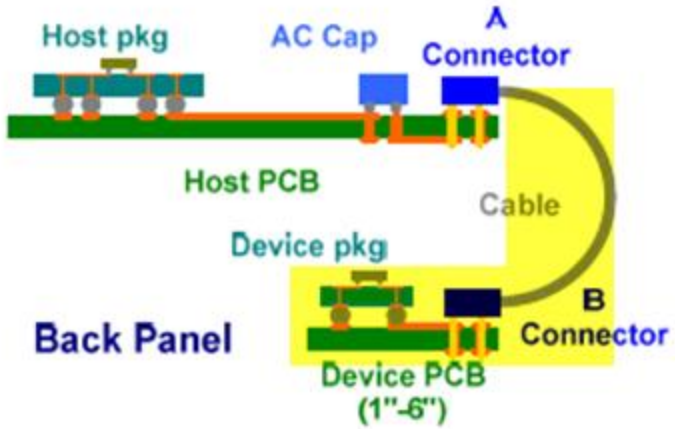
Tethered:

- Channel loss will dominate
- 11” PCB trace for device testing
- 5” PCB trace for host testing
- short USB 3.0 cable

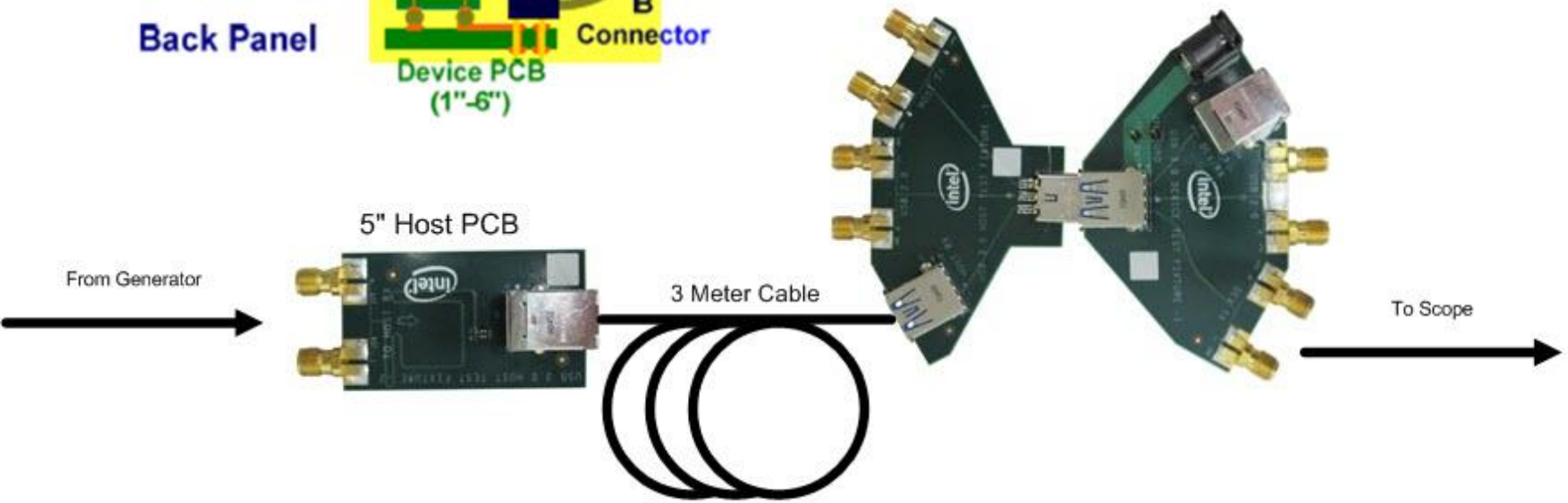
Short Channel = no cable and shortest possible PCB traces



SuperSpeed Host Receiver Test Calibration and compliance channel

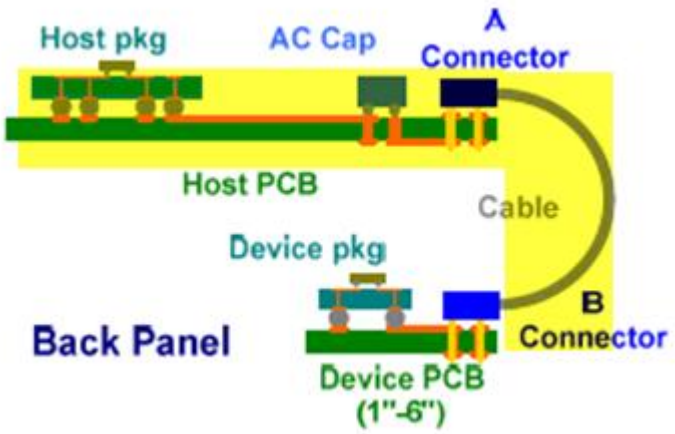


- Host 5” of trace
- 3 meter USB 3.0 cable

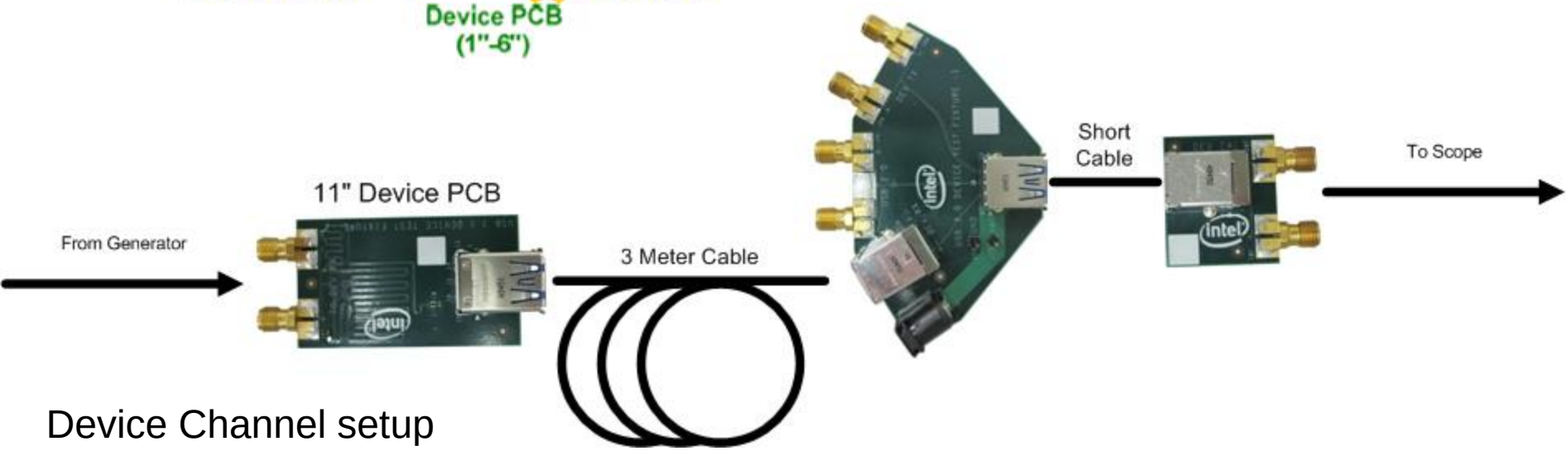


Host Channel setup

SuperSpeed Device Receiver Test Calibration and compliance channel



- Device 11” of trace
- 3 meter USB 3.0 cable



Device Channel setup

Fixtures and cables available from the USBIF at:

http://www.usb.org/developers/estoreinfo/

USB-IF eStore Details

Prior to purchasing products from the USB-IF, please review our return policy and legal disclaimer.

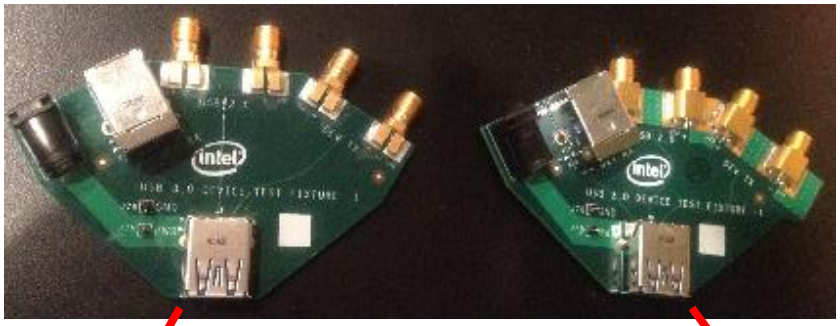
USB 3.0 Electrical Test Fixture Kit

The USB 3.0 Electrical Test Fixture Kit provides a worst case, ISI hardware channel for PHY's. It is intended to assist companies in testing transmitter signal quality and receiver sensitivity for either hosts or peripherals.

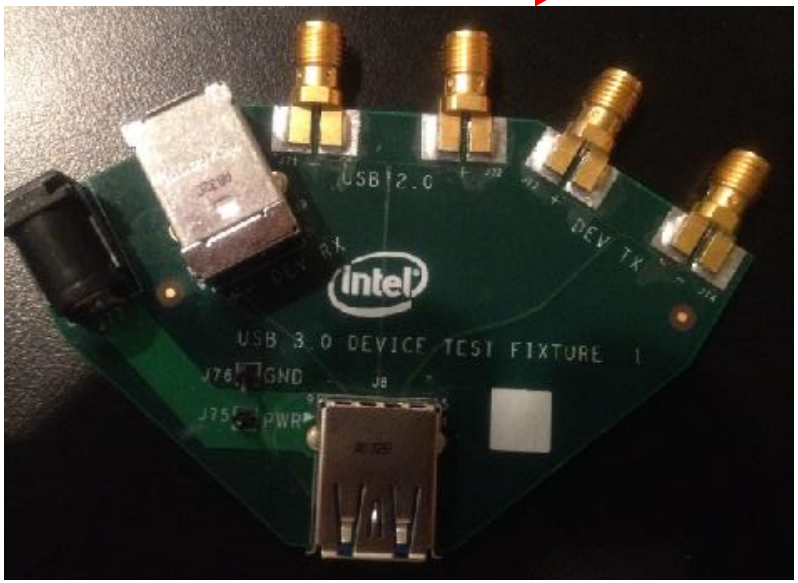
The kit contains five test fixtures and one 5-Volt DC power supply to provide V-Bus to peripherals. The fixtures consist of:

qty 2 – Host Test Fixtures
qty 2 – Device Test Fixtures
qty 1 – Device Calibration Fixture
qty 1 – Cable Assembly to be used in conjunction with the fixtures. Includes a USB 3.0 Standard A to Standard B (3 meter), Standard A to Standard B (4 inch) and Standard A to Micro B (4 inch).

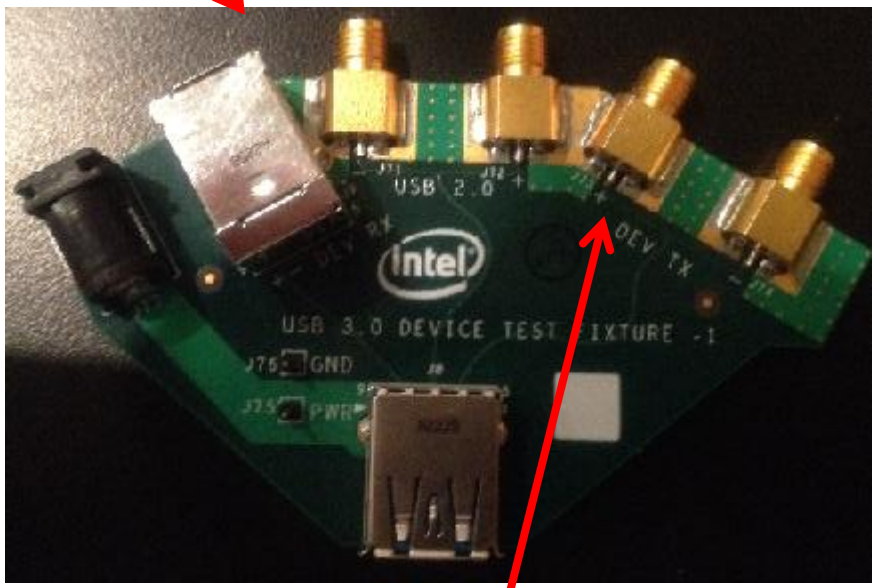
New build of USB-IF Fixture kit now available



Old Fixture



New Fixture



New fixtures include improved SMA connectors

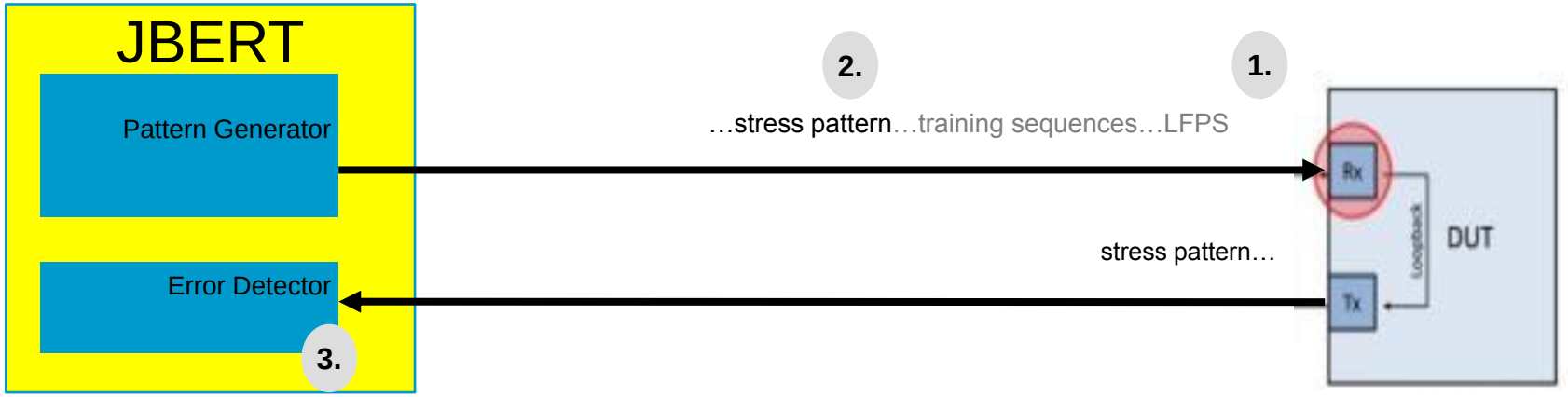
Receiver Test Procedure

External Error Counter

Turn on loopback by sending LFPS and required training sequences

The receiver stress pattern is BDAT with SKPs inserted as described in the standard.
The pattern checker receives the looped stress pattern BDAT and recognizes bit errors

After sufficient test time the error counter of the JBERT is read

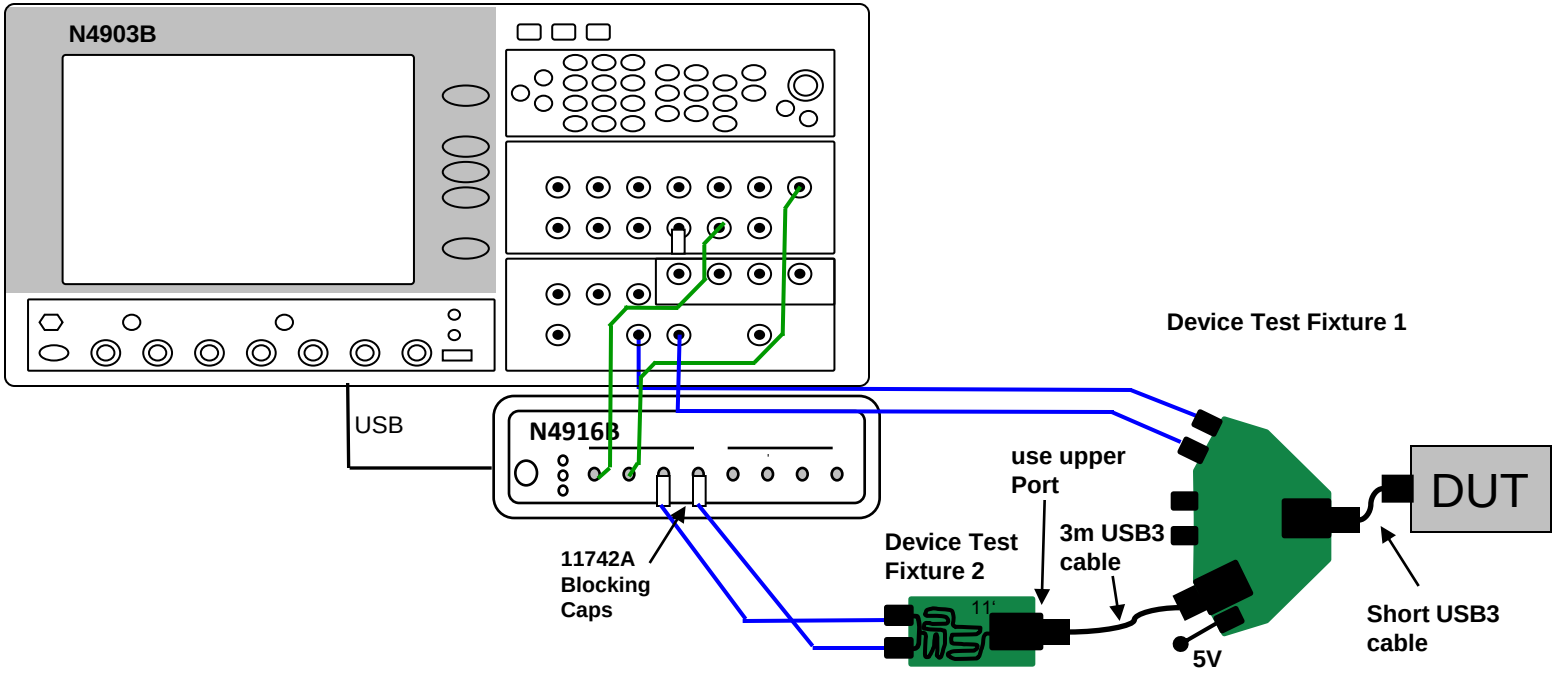


Pattern Checker: JBERTB SER

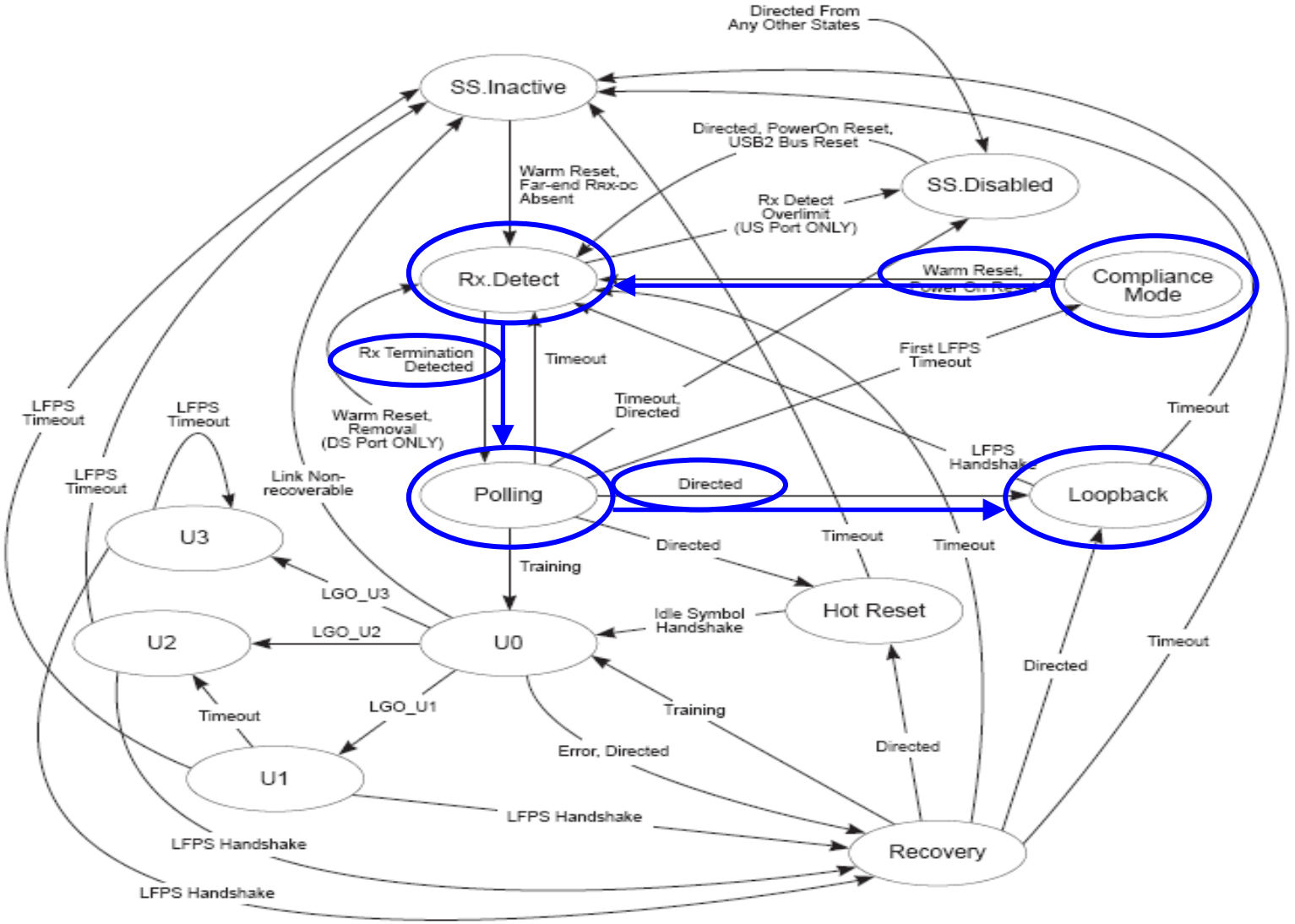
USB 3.0 SuperSpeed Receiver Test Setup

for Devices with J-BERT B SER Counter

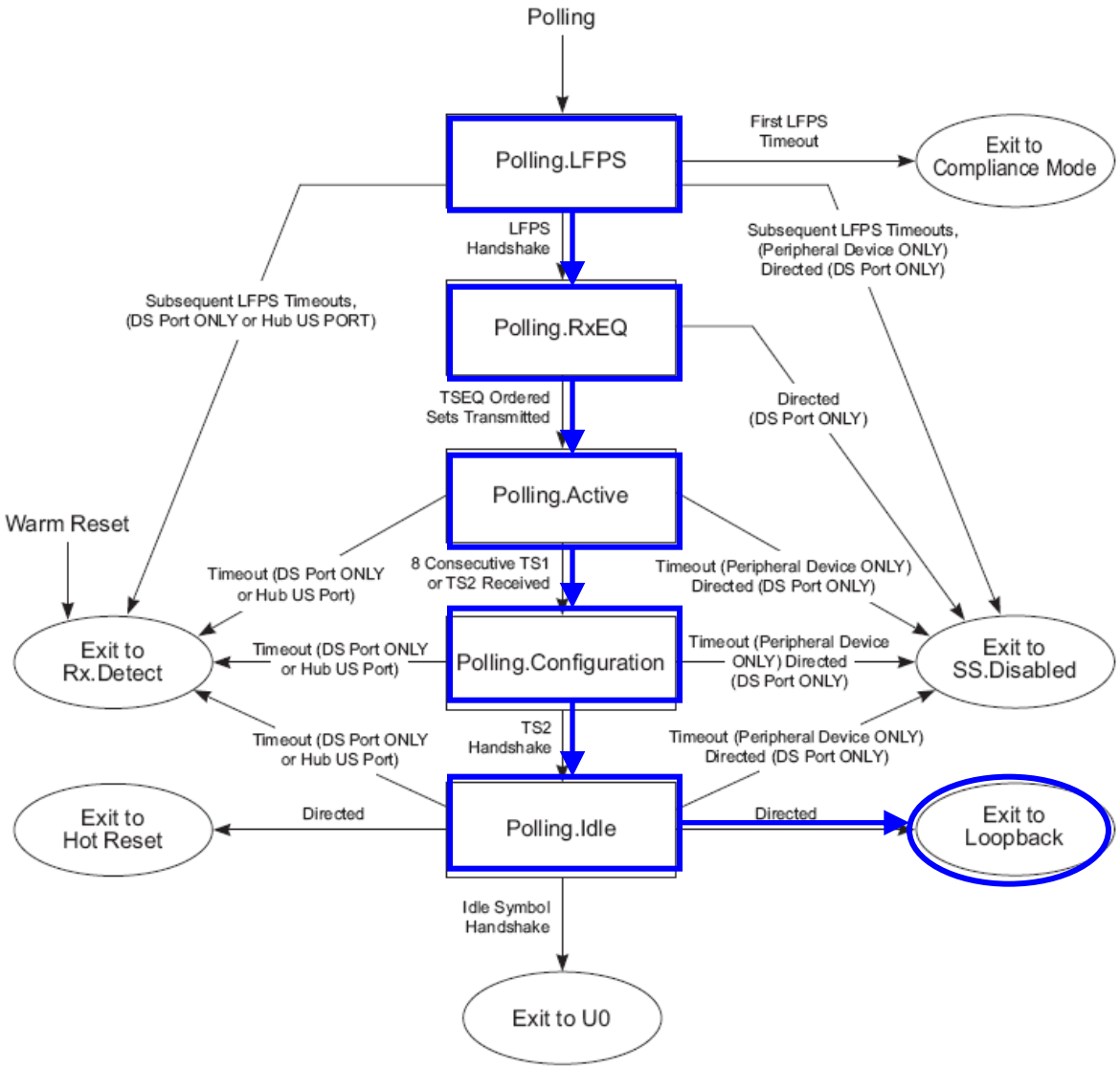
Connect the equipment as shown below
- Use DC blocking capacitors in the connection from the J-BERT/De-Box output to the test fixture input
- For host testing: Additional cabling and a BIAS tee are required
- All necessary connections are displayed in the N5990A software, too



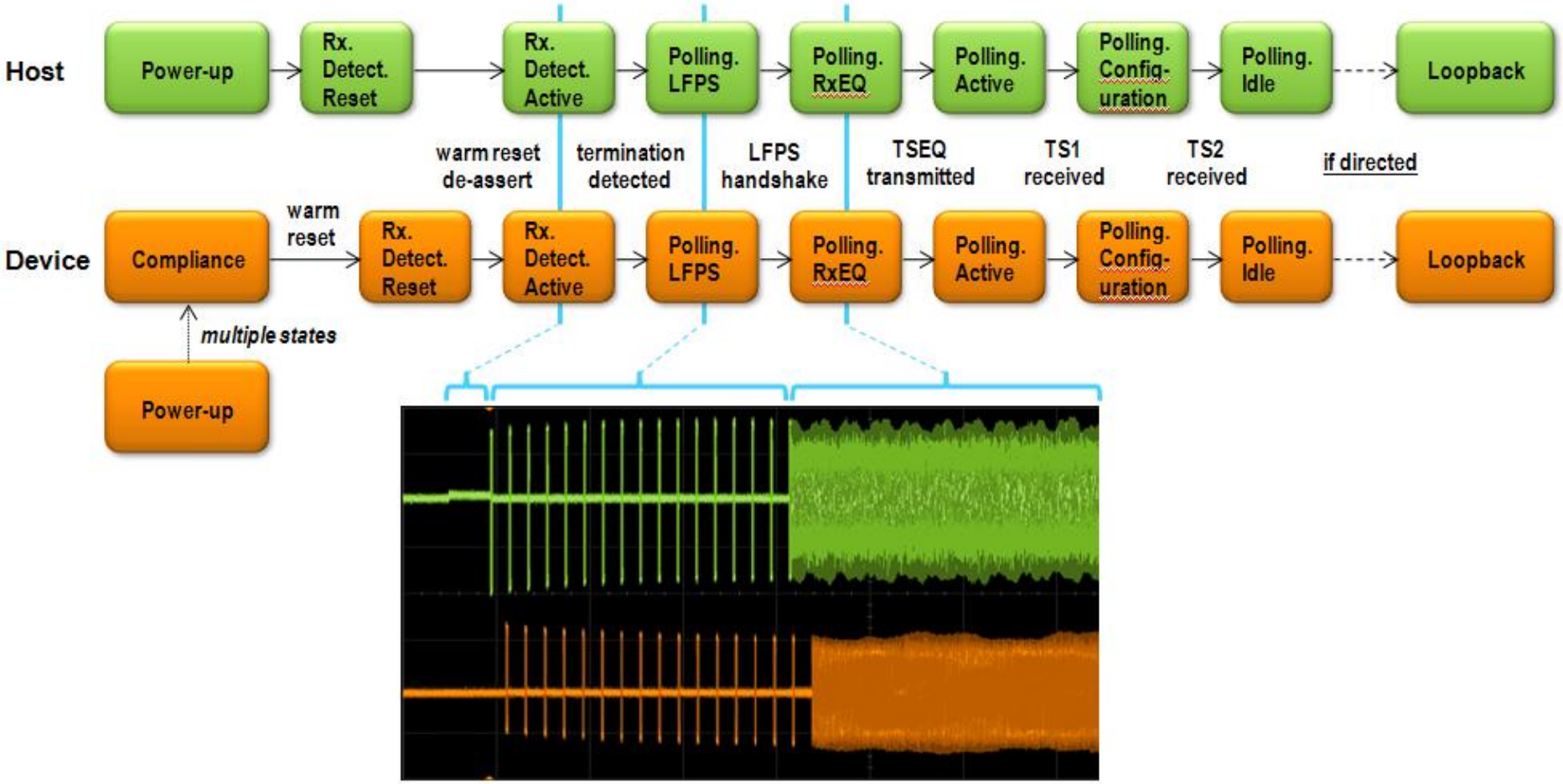
USB 3 Loopback Training



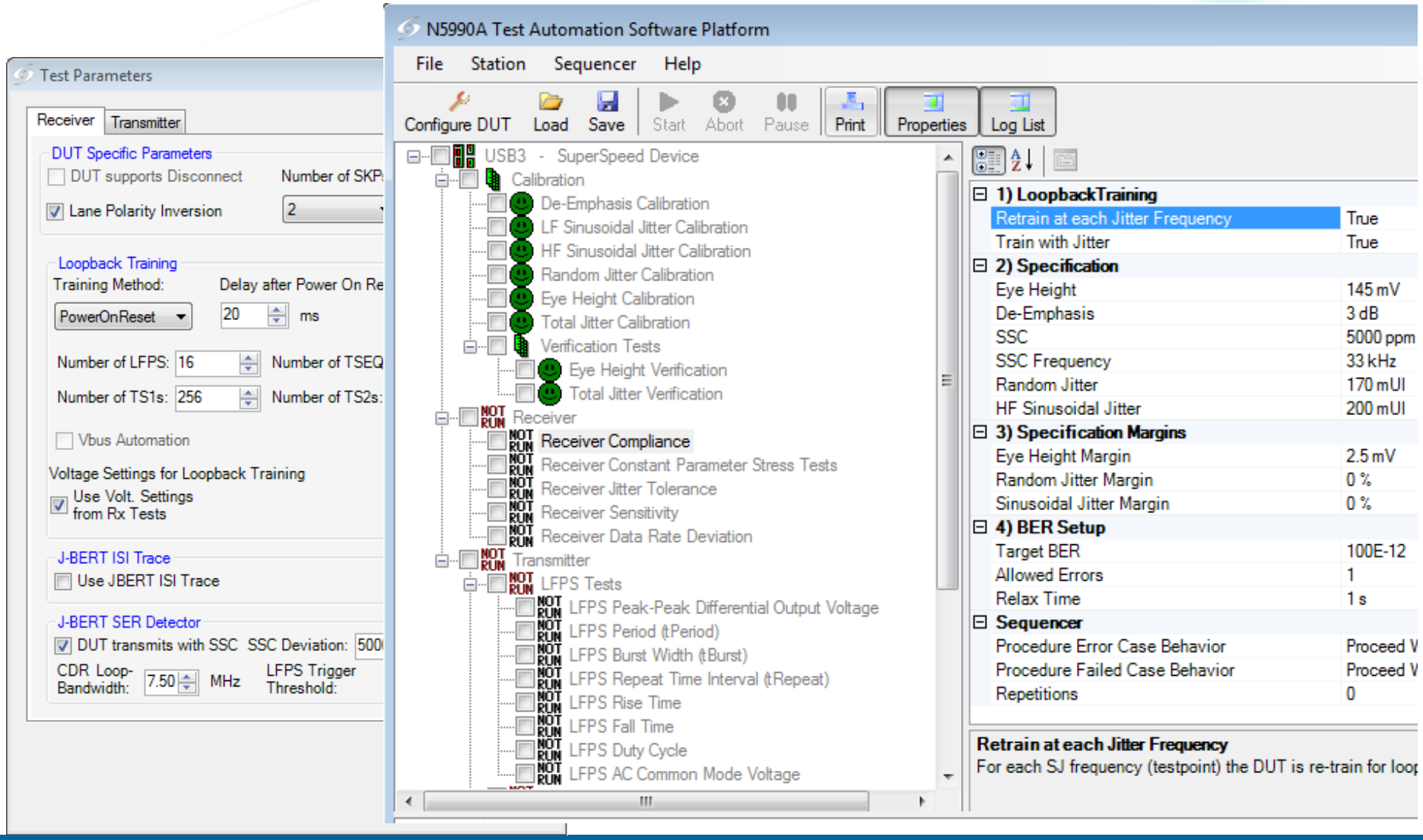
USB 3 Loopback Training



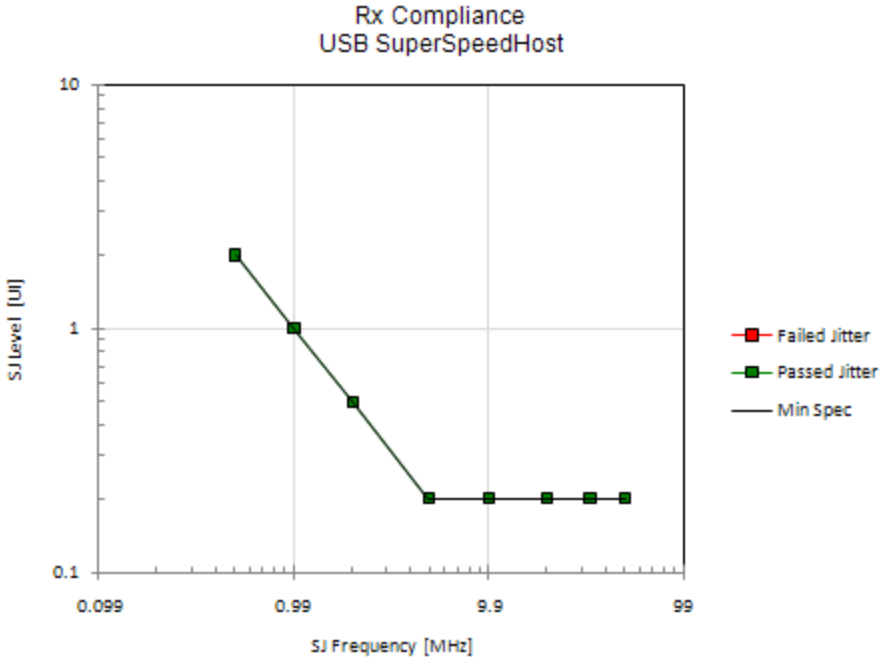
Typical SuperSpeed Link Turn-on Sequence

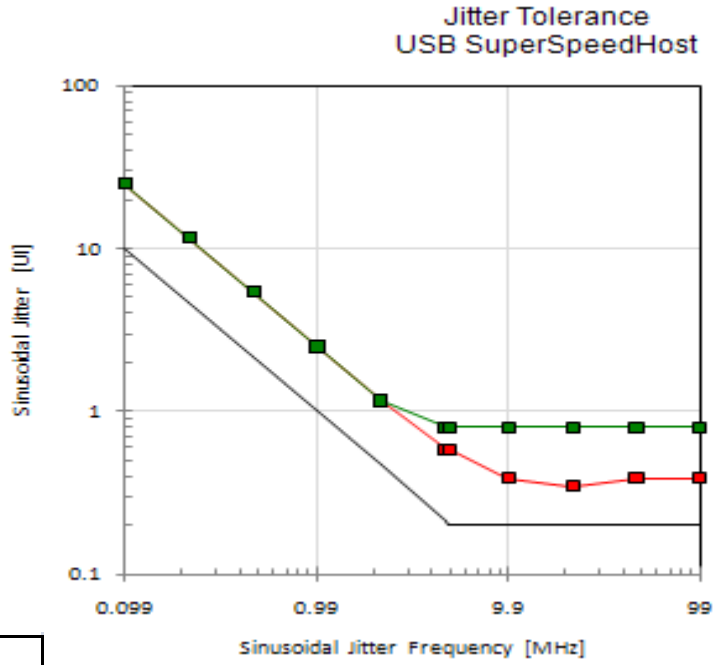


USB 3 Reciever Test Automation using N5990A automation sw



SuperSpeed Receiver Tests
Rx Compliance and Jitter Tolerance Testing





Result	SJ Frequency [MHz]	Failed Jitter [UI]	Passed Jitter [UI]	Min Spec [UI]	Symbol Errors
pass	0.500		2.00	2.000	0
pass	1.000		1.00	1.000	0
pass	2.000		0.50	0.500	0
pass	4.300		0.20	0.200	0
pass	10.000		0.20	0.200	0
pass	20.000		0.20	0.200	0
pass	33.000		0.20	0.200	0
pass	50.000		0.20	0.200	0

Engineering Change Notices (ECNs)

1. The USB 3.0 Specification (including errata and ECNs through May 1, 2011)
2. USB 3.0 Adopters Agreement
3. On-The-Go and Embedded Host Supplement to the USB Revision 3.0 Specification Revision 1.1 as of May 10, 2012
4. USB Power Delivery Specification Revision 1.1, Including Errata through October 31, 2012
5. Inter-Chip Supplement to the USB Revision 3.0 Specification, Revision 1.01 as of February 11, 2013

The following ECNs and Errata that are part of the USB 3.0 Specification are also included in a subfolder of the zip file:

6. New Addition of Link Command LDN Engineering Change Notice as of April 4, 2009
7. USB 3.0 Standard-B and Standard-B Crosstalk Engineering Change Notice as of April 4, 2009
8. Reset Propagation Engineering Change Notice as of May 8, 2009
9. Reset Propagation Figure
10. Q1 09 USB 3.0 Errata as of May 15, 2009
11. Clarification on the Chamfer on USB 3.0 Micro Connectors ECN as of March 23, 2010
12. Maximum Unmating Force Value Definition to USB 3.0 Micro Connectors ECN as of March 23, 2010
13. State Machines Engineering Change Notice as of June 9, 2010
14. Efficient ISO and PINGs Engineering Change Notice as of June 9, 2010
15. Contact Plating Thickness Engineering Change Notice as of June 9, 2010
16. Standard-B Connector Near End Crosstalk Engineering Change Notice as of June 9, 2010
17. USB 3.0 Errata as of June 9, 2010
18. USB 3.0 Errata as of June, 2011
19. DSPORT State Machine as of September 29, 2011
20. USB 3.0 Peripheral USPort State Machines ECR as of September 29, 2011
21. USB 3.0 Reference Equalizer as of September 29, 2011
22. LTSSM Timeout Naming Errata as of September 29, 2011
23. USB 3.0 Standard A Receptacle as of January 19, 2012
24. USB 3.0 Standard A Contact Height as of February 24, 2012
25. USB 3.0 Spread Spectrum Clock Range
26. USB 3.0 Connector Crosstalk Spec
27. USB 3.0 Micro AB Connector as of December 20, 2012
28. USB 3.0 Radio Friendly Clock Unit Interval as of February 18, 2013
29. USB 3.0 Micro-B Cable Loss Specification as of March 18, 2013
30. USB 3.0 Relaxation of tRx Detect Quiet Timeout as of April 3, 2013

USB2 Compliance Testing Updates

Testing requirements have changed over the years

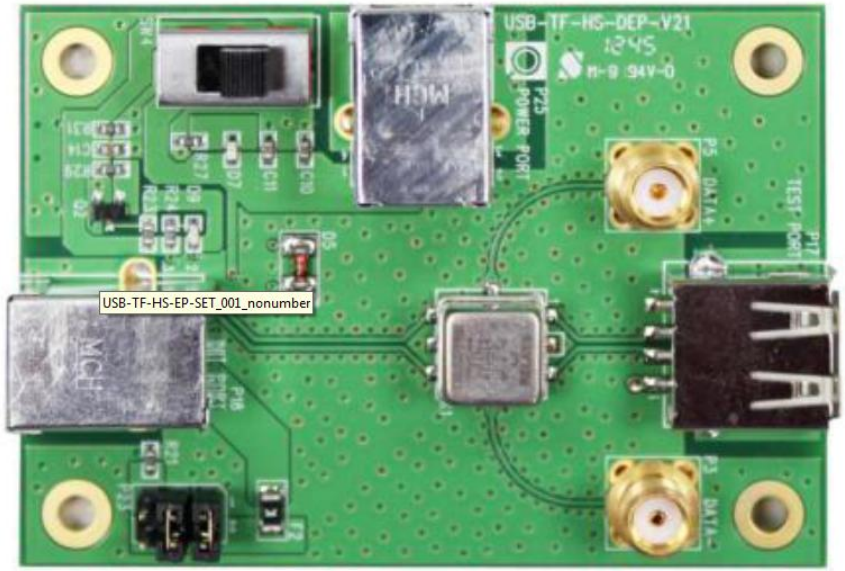
Details can be found at

http://compliance.usb.org/index.html

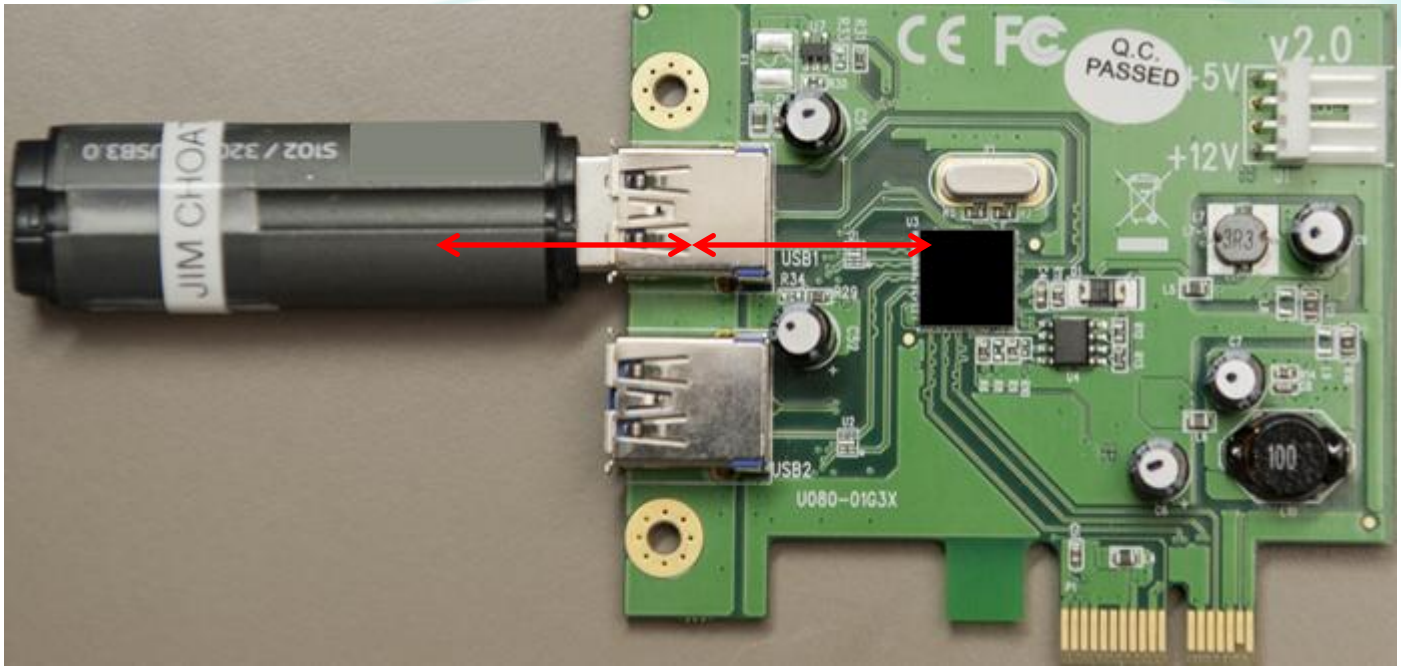
Rise/Fall time measurement

High Speed SQ testing fixture change

High Speed test J and K testing



What is the Short Channel Definition & Why?



- USB 3.0 Flash drives are the best example where short channels are the norm
- For discrete hosts the xHCI controllers are frequently place very near the USB 3.0 connectors with very short PCB traces
- In this use case the loss of the channel is very small and it is critical that RX equalizers have sufficient dynamic range to operate in a low loss channel environment

USB3.0 Reference Equalizer ECN

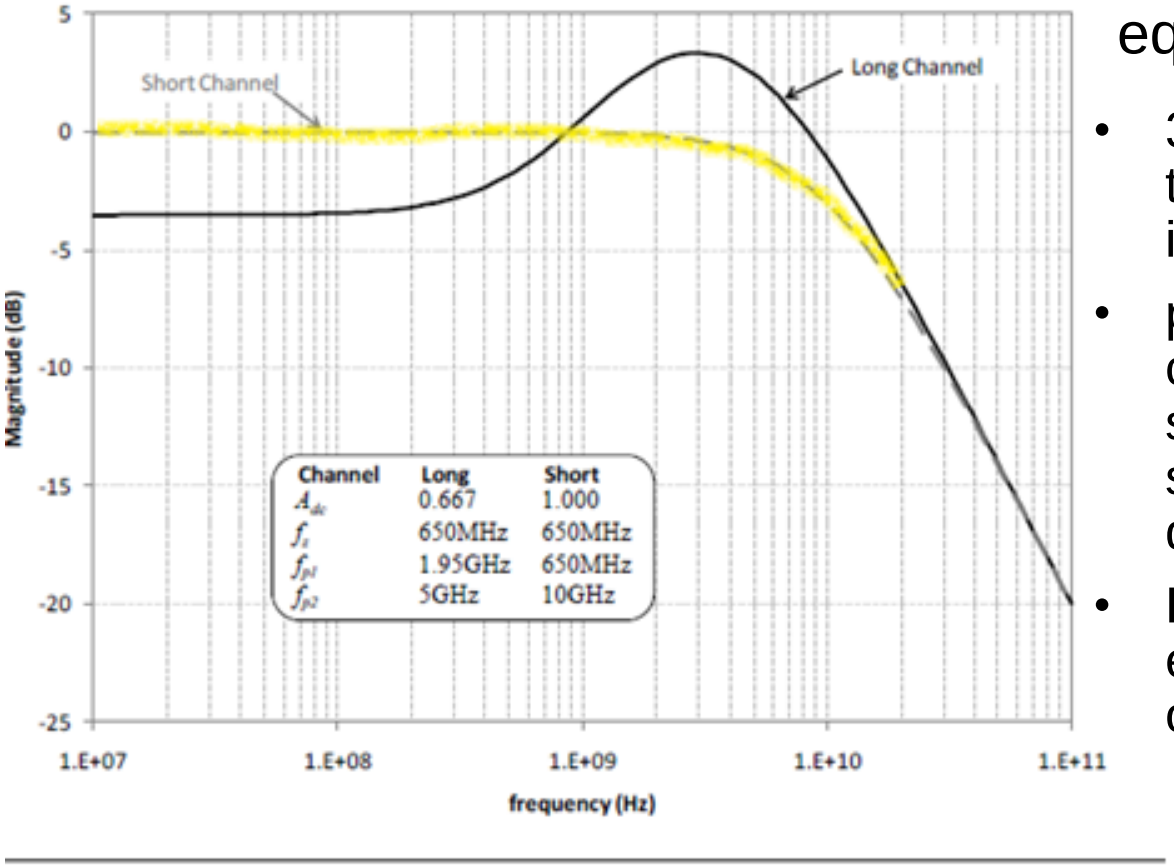


Figure 6-17. Tx Compliance Rx EQ Transfer Functions

- Current testing reference equalizer is for a long channel
  - 3m cable plus long host PCB trace (~18-20dB differential insertion loss).
  - proper equalizer behavior is critical for interoperability in a short channel (no cable and short host PCB, ~3-5dB differential insertion loss)
  - ECN defines a second reference equalizer transfer function that is optimized for the short channel

Physical Layer Compliance Pitfalls

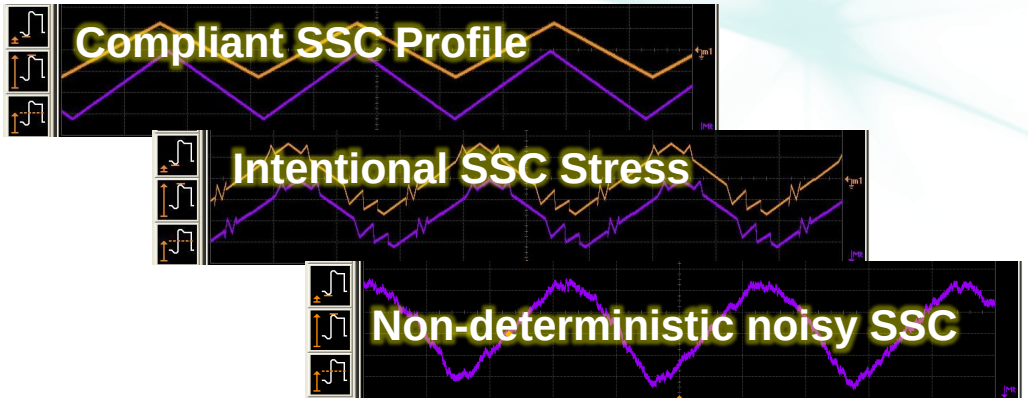
- Transmitter SSC quality
  - SSC ECNs
  - Interference issues

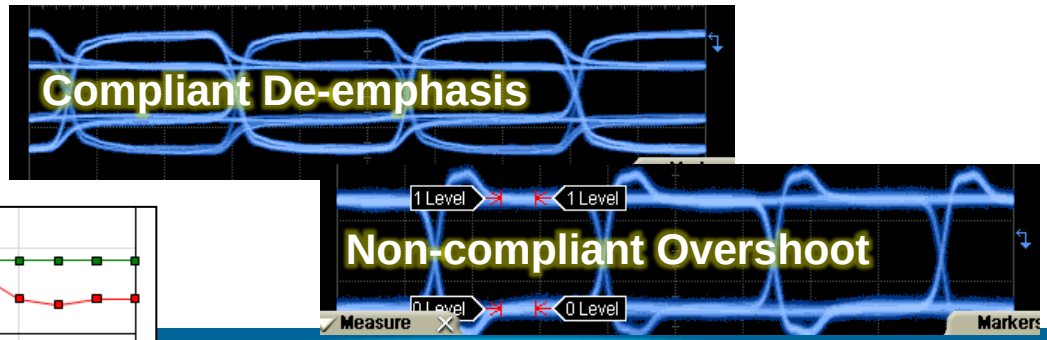
- Loopback issues
  - Dut needs custom sequence
  - DUT drops out easily

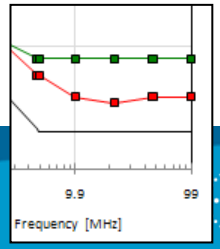
- Calibration issues
  - Inconsistent
  - Poor Sj/Rj mod
  - Automation of Cal

- Failing de-emphasis
  - Great impact on TJ and Eye

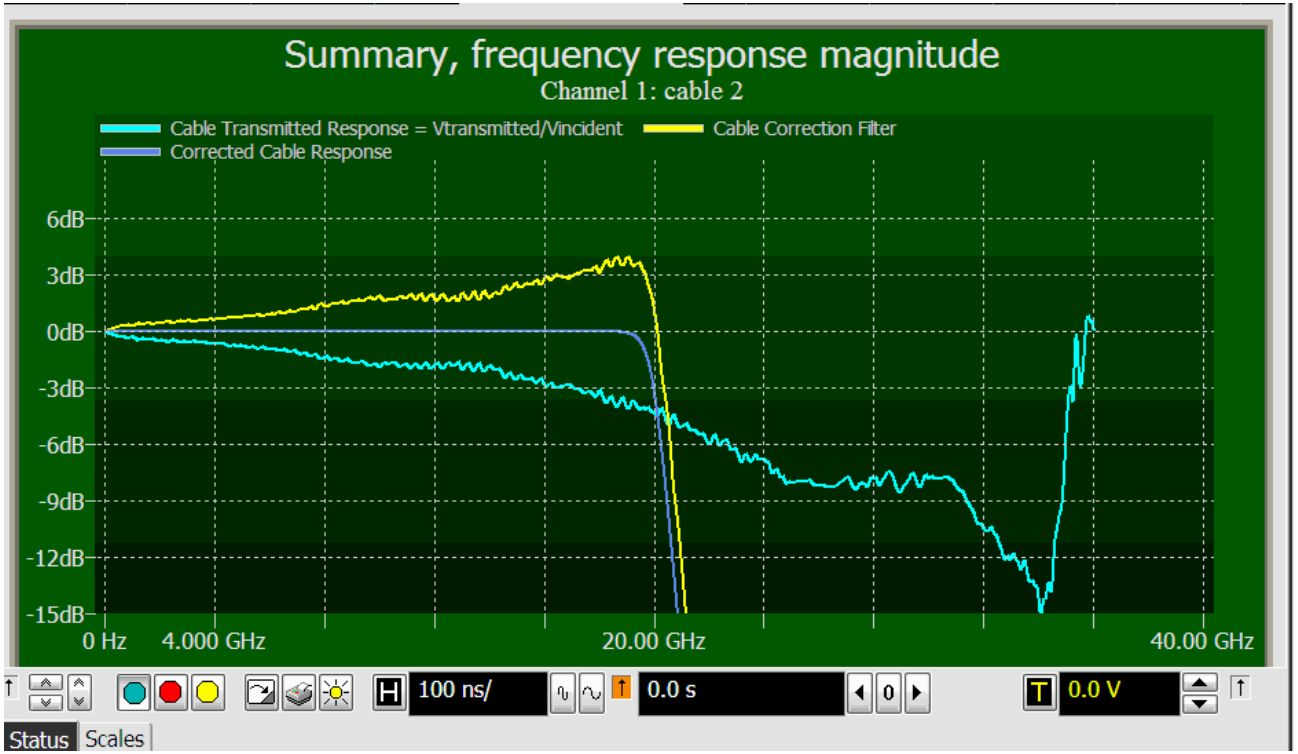
- Jitter tolerance failures
  - 10Mhz, 20Mhz, 33Mhz







PrecisionProbe and Cable (N2809A)

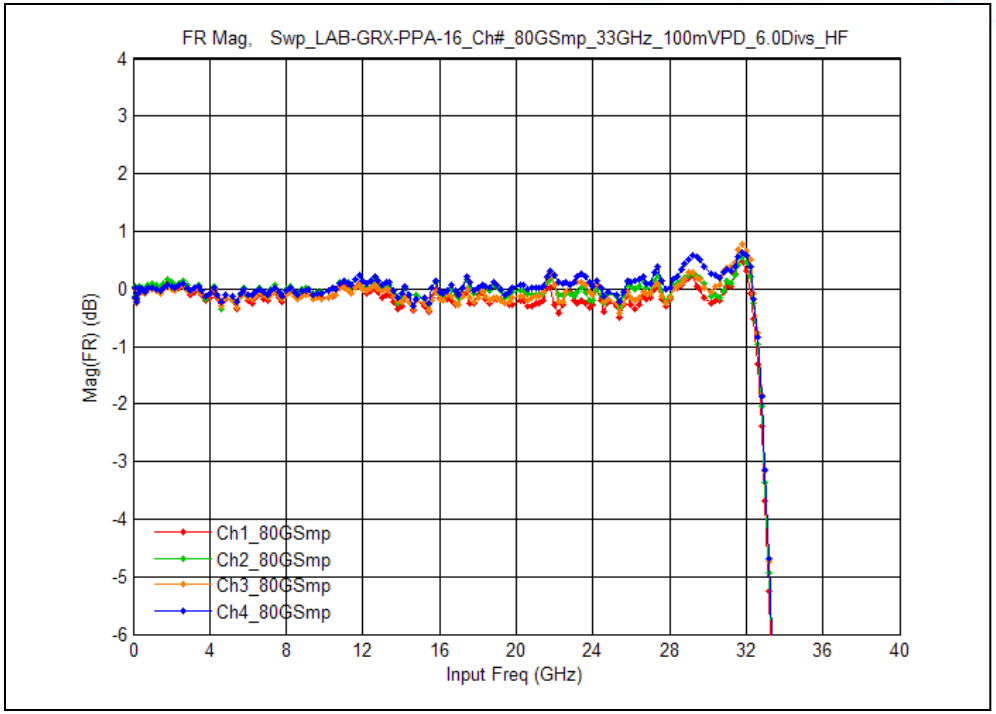


Characterize and correct any input path to your oscilloscope input using only your oscilloscope

The Importance of a Flat Frequency Response

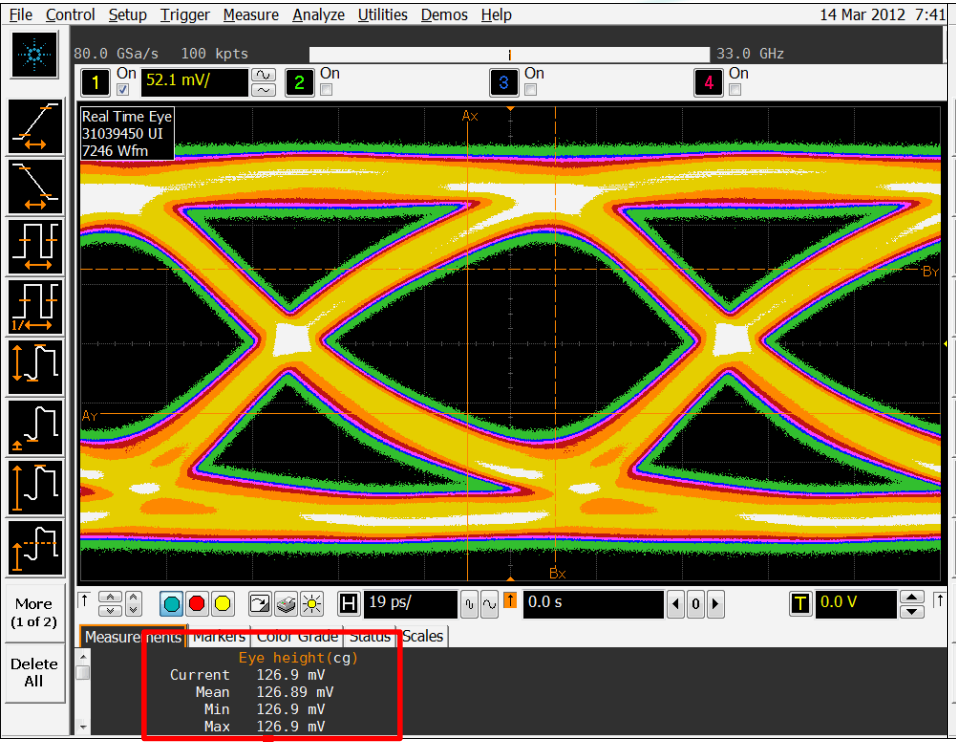
Why do we care about a flat frequency response?

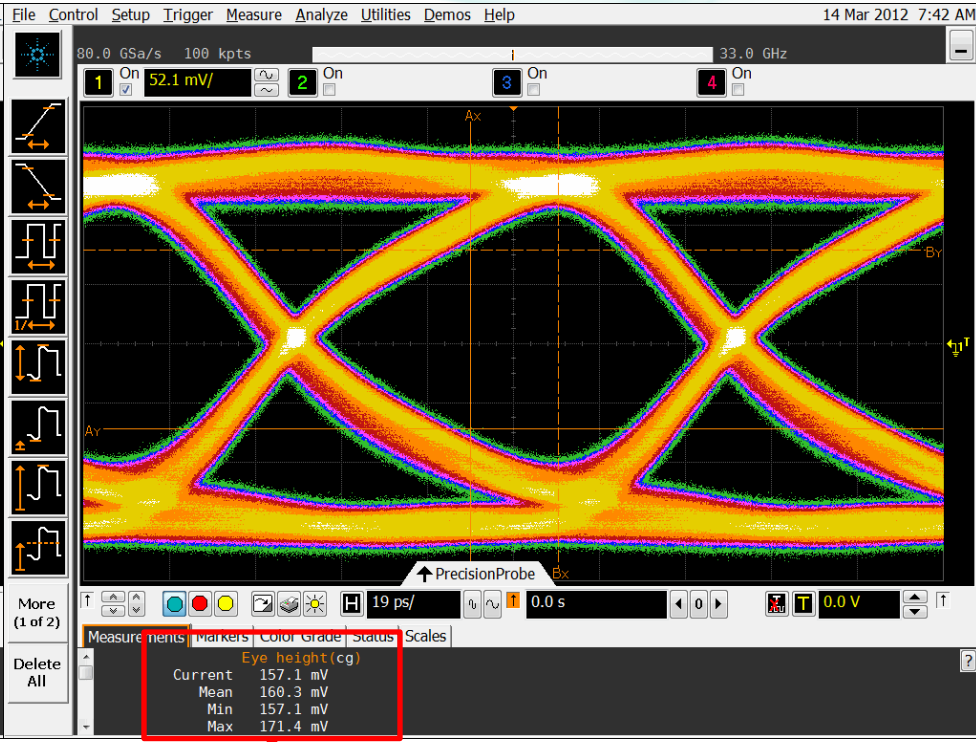
- The flatter the response the more accurately the scope will depict the signal
- Measurements become more repeatable
- ISI modeled closer to the reality



Frequency response of the 90000 X-Series

Eye margin improvement using precision cable



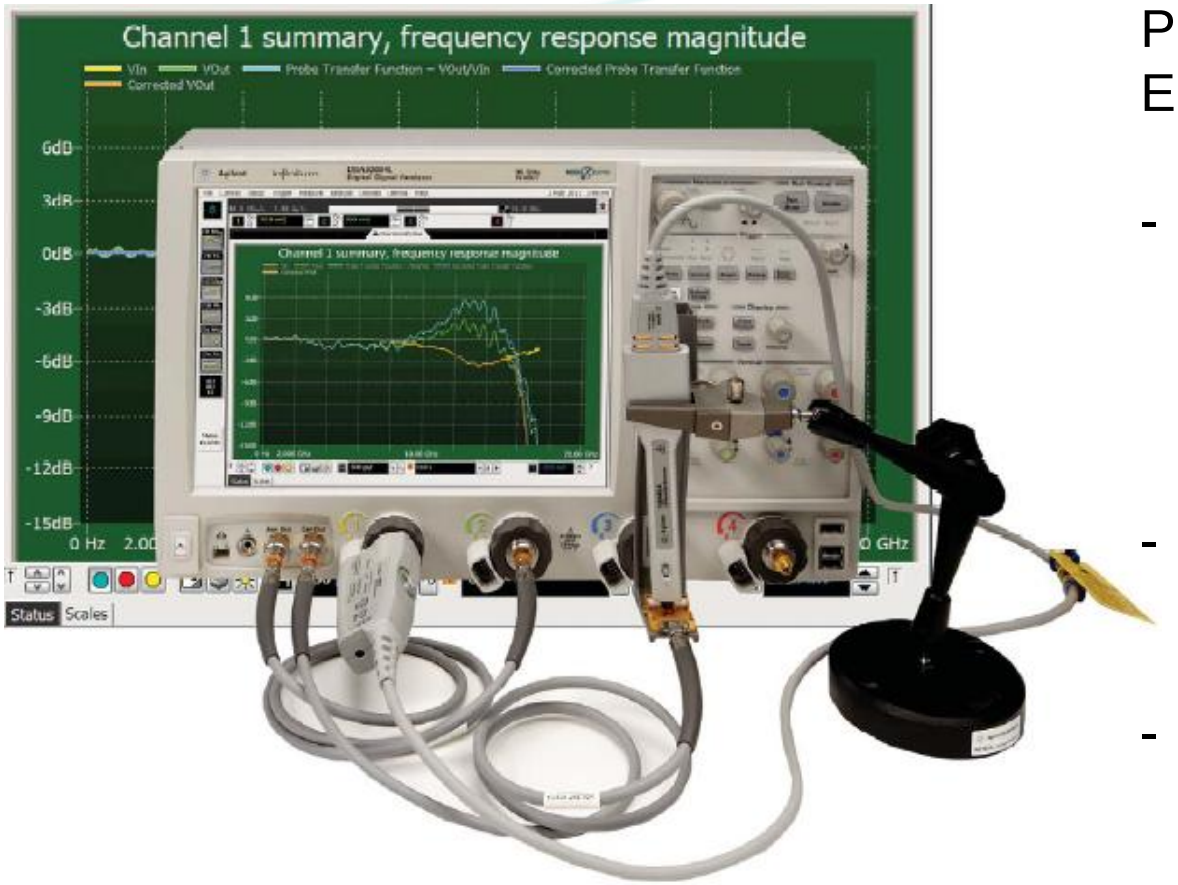


Eye height(cg)	
Current	126.9 mV
Mean	126.89 mV
Min	126.9 mV
Max	126.9 mV

23.8% Increase in eye height

Eye height(cg)	
Current	157.1 mV
Mean	160.3 mV
Min	157.1 mV
Max	171.4 mV

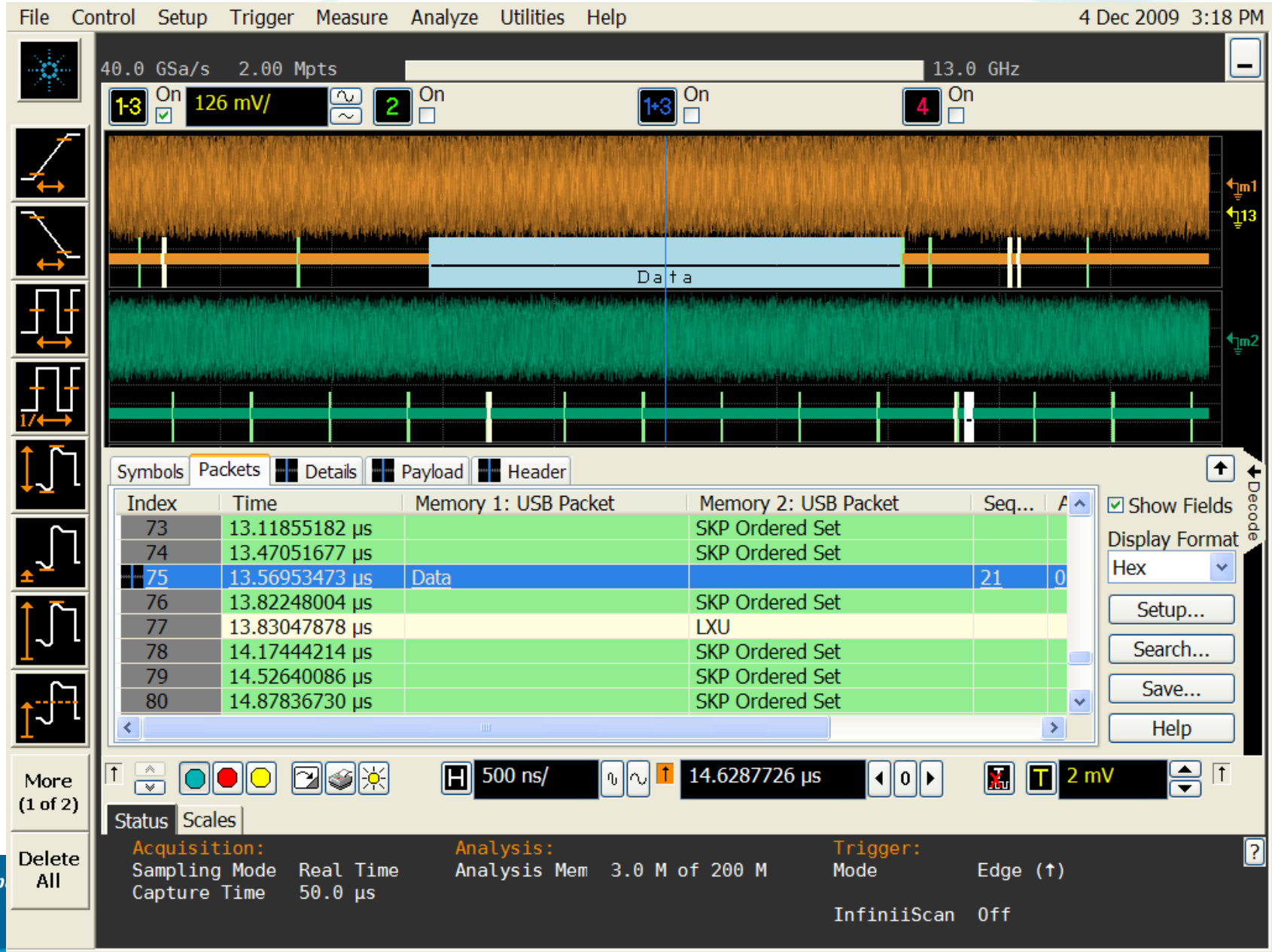
The Solution: PrecisionProbe



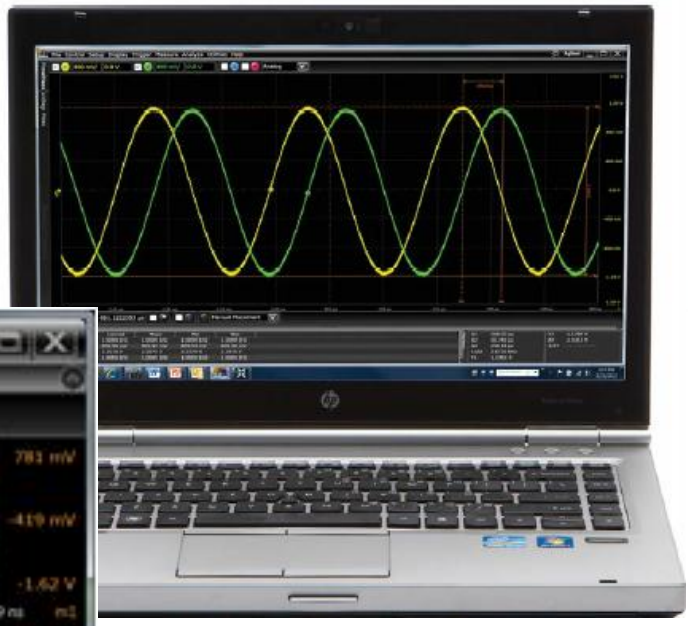
PrecisionProbe Quickly and Easily:

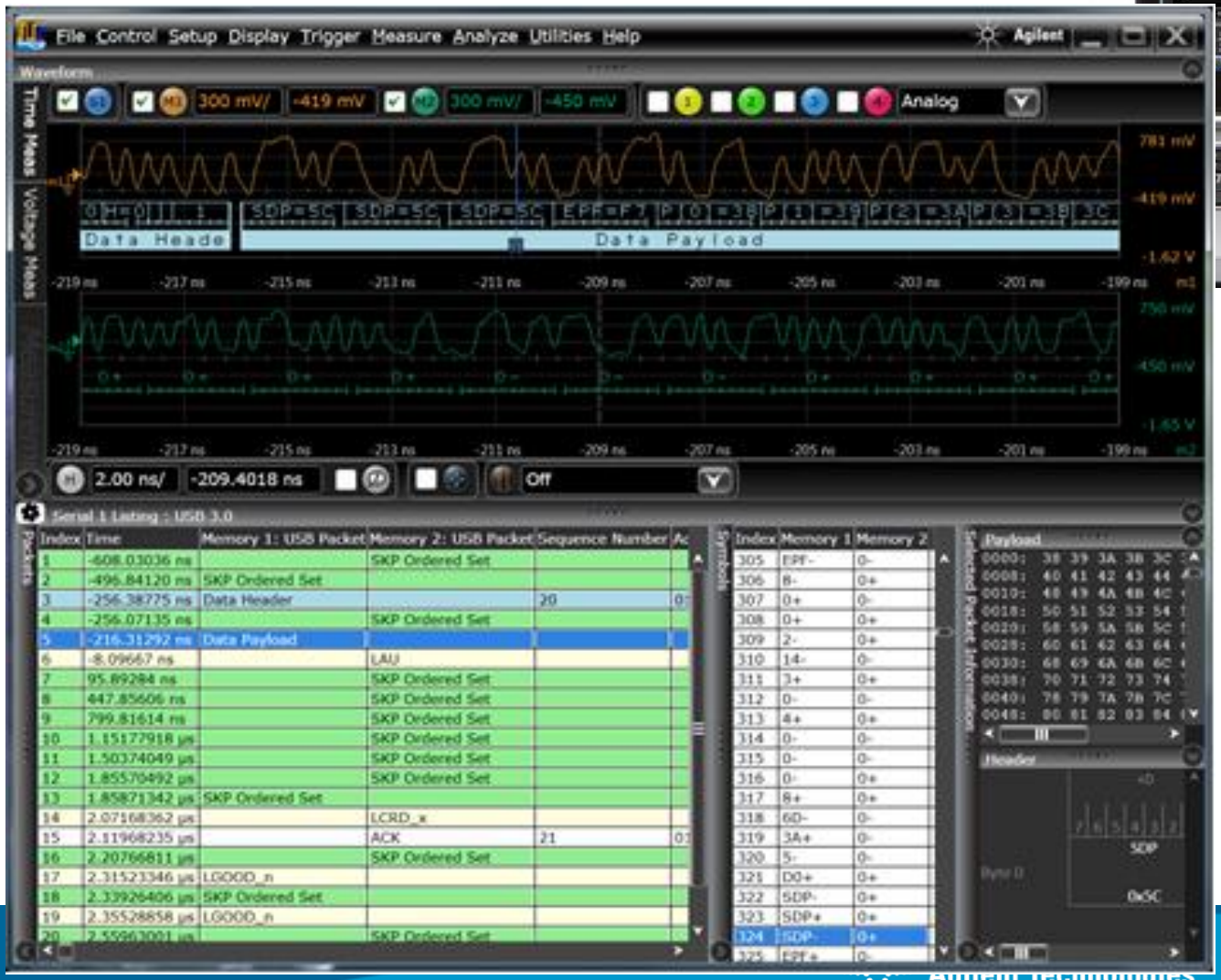
- Characterizes and corrects the frequency response (Vout/Vin) of phase of any probe and probe head combination
- Characterizes and corrects for insertion loss caused by cables and fixtures
- Characterizes and corrects for insertion loss caused by switches for probes and cables.
- For a typical 10-12Ghz cable USB3 eye margin can improve 10-20mV

USB 3.0 Protocol Decode: on the scope



NEW: Agilent N8900A InfiniiView Oscilloscope Analysis Software





- View, analyze, share and document from your PC
- Free up your scope to actually make measurements
- Operates just like the scope
- Undock to better view result windows with multiple monitors

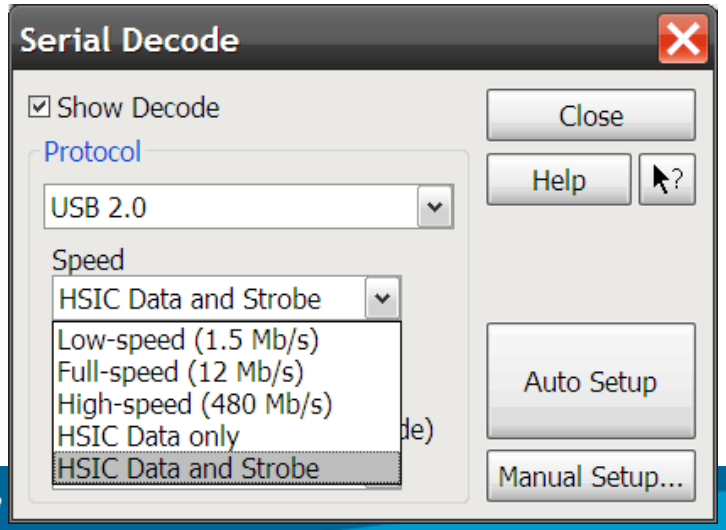
Agilent High Speed Inter-Chip test solutions

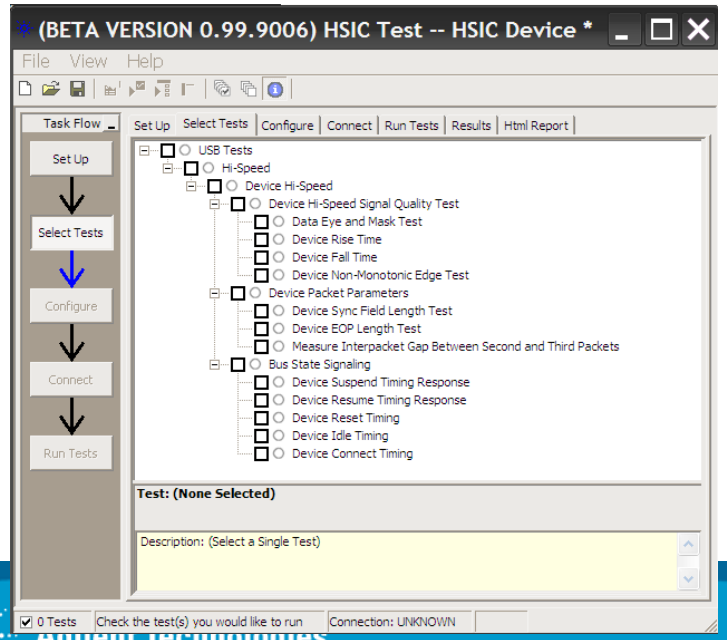
•HSIC is a supplement to the USB 2.0 specification developed primarily by chip vendors to provide simpler and lower power interface between a USB host and device

- Specification is included with USB 2.0 specification located here: http://www.usb.org/developers/docs/

•Agilent U7248A HSIC compliance test software

•Used in conjunction with Agilent's U5464A/B USB protocol triggering and decode software, developers have a complete set of tools to validate/debug HSIC solutions.





Coming Soon: 10Gbps SuperSpeed

USB 3.0 Promoter Group is comprised of Hewlett-Packard, Intel, Microsoft, Renesas Electronics, ST-Ericsson and Texas Instruments. Additionally many other companies are participating in the development effort.

Key characteristics of the 10G SuperSpeed USB solution:

- 10G bps SuperSpeed USB is a supplement to the existing USB 3.0 specification
- The specification is expected to be completed by the middle of 2013
- Compatibility with existing cables and connectors
- Improved data encoding for more efficient data transfer leading to higher throughput and improved I/O power efficiency
- Compatible with existing USB 3.0 software stacks and device class protocols
- Compatible with both existing 5 Gbps and new 10 Gbps USB 3.0 hubs and devices, as well as USB 2.0 products

10Gbps SuperSpeed considerations

- Will require higher BW channels
- Re-driver design requirements and considerations will be more critical
- Speed negotiation handshake for 10G and above
- Channel limitations will need to be understood
- Go to http://www.usb.org/developers/USB-Futures.pdf

For updates and information.

USB 3.0/2.0 Protocol Analyzer & Jammer

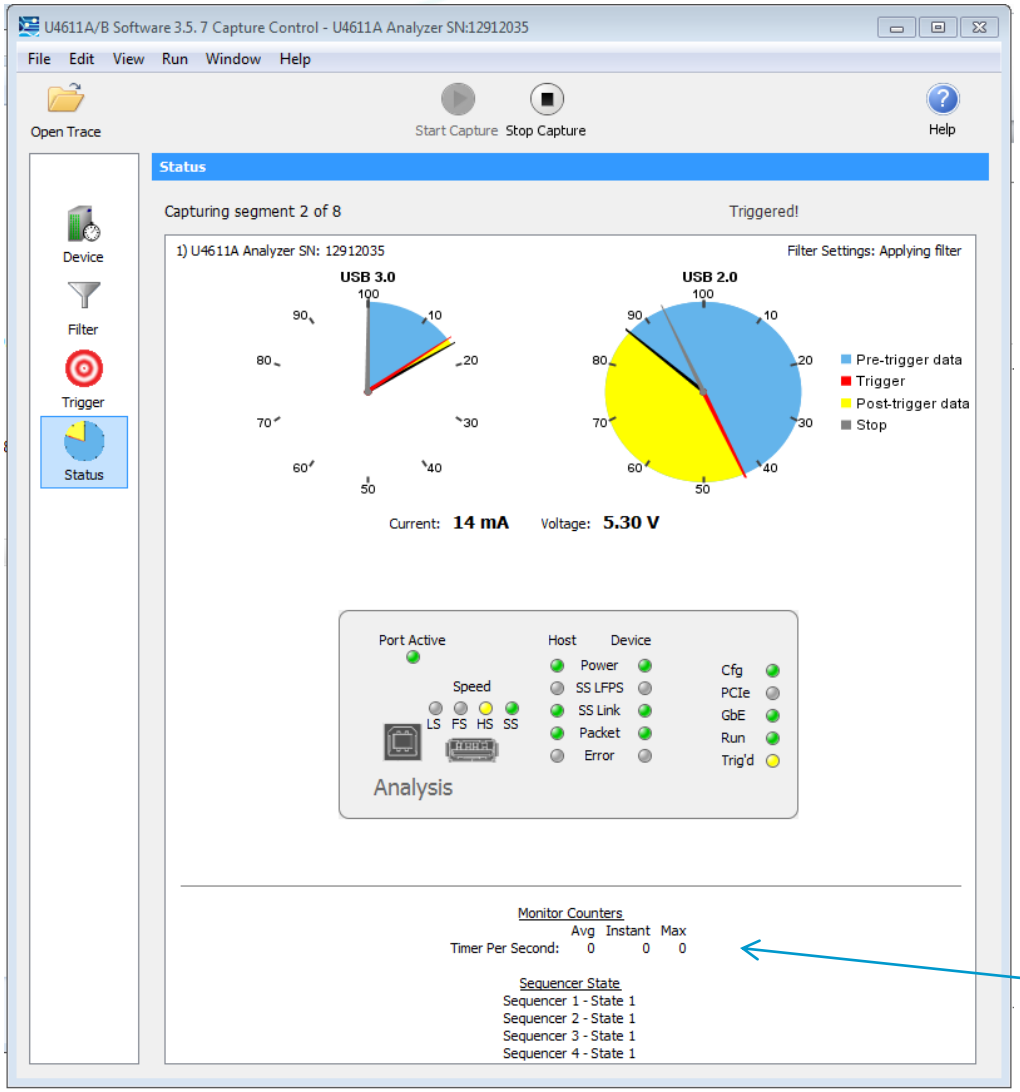
KEY SPECS
Simul. USB 3.0 & 2.0 capture
Up to 18GB trace buffer
4 sequencers, 26 states each
- (32) 32-bit timers & counters
Host I/F: GbE, PCIe X4
Cascadable with SAS/SATA
Full API support

- ***Find & Fix the most complex problems***
  - **Most advanced triggering on the market**
  - **Deepest trace buffers on the market *by far***
    - *Segmented buffers allow memory use options*
  - **The <u>only</u> USB3.0 Jammer on the market!**
- ***See your DUT, not our instrument***
  - **Auto-detect instruments on LAN**
  - **Lightning-quick first-screen display**
  - **Fastest processing of "whole trace," too**
    - E.g. histogram view of multi-GB trace in seconds
  - **Clean, intuitive GUI, with multiple viewing options to ease migration**
    - Drill down into packet details, with "data sheet" graphical views of bit fields, etc.

U4612A USB 3.0 Jammer

- Can be used to create a variety of errors in a real OS environment that cannot necessarily be created by a generator
- Standalone unit (does not require U4611A/B analyzer)
- Example error types, events, packet modification, etc.
  - LGOOD_*n* / LCRD_*a* out of order
  - Corrupted ordered sets, LMPs, etc.
  - CRC-5/16/32 errors
  - LBA out of range
  - Link connect / disconnect
  - Power up / down (bus powered devices only)
  - Missing or corrupt frames
  - BOT or UAS Sense IU / Response IU errors

Deep Buffer required to capture Mixed traffic



Red tic shows trigger event

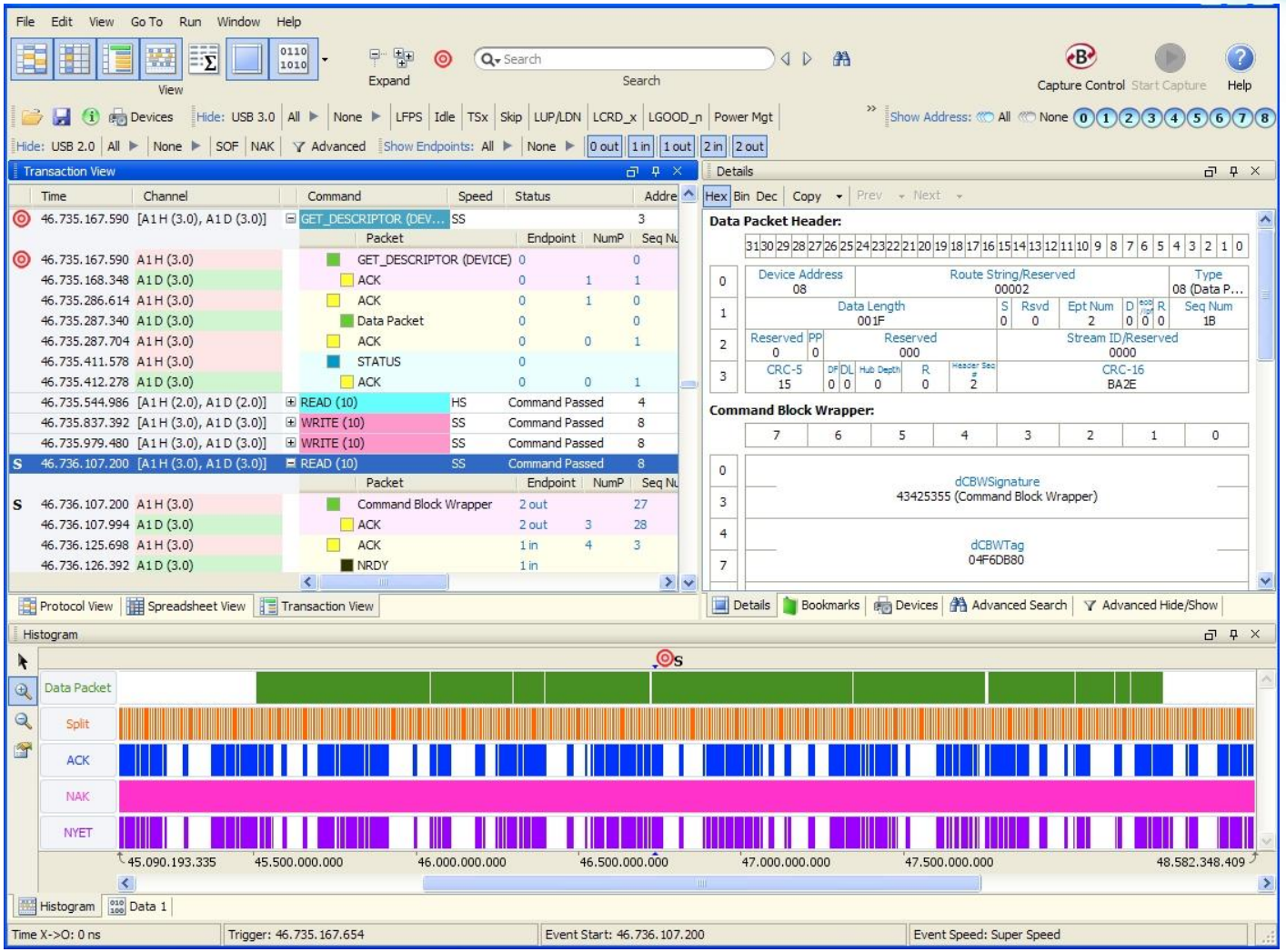
Customizable counters and sequences

Definable event

- Count
- Count per second

Flexible Trace Views, from High-Level to Detailed Synchronized - Multi window

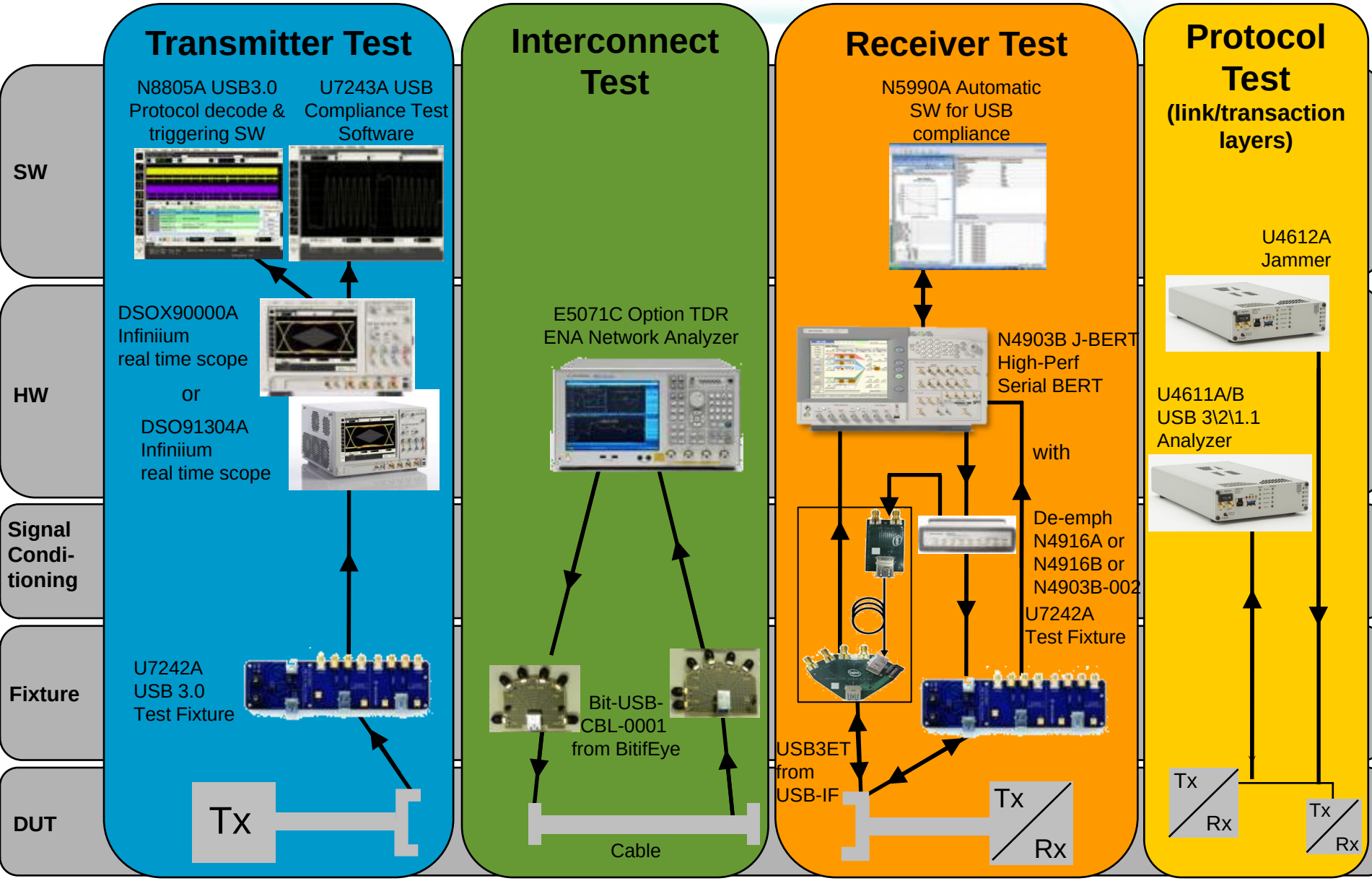
Transaction view



Packet Detail view

Histogram view

USB 3.0 – Total Solution



Summary

- USB-IF compliance tests and requirements have changed over time.
- Be sure to check for updates and ECNs at http://www.usb.org/developers/docs/
- USB 3.0 Receiver testing is the most challenging part of PHY layer testing
  - Accurate and automated calibration is the key to repeatable and accurate results
- Agilent USB solutions adopted by test labs world wide
  - Confidence in our solution comes from our leadership and participation in standards bodies as well as our deep technical expertise
- 10G SuperSpeed USB 3.0 will bring exciting new performance capabilities to product developers next year and beyond

Agilent has the tools and expertise to help you conquer USB 3.0 Physical Layer Test Challenges

Additional Links and References

Agilent Oscilloscope information (TX testing solutions)

www.agilent.com/find/scopes

Agilent Oscilloscope application software

http://www.home.agilent.com/agilent/product.jspx?nid=-35491.0.00&cc=US&lc=eng

Agilent N4903B Jbert (Rx testing solutions)

www.agilent.com/find/JBERT

Agilent N8900A InfiniiView Oscilloscope Analysis Software

www.agilent.com/find/InfiniiView

Agilent N2809A PrecisionProbe oscilloscope probing software

www.agilent.com/find/precisionprobe

THANK YOU