2017 ARROW

High Speed Converter (RF Sampling)

ARROW KOREA

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Texas Instruments

Agenda

- Introduction to RF Sampling
- Introduction to ADC32RFxx RF ADC
- Introduction to DAC38RF8x
- ADC32RFxx DDC Features
- RF Sampling Clocking

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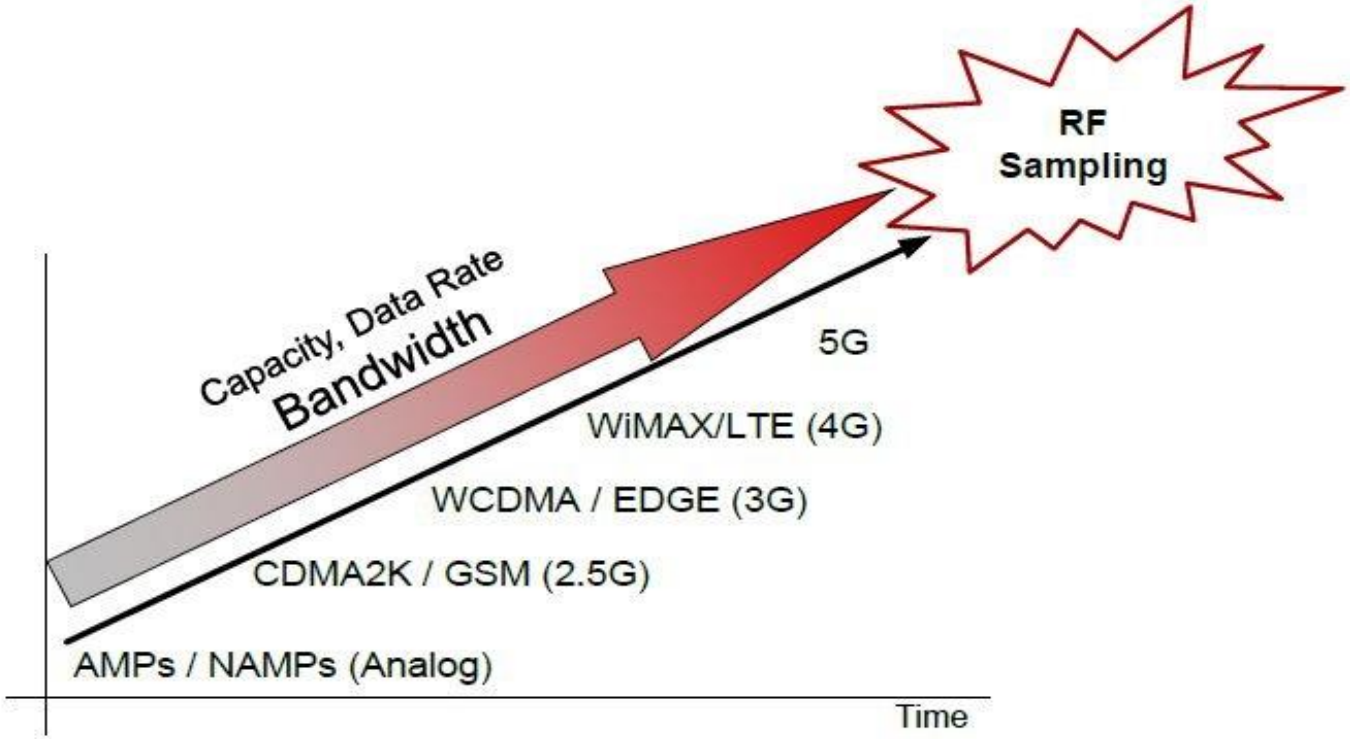
Introduction to RF Sampling

Communication Trend

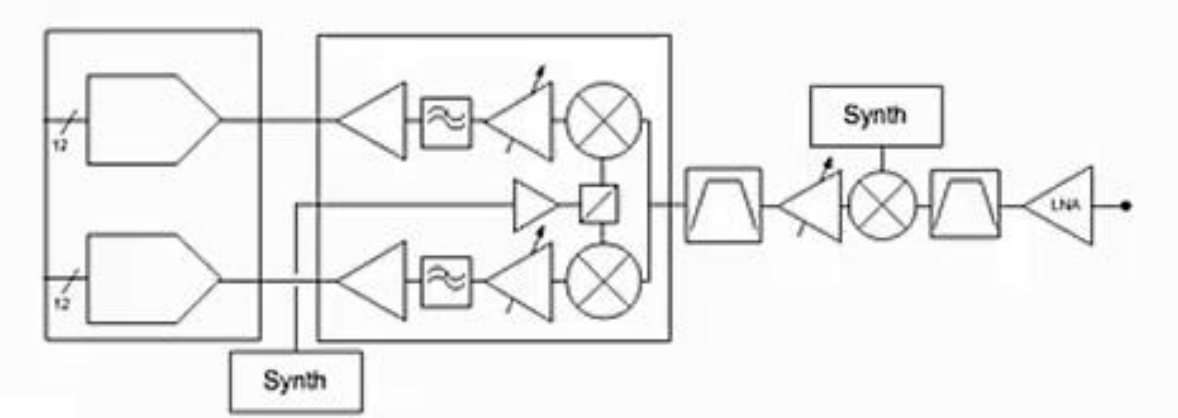
- **Communication Architectures morph to support:**
  - **Higher bandwidth systems**
  - **Lower cost systems**



Traditional Super Heterodyne Receiver

- **Traditional Architecture for measuring wide bandwidth signals**
  - **Mixer down-converts RF/μ-wave band to IF band**
  - **Quadrature Demodulator down-converts IF to BB**
    - **Utilize dual ADC to capture I/Q signals**
    - **ADC sampling speed needed to support half bandwidth of original signal**

- **Key Issues**
  - **1'st mixer stage tunes frequency to fixed IF band**
  - **BB I/Q amplitude/phase balance impact signal integrity**

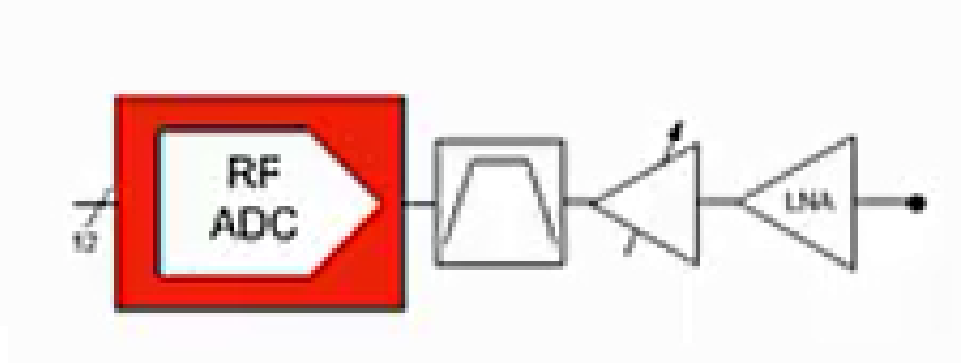


RF Sampling Receiver

- **Eliminate**
  - **Quadrature Demodulator**
  - **RF Synthesizer**

- **Replace: Dual ADC with one RF sampling ADC**

- **Supports:**
  - **Higher Signal Bandwidths**
  - **Direct sampling of RF bands**



RF Sampling Architecture

- **Spectral Performance**
  - **Support wide bandwidth signals (or multi-mode)**
  - **Support for very large bandwidths not previously obtainable due to ADC sampling rate limitations.**
- **Flexibility**
  - **Wide bandwidth signals, Multi-band applications, and DPD expansion bandwidth**
  - **Higher density systems (MIMO, Beam-forming, Radar Arrays)**
  - **Easier implementation for multiple standards or configurations (SDR)**
- **Size and Power dissipation**
  - **Size and power dissipation improvement by eliminating mixer, RF synthesizer, and BB signal conditioning components.**

Bandwidth Consideration

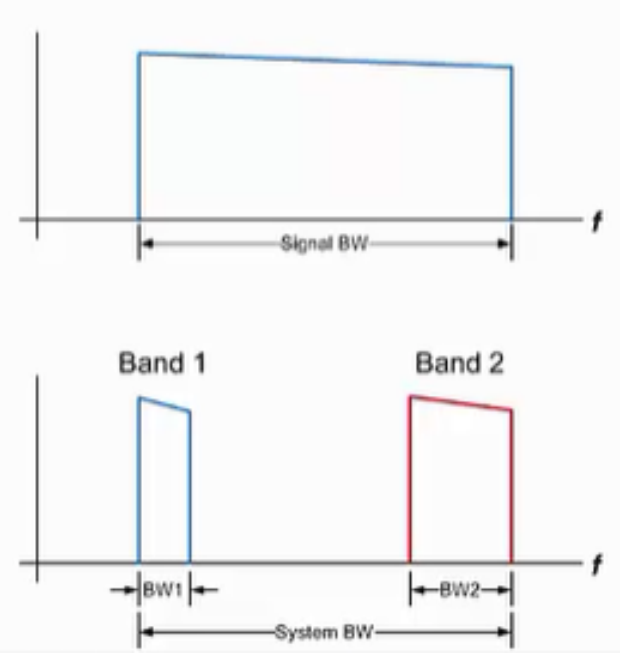
- Large BW signals support large data throughput and high capacity
  - How to support?
- Traditional architectures were limited by data converter sampling rate
  - Per Sampling Theorem, minimum sampling rate is at least 2x desired BW
  - Only alternative was to chop-up signal into smaller chunks for sampling
- RF Converters drastically increase sampling rate and thus can support much higher signal bandwidths
  - Very large signal bandwidths can be directly sampled
  - High frequency signals under-sampled to the first Nyquist zone
- Example:
  - 1 GHz of Spectrum requires minimum of 2 GHz sampling rate
  - For practical consideration, additional guard band is required

Bandwidth Considerations - Frequency

- **Sampling Theorem dictates that minimum sampling rate must be at least 2x desired bandwidth**
  - **In practice, more is required**

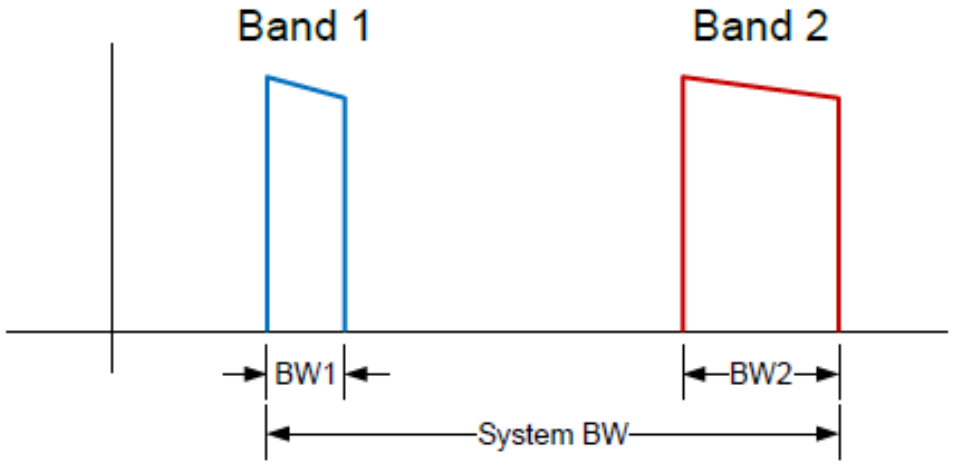
- **Case 1:**
  - **One large signal bandwidth**

- **Case 2:**
  - **Two or more smaller signal bandwidths separated in frequency**



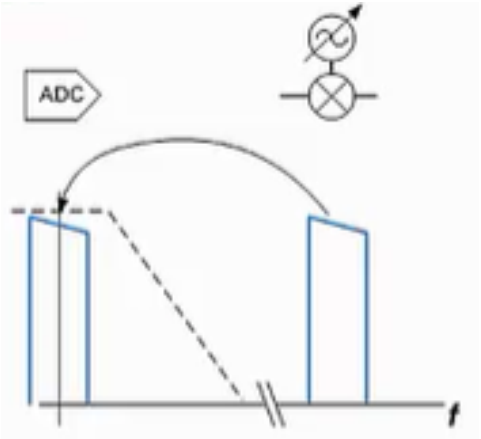
High Bandwidth - Multi-band Operation

- **Signal BW does not need to be contiguous**
  - **i.e. Two smaller BW signal separated in frequency can be considered as one larger signal BW**
- **RF Sampling solution provides a mechanism to support multiple bands, each with arbitrary signal bandwidth and with variable spacing**

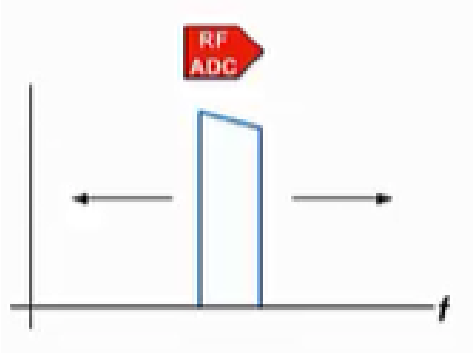


Frequency Flexibility - Tunable

- Frequency band tuning previously achieved with tunable RF synthesizer

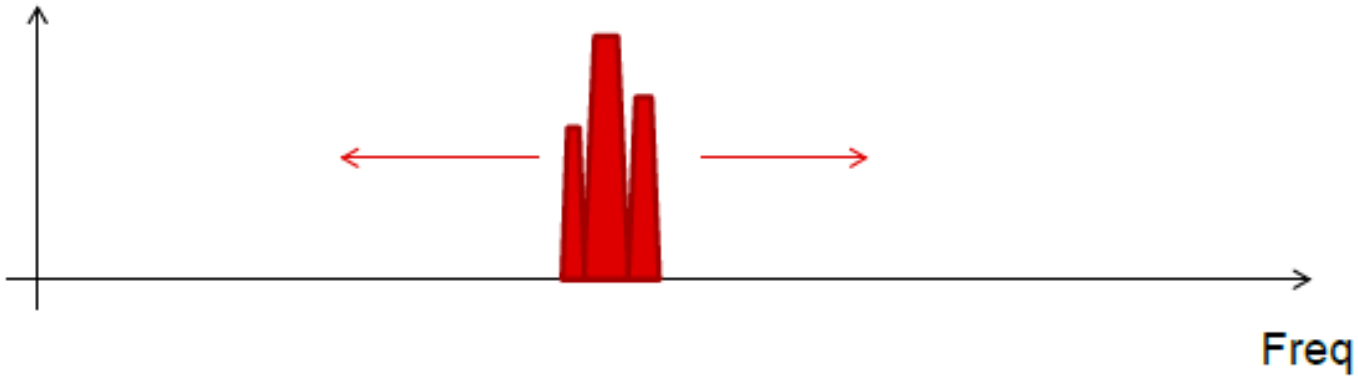


- RF Sampling can capture large bandwidth, so signal does not need to be down-converter to BB or specific IF band.
- Once captured, utilize digital converting means to get to signal information.
- Flexible signal capturing – don't need to know specifically where signal resides.



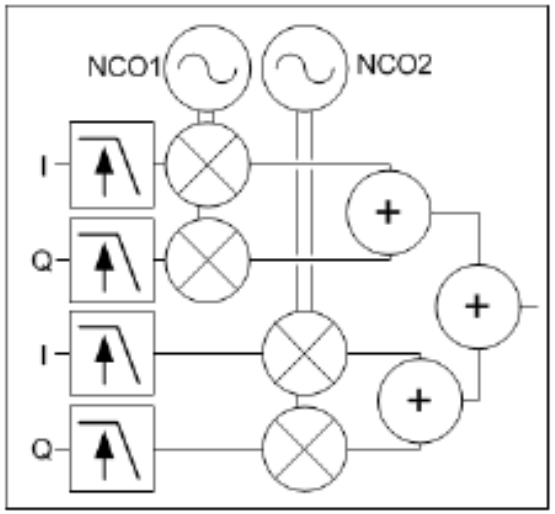
High Bandwidth - Tunable

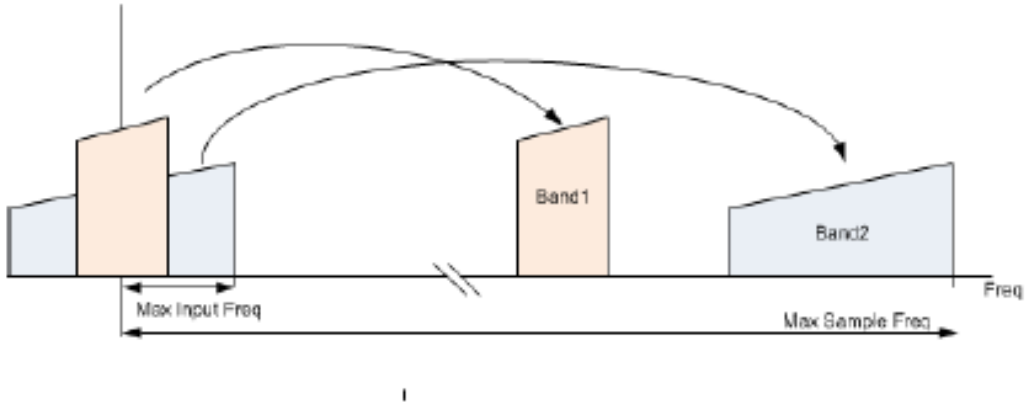
- **Allocated RF Frequency Band is pre-defined**
  - **i.e. defined from standards requirement, regulatory requirements, or from system specifications.**
- **Within the allocated band, desired signal can be assigned to specific (narrow band) channel.**
- **RF Sampling Solution provide mechanism to easily place/capture desired signal at any arbitrary channel.**



Multiple NCO – Multi-Band

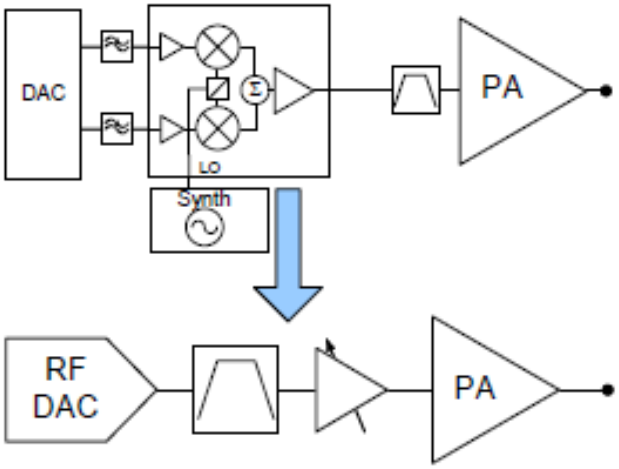
- Include multiple NCOs to tune separate channels to arbitrary RF frequency location
  - Supports non-contiguous multi-carrier operation
  - Supports multi-band or multi-mode operation
- Keeps input data rates low; sufficient to meet bandwidth requirements of each signal
- Supports very wide effective output bandwidth

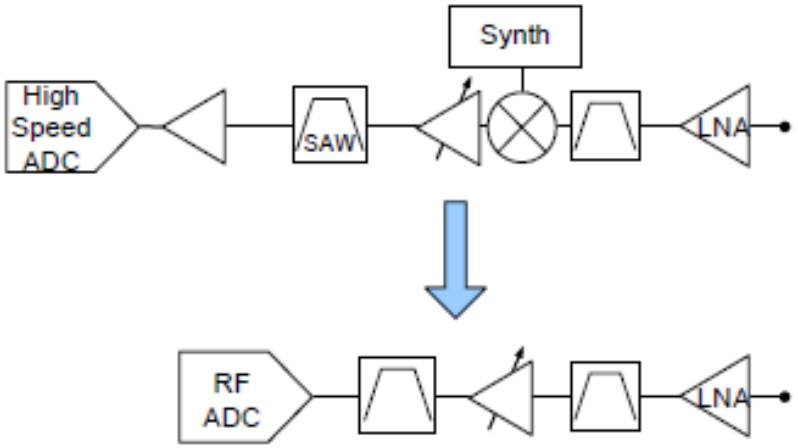




Transformation to RF Sampling Architecture

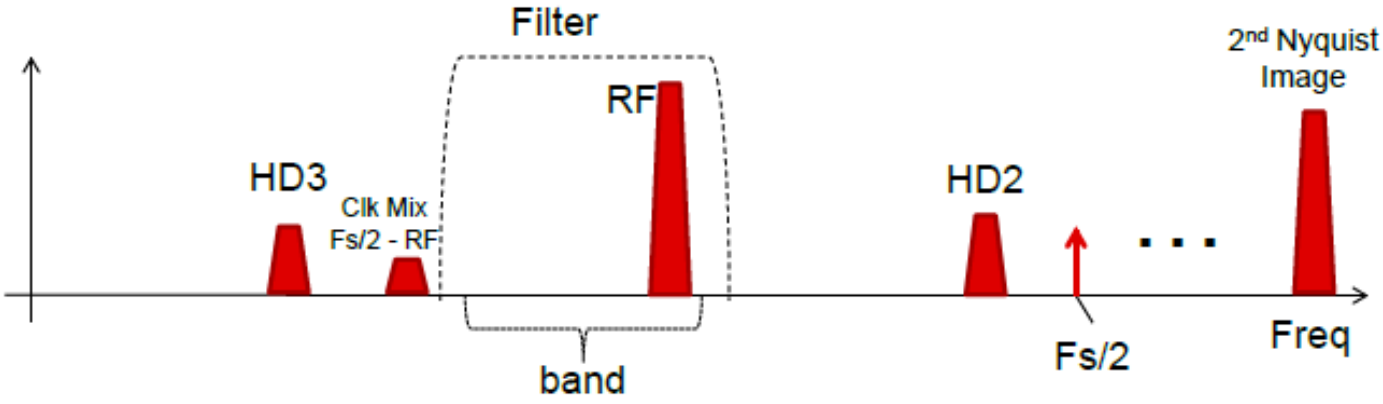
- **Transmitter**
  - **Eliminate IQ Modulator**
  - **Eliminate RF Synthesizer**
- **Receiver**
  - **Eliminate RF mixer**
  - **Eliminate RF Synthesizer**
  - **Eliminate IF channel filter**
  - **Transform IF VGA to RF VGA**





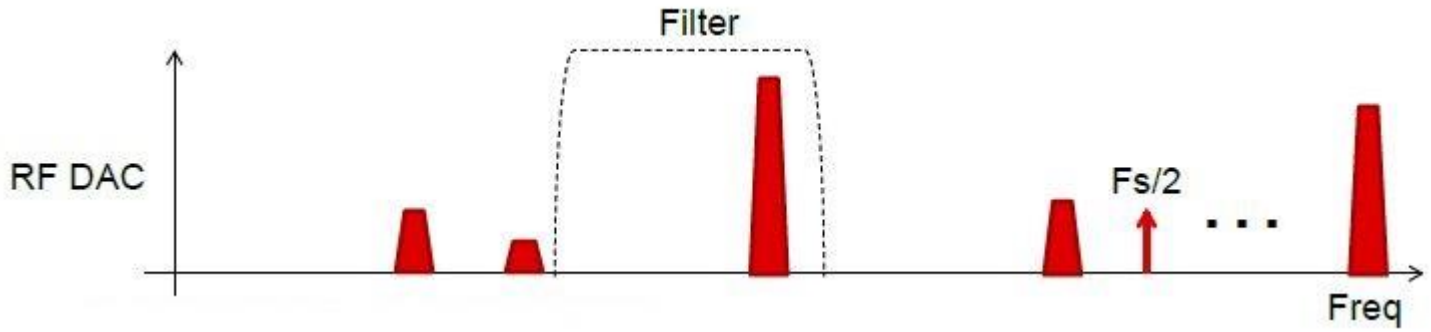
Reality of RF Sampling Transmitter

- **Ideal Transmitter: Fundamental signal at the frequency of interest**
- **Real World Impairments:**
  - **HD2 Component**
  - **HD3 Component (aliased)**
  - **Clock Mixing Spurious**
  - **Fs/2 Spur**
  - **Image Frequency in 2nd (and higher) Nyquist zone**
- **Analog filter added to minimize/eliminate spurious outputs**



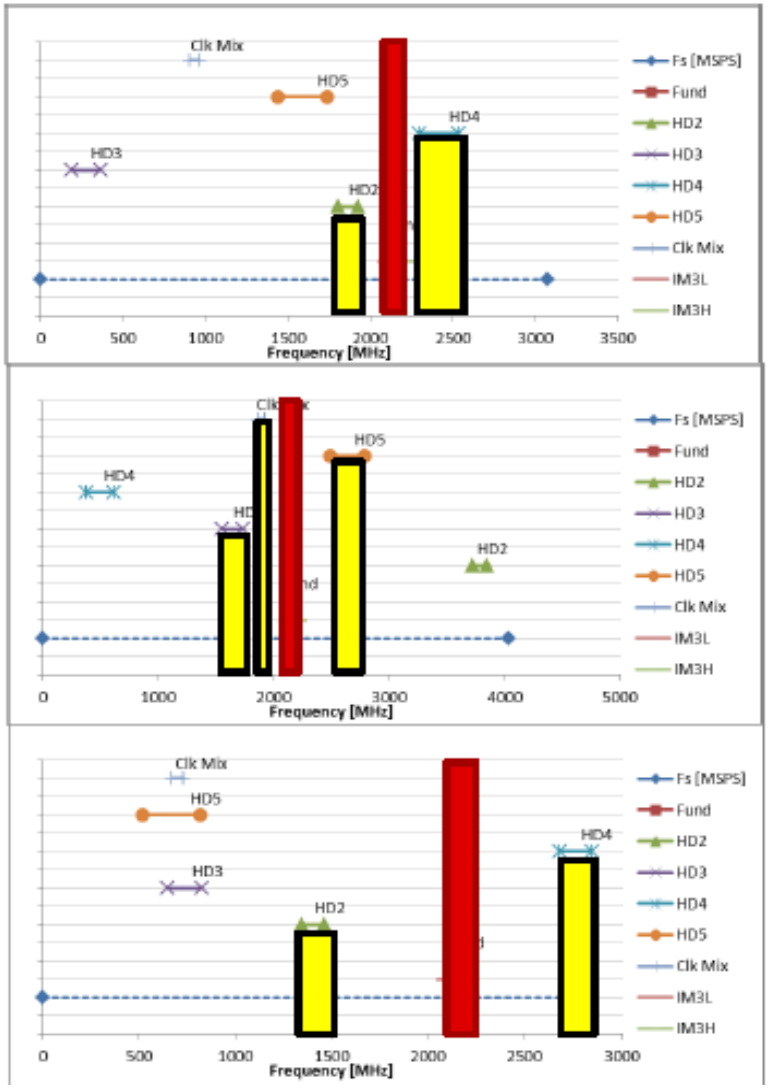
Strategy for Spectral Mask with RF DAC

- **Meeting in-band spectral mask**
  - No filtering is possible; inherent performance must meet mask
  - Frequency plan to move known spurious product outside of band
- **Meeting out-of-band spectral mask**
  - Optimize sampling rate to move spurious far away from desired band
  - Incorporate filtering to suppress out-of-band spurious from being transmitted
  - Farther the separation of spurious products, the easier to filter
  - With proper planning, filtering can be eliminated or relaxed compared to other architectures



TX Frequency Planning Example
RF = 2140 MHz; BW = 60 MHz

- Fs = 6144 MHz
- In-band is clear but HD2 and HD4 are close and hard to filter
- Increase sampling rate:
  - Fs = 8024 MHz
- In band still clear but HD3, HD5, and Clock mixing spur hard to filter
- Decrease sampling rate:
  - Fs = 5683.2 MHz
- In-band clear and lots of spacing to other spurious : easy filtering

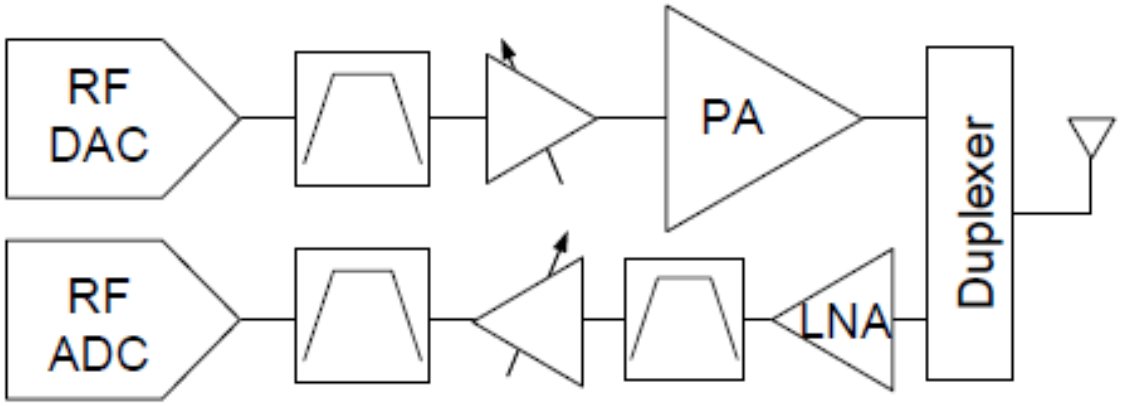


RF Sampling Transmitter Advantages

- **In-band Impairments: Better for wider bandwidth**
  - **Digital quadrature modulation eliminates sideband correction.**
    - **Higher BW signals yield more frequency dependent phase/gain mismatch**
    - **More difficult to correct in traditional architecture**
  - **More consistent Gain/Phase vs. Frequency than with analog BB or IF filter**
- **Power dissipation**
  - **Potential for improvement over discrete approach depending on implemented features and sampling rate.**
- **Size (PCB Real Estate)**
  - **80% size reduction over discrete IF solution**
  - **50% size reduction vs. MCM IF solution**
- **Better for…**
  - **Wide bandwidth signals and Multi-band applications**
  - **Higher density systems (MIMO, beam-forming)**
  - **Easier implementation for new markets, requirements and frequency bands**

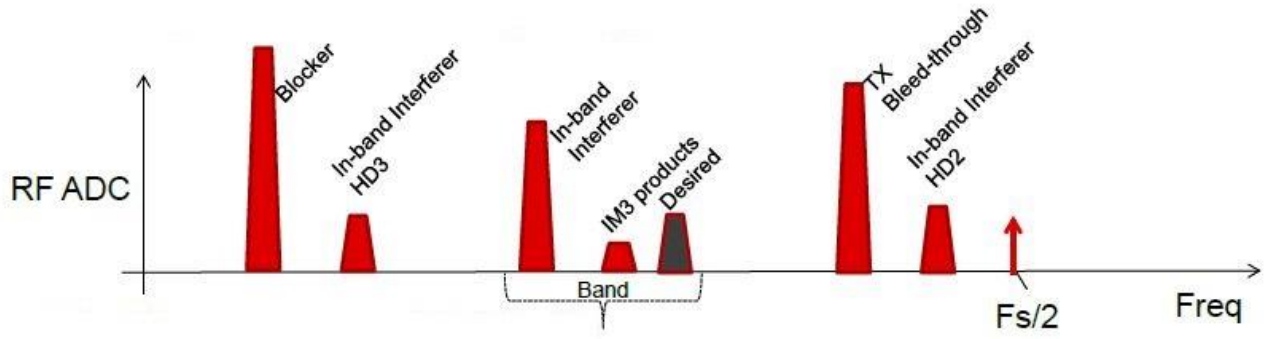
RF Sampling Receiver

- All signals alias down into the first Nyquist zone
- Ideal RF Sampling ADC directly captures desired band
- ADC must balance dynamic range
  - Need low noise floor (good SNR) to capture desired low power received signal
    - Maintain Sensitivity requirements
  - Need to handle high amplitude level from blocker or TX bleed-through so that ADC is not overdriven and distorted.
    - Maintain blocker/jammer requirements



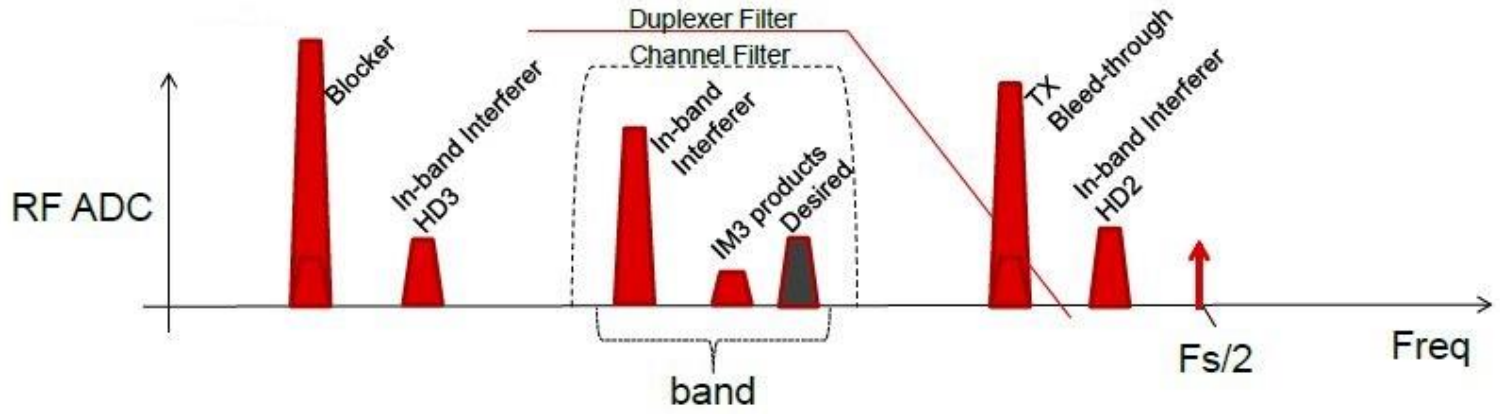
Reality of RF Sampling Receiver

- **Real World Spectral Impairments**
  - Spurious signals (i.e. IM3, HD2, HD3 etc.) from in-band interferers generated in analog chain (i.e. LNA, VGA)
  - Out-of-band Interferers from Blockers/Jammers
  - TX signal bleed-through to the RX path
  - IM3 Mixing products between Jammers and TX bleed-thorough
- **Real World Overdrive Impairments**
  - TX Bleed-through
  - Blockers/Jammers
- **Broadband Noise folding into 1st Nyquist Zone**



Strategy for Maintaining Sensitivity RX

- **Duplexer Filter**
  - Suppresses TX Bleed-through into receiver
  - Eliminates IM3 Spurious generation
- **Channel Filter**
  - Suppress out-of-band spurious generated from in-band interferers
  - Suppress Blocker signals
  - Suppress harmonic/mixing spurs from blocker(s)
- **Anti-aliasing filter to eliminate broadband noise**

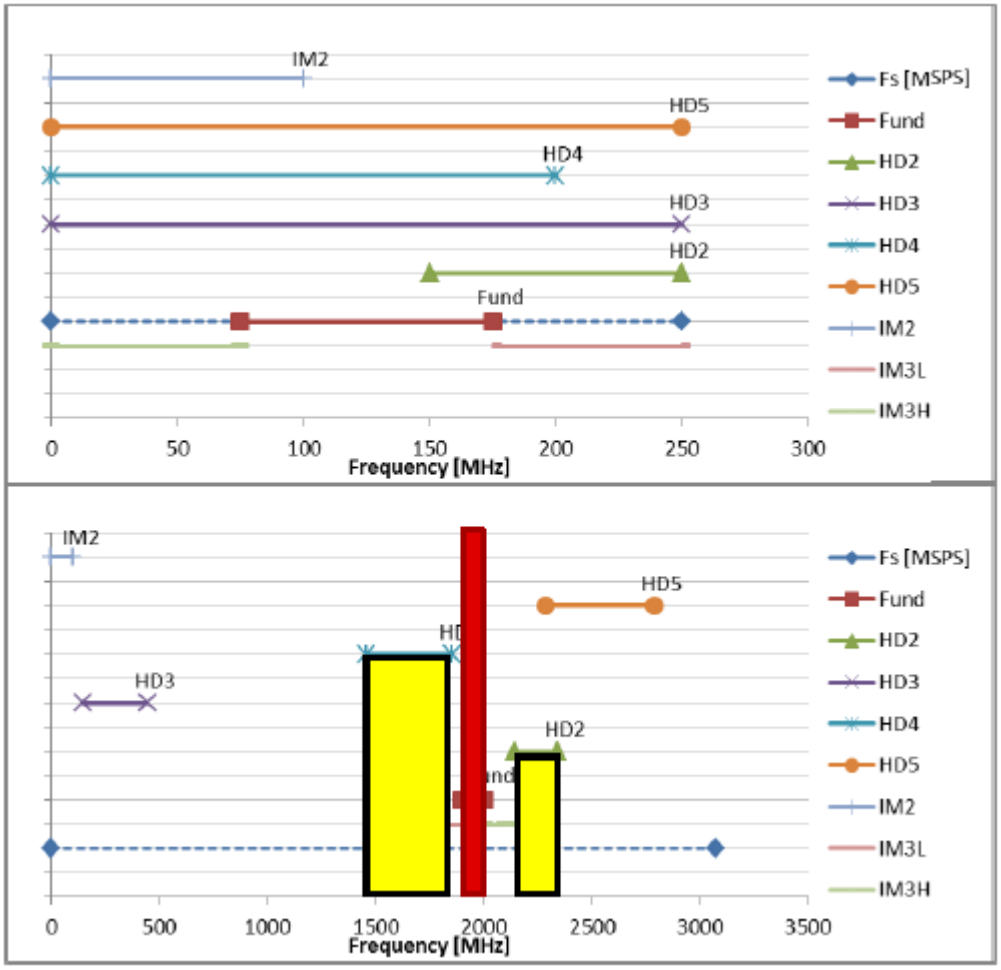


RF Sampling ADC - Frequency Planning

- **Spurs from out-of-band interferers or TX bleed-through**
  - **Proper filtering can minimize or eliminate these threats**
- **Spurs from in-band interferers**
  - **Can not filter these signal out**
- **Need to frequency plan around**
- **Higher sampling rate affords flexibility in frequency planning around troublesome harmonic and spurious products**
- **Frequency planning in High IF systems**
  - **Choose available sampling rate converter**
  - **Optimize IF location for best results**
- **Frequency Planning in RF Sampling**
  - **Can not choose location of RF signal; this is fixed**
  - **Optimize sampling rate to achieve best results**

Frequency Planning Example

- **Case 1: High IF Sampling**
  - **Fs = 500 MHz**
  - **IF = 375 MHz**
  - **BW = 100 MHz**
- **Can not escape from aliased HD2 and higher harmonics**
- **Case 2: RF Sampling**
  - **Fs = 6144 MHz**
  - **BW = 100 MHz**
  - **RF = 1950 MHz**
- **Higher order harmonics do not fall in band**



RF Sampling Receiver Advantages

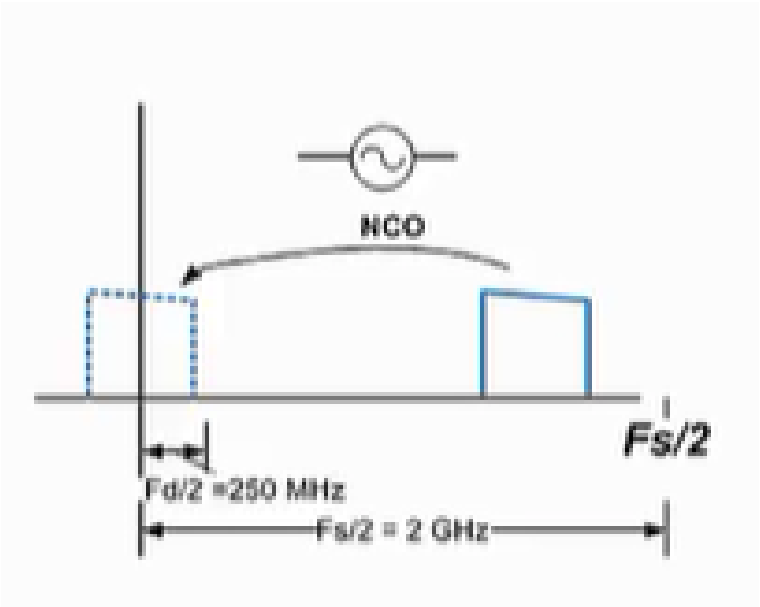
- **Spectral Performance**
  - Support wide bandwidth signals (or multi-mode)
  - Frequency agile
  - Digital features like decimation can minimize filter requirements
- **Power dissipation**
  - Power dissipation improvement possible by eliminating mixer and RF synthesizer components (depending on digital features/sampling rate).
- **Size (PCB Real Estate)**
  - Size reduction over discrete IF solution
- **Better for…**
  - Wide bandwidth signals, Multi-band applications, and DPD feedback
  - Higher density systems (MIMO, beam-forming)
  - Easier implementation for multiple standards

Input Data Rates

- Higher sampling rates required for sampling at RF and for frequency planning around spurious
- Data rates can not operate at those speeds
  - Limited by processor or FPGA rate
  - Limited by available I/O on the device
- Implement
  - Interpolation/Decimation in order to keep data rates reasonable
  - NCO (Numerically Controlled Oscillator) to move desired signal to any required band
- Rule of thumb:
  - Select data rate to support bandwidth of the signal
  - Select sampling rate to support output frequency band and spectral purity

RF Sampling Example

- **System Specifications**
  - Signal BW = 400 MHz
  - Center Frequency = 1.5 GHz
- **ADC Specifications**
  - Fs (Sampling Freq) = 4 GPSP
  - Fd (Data Rate) = 500 MSPS
  - Decimation = /8
  - NCO = 1.5 GHz



- **Data/Sample Rate Rule-of-Thumb**
  - Input data rate determined by signal BW
  - Output sample rate determined by RF frequency
- **Benefit: Flexibility to capture signal at arbitrary center frequencies**

System Challenges for RF Sampling

- **Digital Interface**
  - High data rates needed to support high bandwidth signals
  - Incorporate interpolation/decimation filters to maintain reasonable rates
- **Clocking**
  - Requires high frequency, low phase noise sampling clock
    - Challenging to generate and route across board
    - Challenging for multi-device synchronization
  - Incorporate an optional internal PLL/VCO to generate required clock on-chip
- **Spectral Performance**
  - Low order harmonics
    - Frequency plan around troublesome spurious when possible
    - Maintain low spurious generation where frequency planning not possible
  - High order harmonics
    - Cannot frequency plan around these
    - Must rely on design to meet requirement

Overall System Benefits for RF Sampling

- Support higher bandwidth signals that were previously not possible
- Support for a frequency agile architecture
  - One design can service many bands, standards, etc.
- Digital features allow for additional flexibility in controlling the signals and manipulating the channel
- Filtering schemes can be relaxed in many cases and potentially eliminated
- Multiple devices/line-ups can be more easily synchronized together to build more complex systems
  - Large Radar Arrays
  - Beam-forming Antennas
  - Massive MIMO

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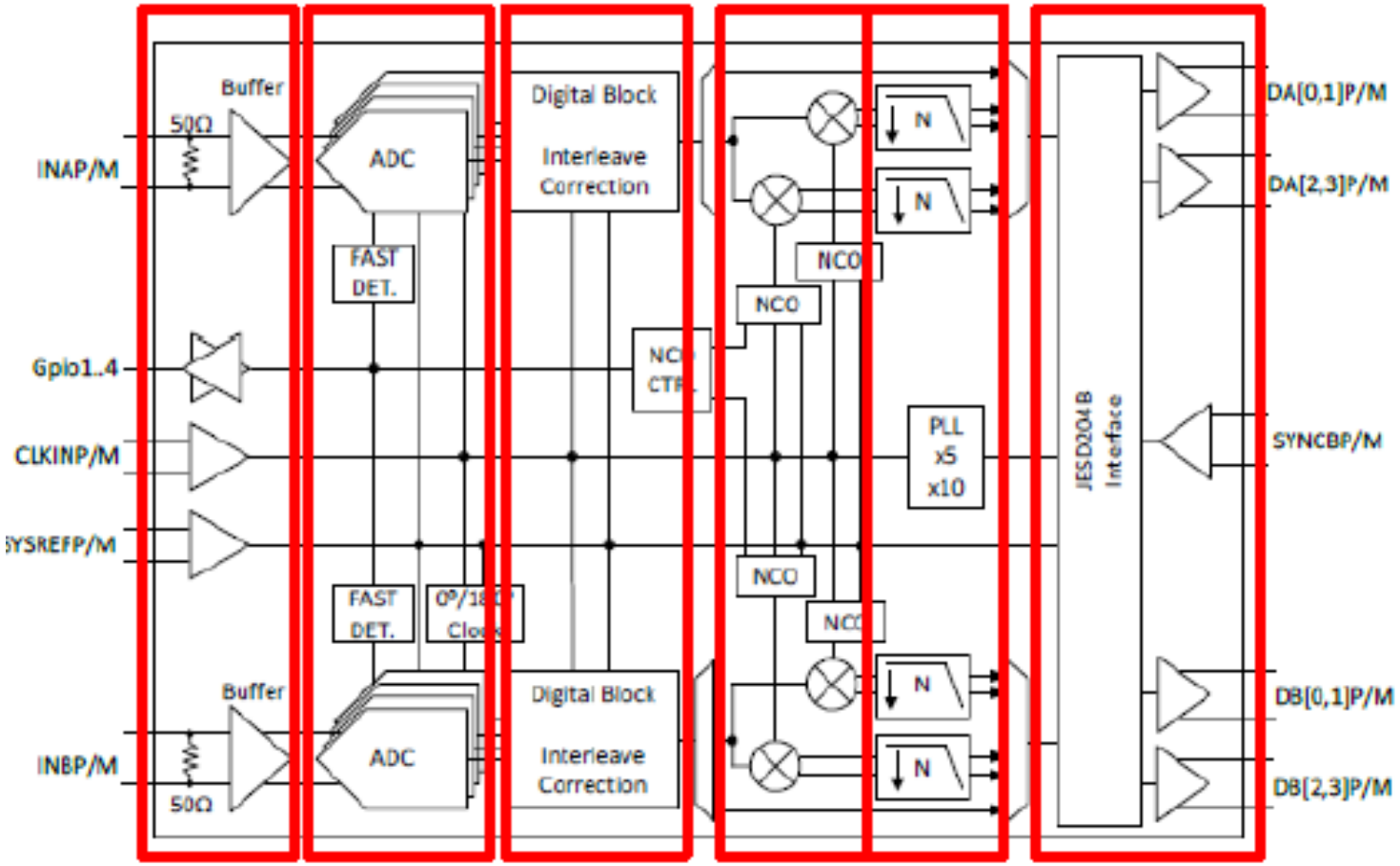
Introduction to ADC32RFxx RF ADC

ADC32RFxx Product Overview

- **Two main families**
  - **ADC32RF45 Dual-channel, 14-bit, 3GSPS**
    - **Supports Bypass mode (operation with full Nyquist bandwidth)**
    - **Supports full DDC (Digital Down Converter) modes**
  - **ADC32RF80 Dual-channel, 14-bit, 3 GSPS**
    - **Supports only DDC modes (decimation /4 to /32)**

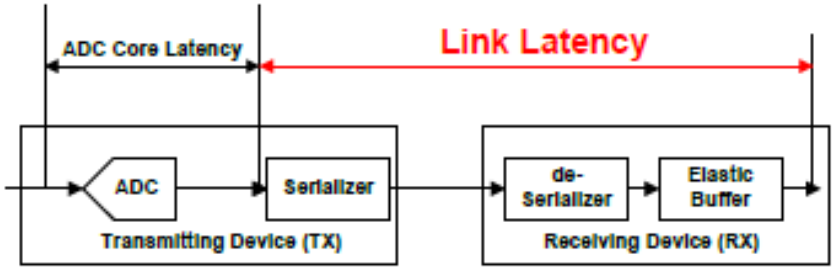
ADC32RF4x Family		
Device	# of DDC	Speed Grade
ADC32RF45	2	3.0 GSPS
ADC32RF44	2	2.5 GSPS
ADC32RF43	2	2.0 GSPS
ADC32RF42	2	1.5 GSPS
ADC32RF41	2	1.0 GSPS
ADC32RF8x Family		
Device	# of DDC	Speed Grade
ADC32RF80	2	3.0 GSPS
ADC32RF83	1	3.0 GSPS

ADC32RFxx Block Diagram



JESD204B Interface

- **JESD204B SerDes (Serializer/De-serializer) standard provides a widely adopted interface for transferring a large amount of data**
  - **Data is parsed over specified number of lanes**
  - **Uses 8b/10b encoding for synchronization, clock recovery, and DC balance**
  - **Standard supports up to 12.5 Gbps lane rates**
  - **Provisions to support deterministic latency across the serialized link**
- **Key clocking requirements**
  - **Sample clock: sampling clock and reference for all other system timing**
  - **SysRef:**
    - **Source synchronous to the sample clock**
    - **Provides phase reference for SerDes frame clocks**



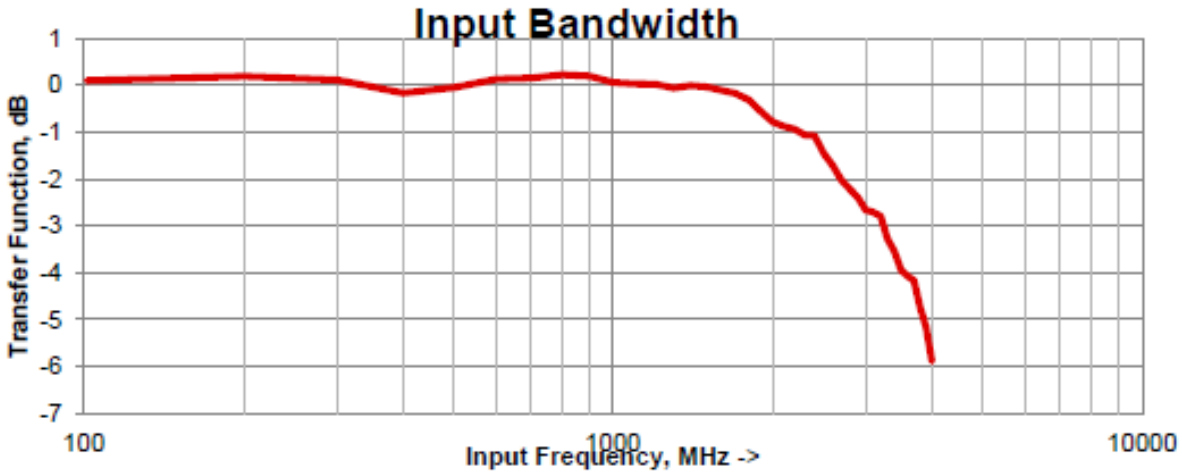
JESD204B Interface – Key Parameters

- **Key Data Converter Parameters: LMFS**
  - L # of lanes per converter device
  - M # of converters per device
  - F # of octets per frame (per lane)
  - S # of samples per converter per frame clock cycle
- **SerDes speeds may vary for each of the LMFS mode**
  - Fewer lanes increases lane rate
  - More decimation decreases lane rate
  - FPGA clocking will often be 1/10 to 1/40 the lane rate
- **Data Sheet provides lane mapping for desired modes/lanes**
  - "L" = up to 8 lanes at 12 Gbps max rate
  - "M" = 2, 4, 8 effective converters
    - M= 2 Bypass mode
    - M= 4 Single DDC, complex mixer
    - M= 8 Dual DDC, complex mixer

Decimation Setting (complex)	# of Active DDCs	Output Complex/ Real	L	M	F	S
/ 4		Complex	8	4	1	1
		Complex	4	4	2	1
/ 6		Complex	8	4	1	1
		Complex	4	4	2	1
/ 8		Complex	4	4	2	1
		Complex	2	4	4	1

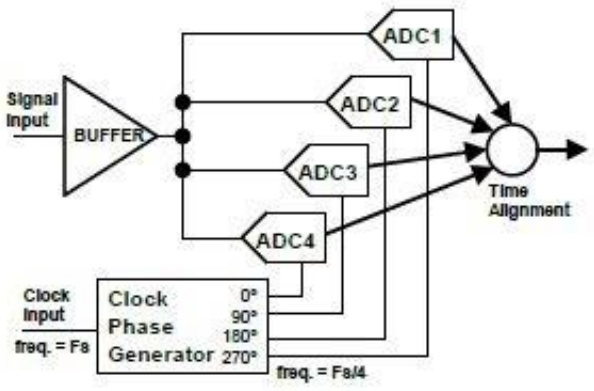
Input Buffer

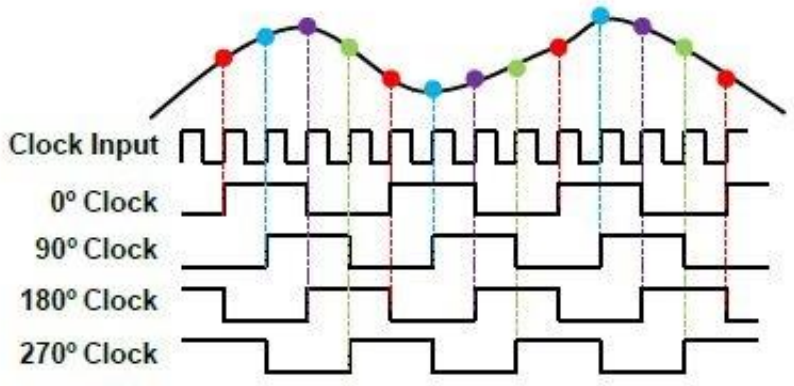
- Differential Input buffer impedance: 50 ohms
- Recommend high frequency 1:1 balun/transformer with good phase balance across the frequency of operation
- Input bandwidth capability: 3 GHz
  - Support 1st and 2nd Nyquist bands directly
  - Support 3rd Nyquist up to 4 GHz with degraded performance



Interleaving

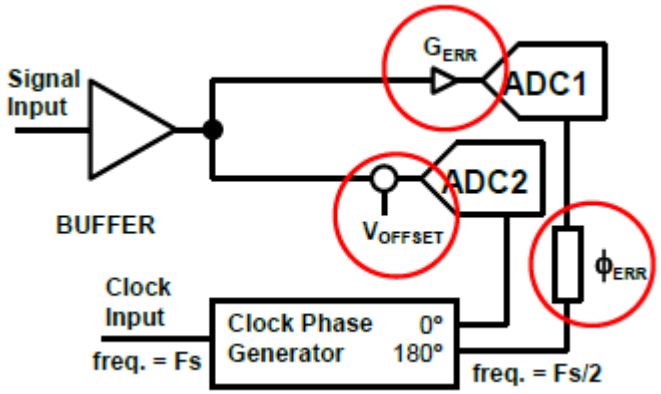
- Interleave four 750 MSPS ADC cores = 3 GSPS
- Clock distribution handled on-chip
  - ADC cores sample at same divided frequency but at different phase offsets
  - Digital outputs are re-aligned in time
- Why Interleave?
  - Utilize ADC core with good SNR/SFDR performance
  - Combine to achieve high sampling rate & high bandwidth capabilities

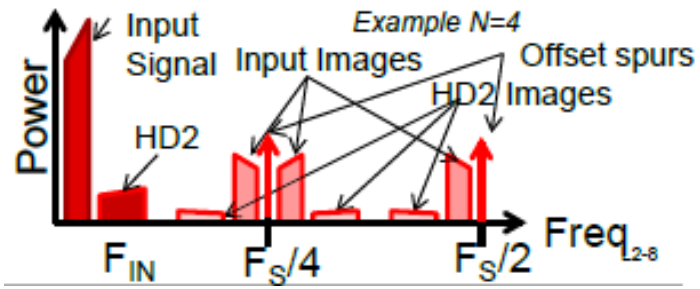




Non-ideal Interleaving

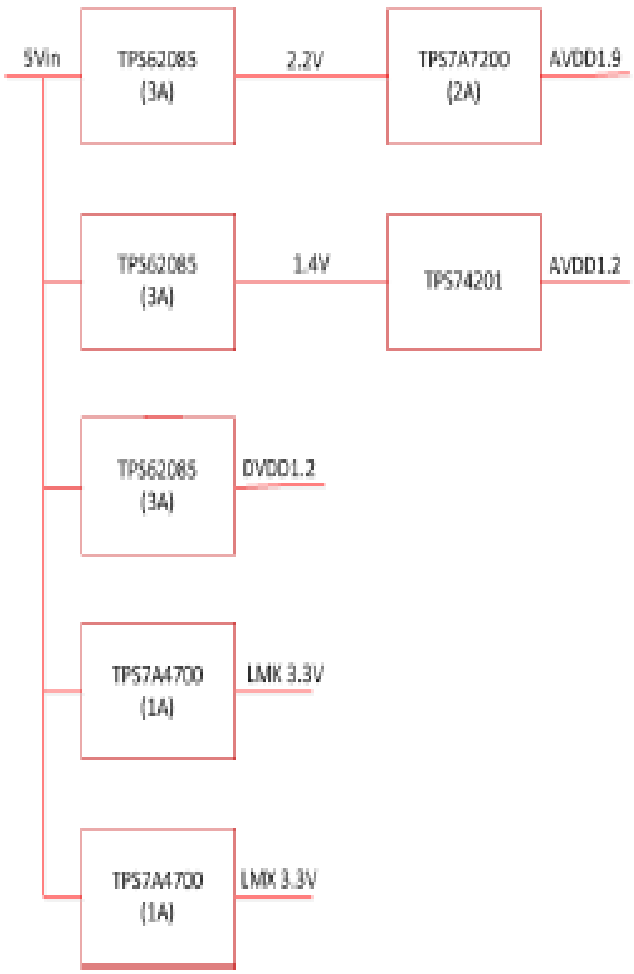
- **Offset Errors**
  - Mismatched ADC core voltage offset
- **Amplitude Errors**
  - ADC core gain error
  - ADC reference voltage error
- **Phase Errors**
  - Input routing delay
  - Input BW difference
  - Clock phase error or imprecise sampling instant
- **Interleaving errors create unwanted spurs and images**
  - Offset Errors => spurs at Fs/2, Fs/4
  - Amplitude/Phase => images
- **Digital Correction Block**
  - Continuous digital interleave adjustment
  - Maintain IL spur < 80 dBc at 2.1 GHz





DC Power Considerations

- **ADC Power rails**
  - **Analog: 1.9 V**
  - **Analog: 1.2 V**
  - **Digital: 1.15 V**
- **Power management strategy**
  - **Option 1: (most conservative)**
    - **DC-DC convert to intermediate voltage**
    - **LDO convert to required rail**
  - **Option 2: (minimum power dissipation/cost)**
    - **DC-DC convert to required rail**
    - **Ensure switching spurs/noise do not cause system issues**
    - **Improve supply filtering as needed**
- **Power Dissipation: ~6W**
  - **Dependent of sampling frequency and mode**
  - **Heat sink recommended L2-9**



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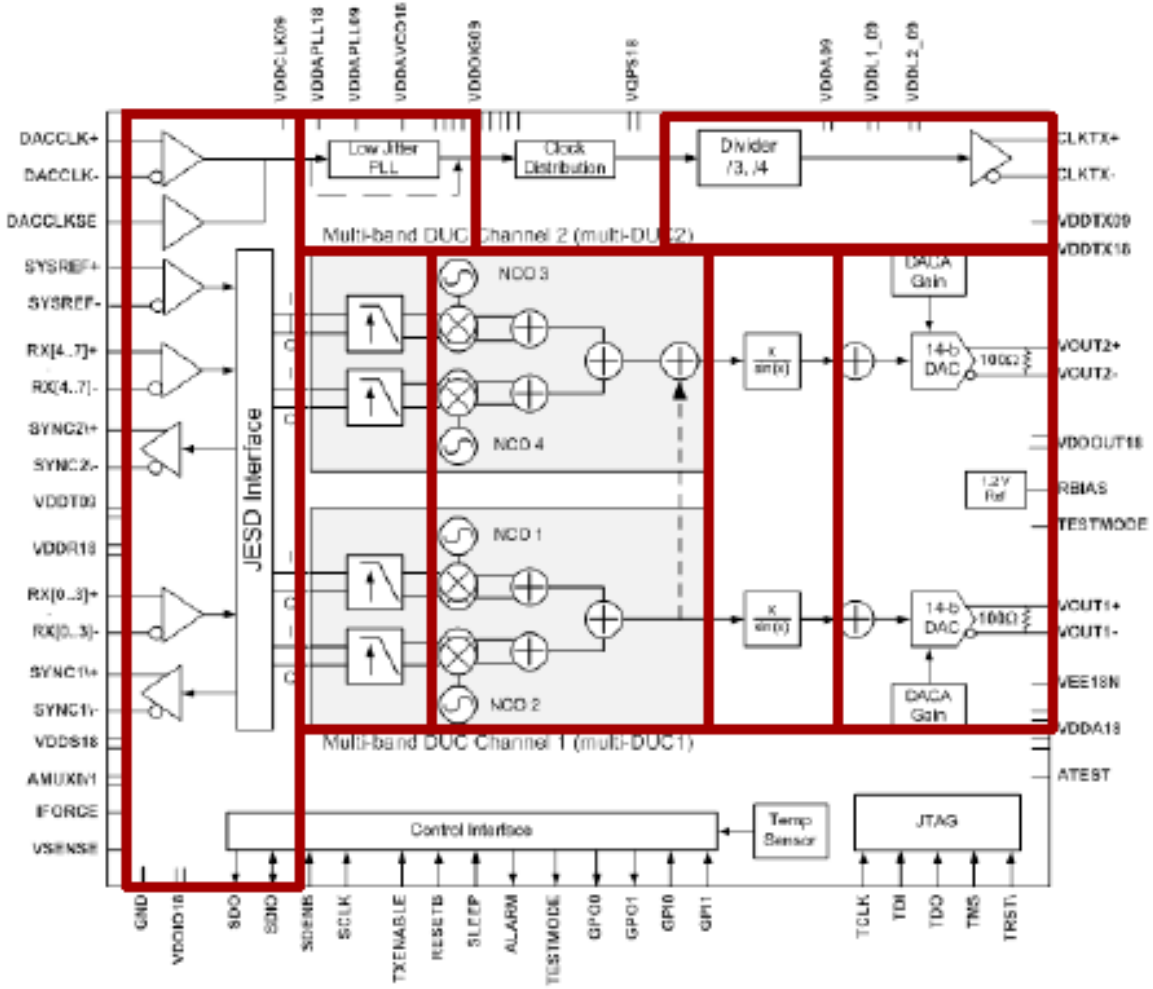
Introduction to DAC38RF8x

DAC38RF8x Product Overview

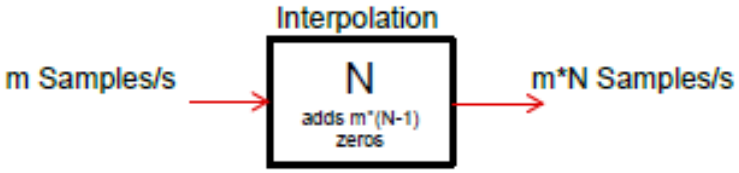
	DAC38RF80	DAC38RF82	DAC38RF83
Channels	2	2	2
Output Interface	SE	DIFF	DIFF
Output Frequency Range	700-2700 MHz	100 - 4500 MHz	100 - 4500 MHz
Resolution	16, 12	16, 12, 8	16, 12
Min Interpolation	6x	1x	6x
Max Interpolation	24x	4x	24x
Maximum Signal BW	750 MHz	1600 MHz	750 MHz
Integrated Balun	Yes	No	No
Integrated PLL	Yes	Yes	Yes
Coarse Mixer	Yes	Yes	Yes
48-bit NCO	Yes	Yes	Yes
JESD204B Interface	Yes	Yes	Yes
Max SerDES Rate (Gbps)	12.5	12.5	12.5

Anatomy of RF DAC



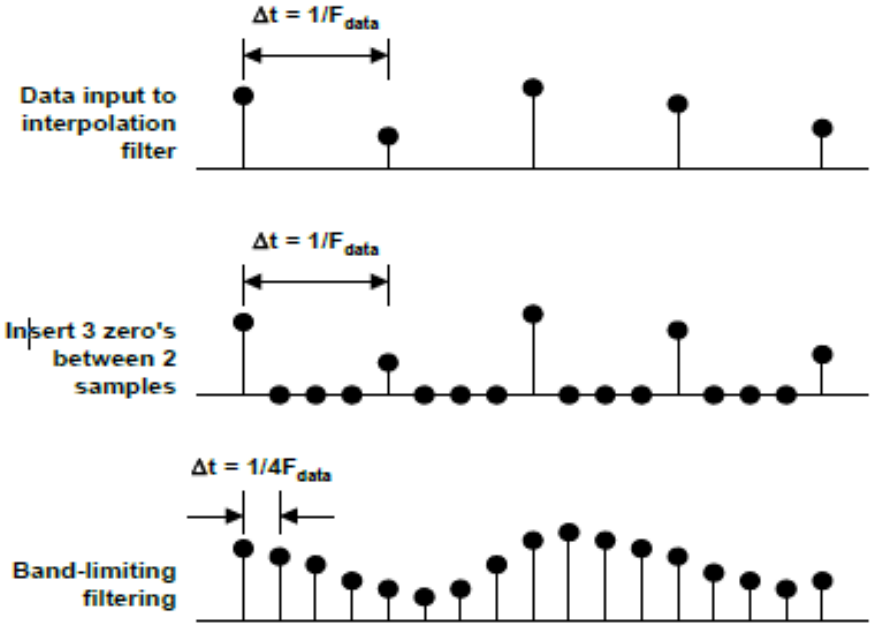
What is Interpolation?

- Interpolation increases the sample rate of a signal without affecting the signal itself
  - Insert a 0 between each sample (zero stuffing / up sampling)
  - Filter the resulting images from the up sample process
- Interpolation is used to:
  - Maintain reasonable input data rates; achieve higher output frequencies
  - Shift the DAC images further from the band of interest…easier filtering
  - Allow for a wider Nyquist zone for more flexible frequency planning
  - Reduces NSD as quantization noise is spread over a wider Nyquist band
- Input BW limited by interpolation filters
  - BW = 0.4 * Fdata



Time Domain View of Interpolation

- 0's are inserted between the original samples
  - Adding a 0 does not change the spectral content, just sampling frequency
  - Widens the unique BW of the signal
- Low-pass (band-limiting) filtering fills in the missing levels between the original samples



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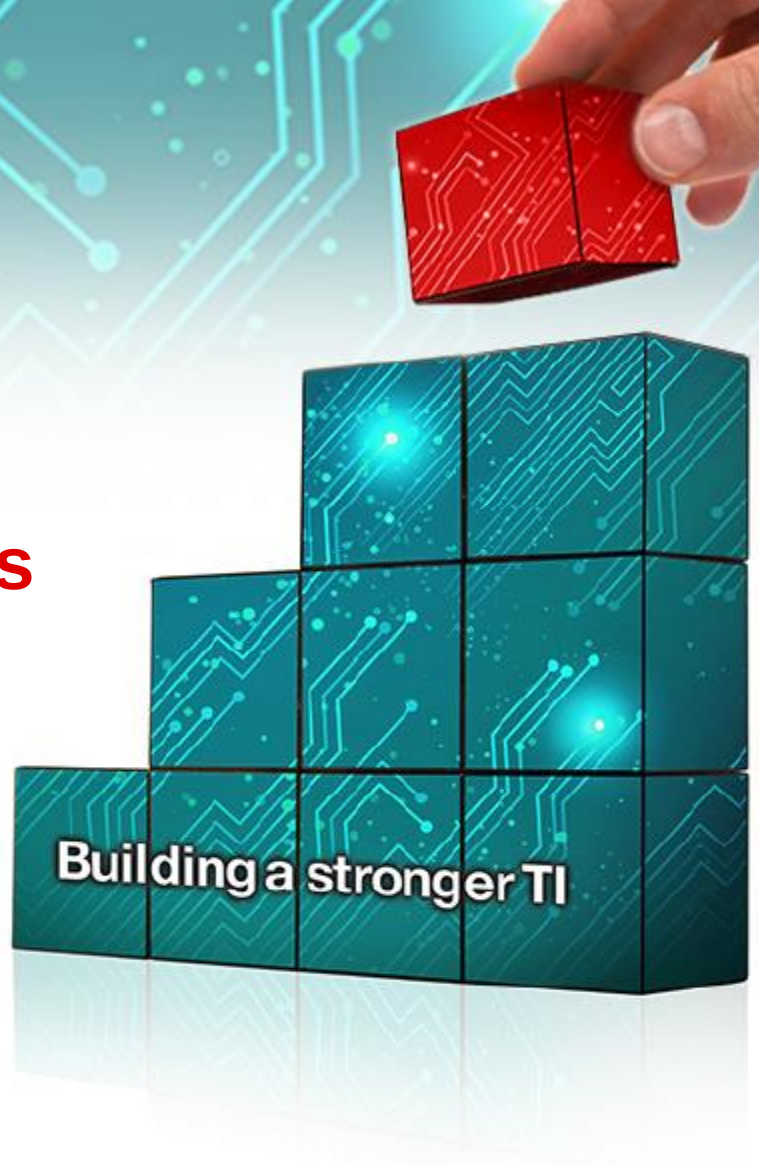
ADC32RFxx DDC Features

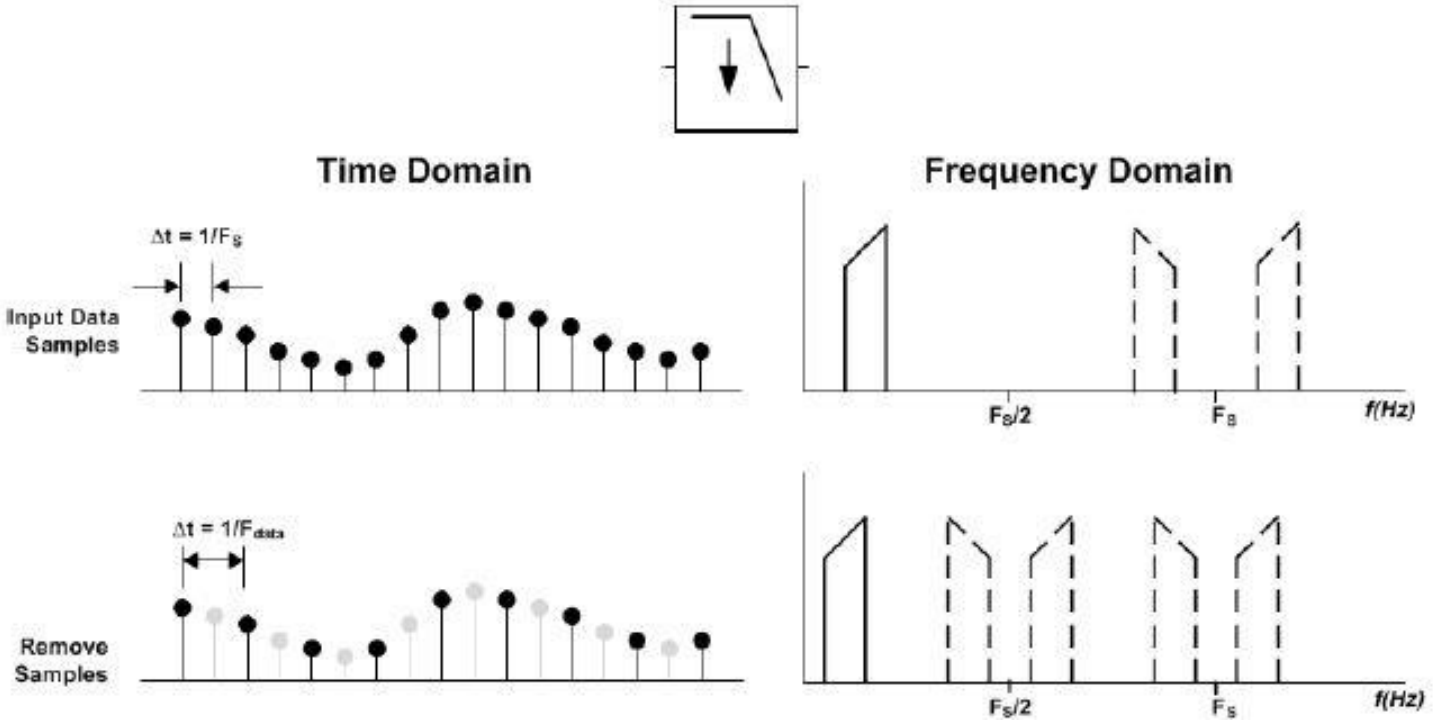


What is Decimation?

- Decimation decreases the sample rate of a signal by removing samples from the data stream
- Decimation includes digital low pass (anti-aliasing) filter followed by a decimator
  - The operation is equivalent to utilizing an analog anti-aliasing filter at fc = FS /2M and sampling a converter at Fd = FS /M, where M = decimation count (i.e. 2)
- Decimation is used to:
  - Decrease the ADC data rate to reasonable levels for data capture
  - Maintain high output sampling rate for more flexible frequency planning
  - Take advantage of decimation filtering for improved spectral performance

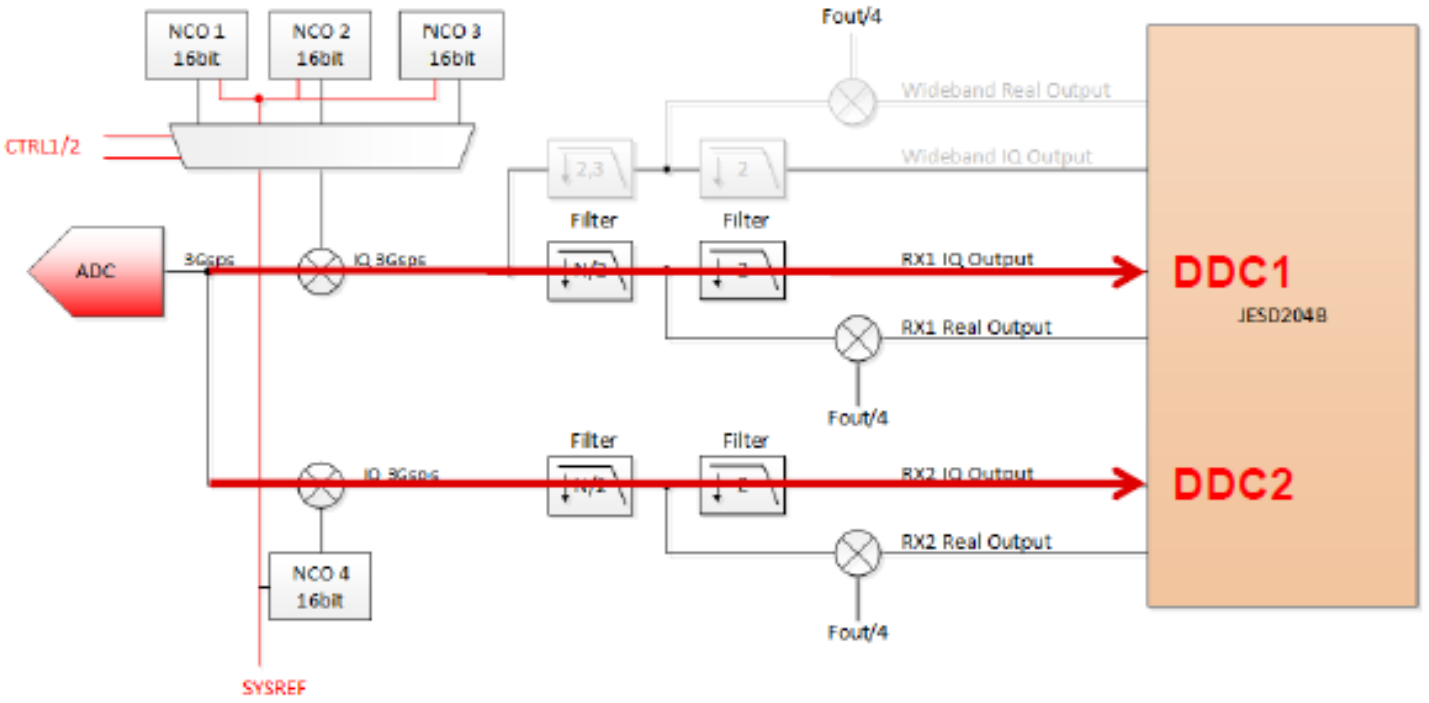
Time/Freq Domain View of Decimation

- Images created with each decimation
- Low Pass filter provides anti-aliasing protection
- Data rate reduced for easier processing



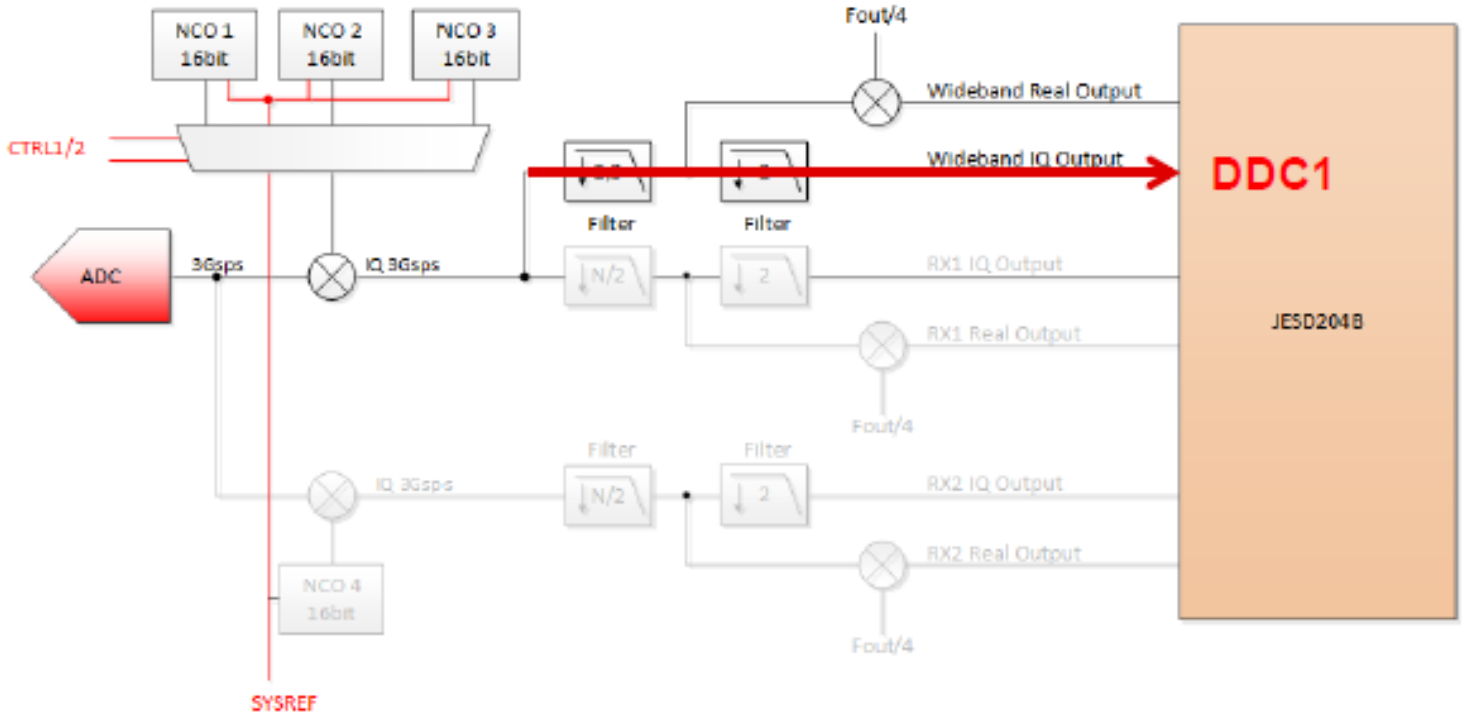
Digital Down Converter (DDC) - Receiver

- **Single or Dual complex Digital Down Converter**
- **Decimation modes: 8, 9, 10, 12, 16, 18, 20, 24, 36**



DDC – Wideband Receiver

- **Decimation modes: 4, 6**
- **Signal bandwidth: 750 MHz, 500 MHz**



Key Decimation Advantage

- **Decimation provides SNR processing gain**
- **Frequency Domain View**
  - **Signal remains constant**
  - **Noise power is reduced by decimation filter**
  - **Improved SNR performance**
- **Time Domain View**
  - **Form over averaging samples to reduce overall noise**
- **Decimation "Penalty"**
  - **Increased digital power consumption**
  - **Reduced signal bandwidth capability**

Decimation Setting	# of DDCs available per Channel
/ 4 complex	1
/ 6 complex	1
/ 8 complex	2
/ 9 complex	2
/ 10 complex	2
/ 12 complex	2
/ 16 complex	2
/ 18 complex	2
/ 20 complex	2
/ 24 complex	2
/ 32 complex	2

NCO (Numerically Controlled Oscillator)

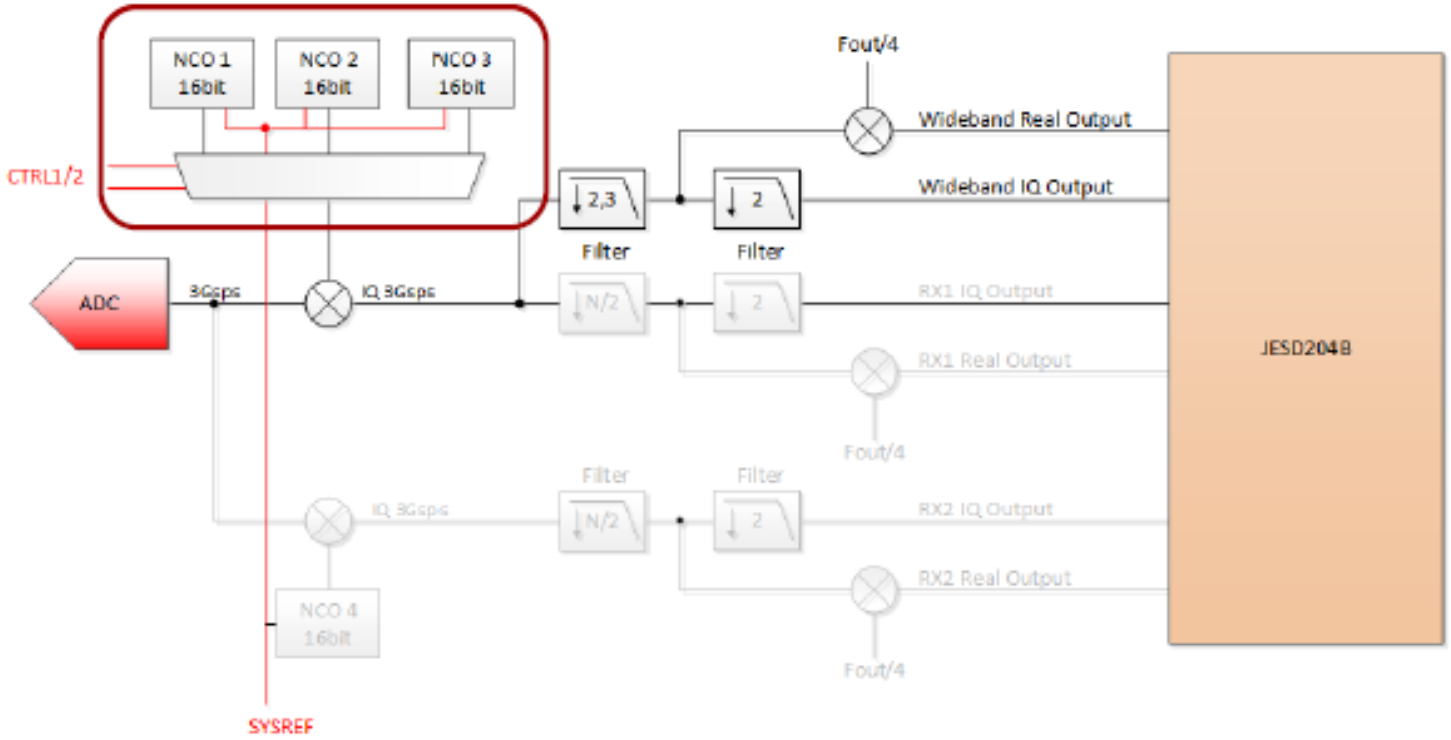
- Total of 4 NCOs per channel
- NCO frequency is set as a fraction of sampling frequency (Fs)
- Each NCO has a 16-bit control value (Freq[n])

$$F_{NCO} = \frac{NCO\ Freq\ [n] * FS}{2^{16}}$$

- NCO frequency step size: Fs/65,535 = ~45.776 kHz at 3 GSPS
- DDC0 employs 3 switchable NCOs
  - Each NCO can be pre-set via (slow) SPI control
  - NCO switched by external GPIO quickly
  - Supports switching between multiple DPD feedback channels

Wideband DPD Feedback Example

- Utilize NCO 1, 2, 3 to program to DPD feedback channels
- Employ wideband I/Q output to capture expansion bandwidth



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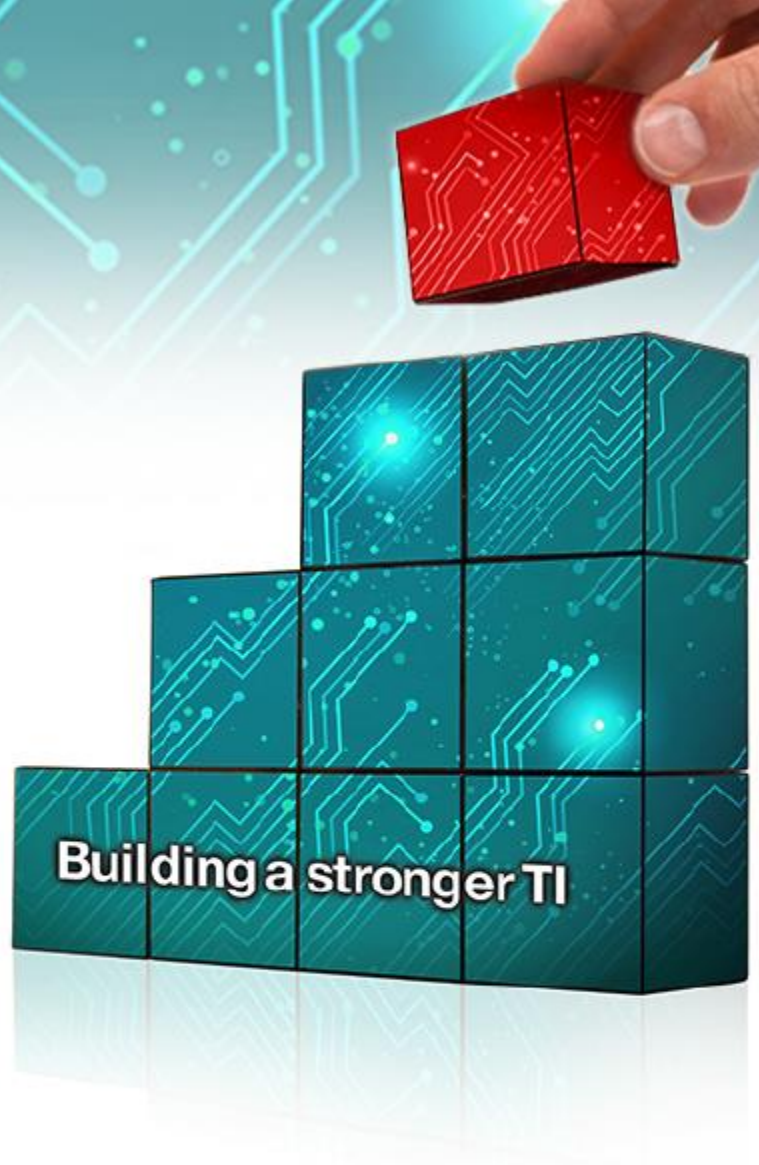
RF Sampling Clocking



Clocking for RF Sampling

- RF sampling requires high frequency clock source
- Jitter or Phase Noise performance of the clock is critical to maintain best performance
- High Frequency Clock in RF Sampling vs. High Frequency Synthesizer in super-heterodyne architecture
  - RF Sampling only needs one frequency clock. No tuning is required.
    - Narrow band VCO or VCXO is sufficient
      - ✓ Easier to achieve very good phase noise performance
    - No channel tuning required
      - ✓ Channel allocation is accomplished digitally
  - Pure sinusoid not absolutely needed; only concerned with transitions

Clock Jitter Impact in Data Converters

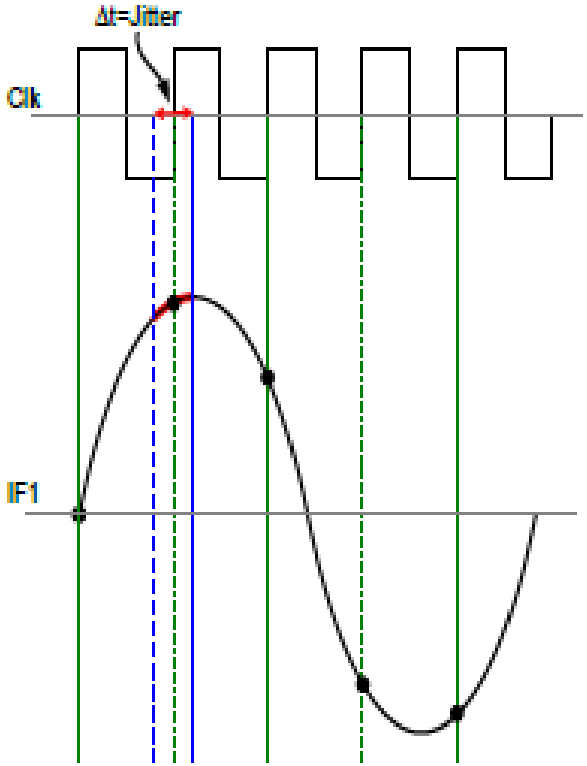
- Random variation of the clock position compared to its ideal position with respect to time
- As clock position varies, the position of the sampling point varies
- Sampling at imprecise locations yield SNR degradation
- Theoretical limit of SNR due to jitter:

$$SNR_j = -20 \cdot \log(2\pi f_{in} \cdot \tau_j)$$

where:

fin = input frequency

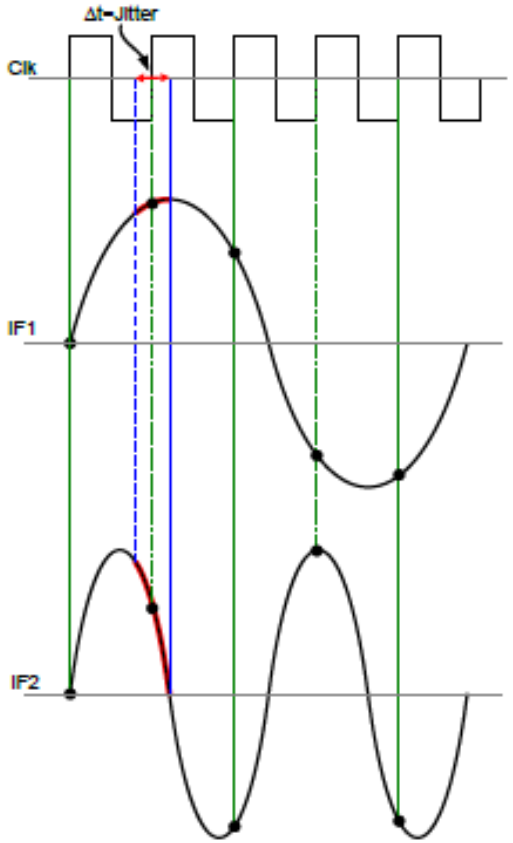
τj = clock jitter



Jitter Impact with respect to Frequency

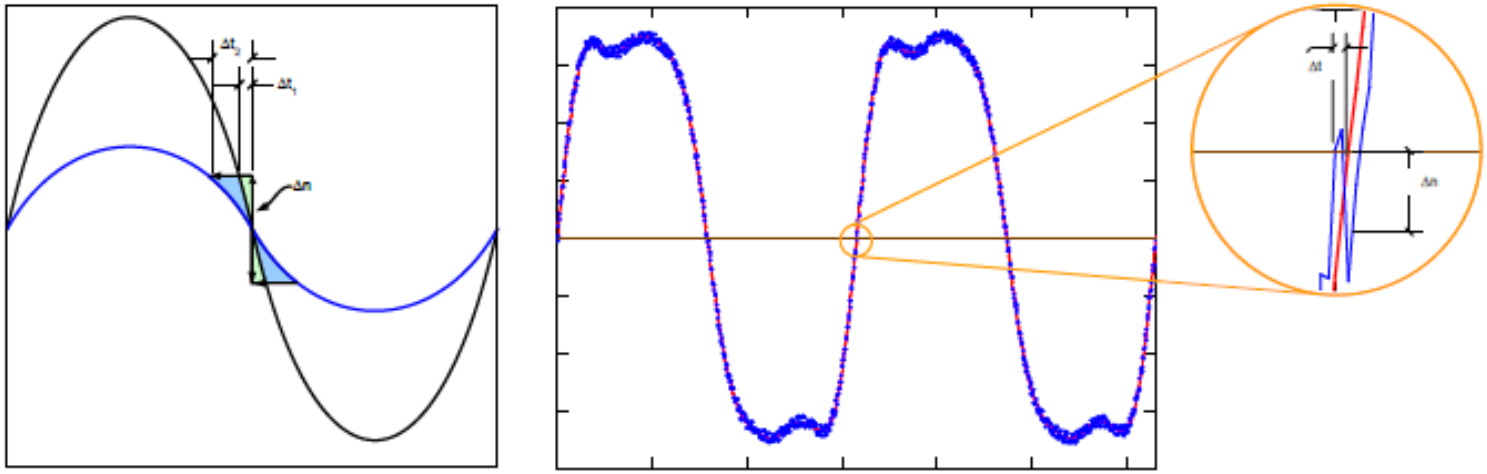
- SNR is independent of sampling rate
- SNR is dependent on input frequency
  - For a given amount of jitter, SNR degrades as input frequency increases
- Higher sampling rates indirectly lead to more stringent jitter requirements
  - High sampling rate device are not “more sensitive”; rather, high sampling rates allow higher input frequencies

$$SNR_j = -20 \cdot \log(2\pi f_{in} \cdot \tau_j)$$



Slew Rate and Jitter Performance

- Slower slew rate is more susceptible to variations in the zero crossing point due to noise
- BPF filters broadband noise but also removes harmonics
  - Square-wave-like clocks become sinusoid clocks
  - Sinusoid signals have lower slew rate
- Increase signal to large amplitude to minimize slew rate impact



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Thank You