Intel® Cyclone® 10 LP FPGA Webinar

Uniquest Train the Trainer

February 2018

Webinar OBJECTIVE

Learn about Intel® Cyclone® 10 LP FPGA – Intel's next generation low cost and low power FPGA

Get hands on experience with hardware and software required to build an FPGA and run an embedded processor system

Intel® Cyclone® 10 LP FPGA Webinar **Agenda**

Presentation

10 minutes

1. Intel Cyclone 10 LP FPGA product & target applications
2. Overview of Intel Cyclone 10 LP FPGA evaluation kits
3. Device, SW and evaluation kit rollout status

HANDS ON LAB

20 minutes

1. My first FPGA design using Nios® II – 20 min

Introduction to Intel® Cyclone ® 10 LP FPGA

Lower power

Improved number of I/O / watt

Up to 50% lower power

Lower cost

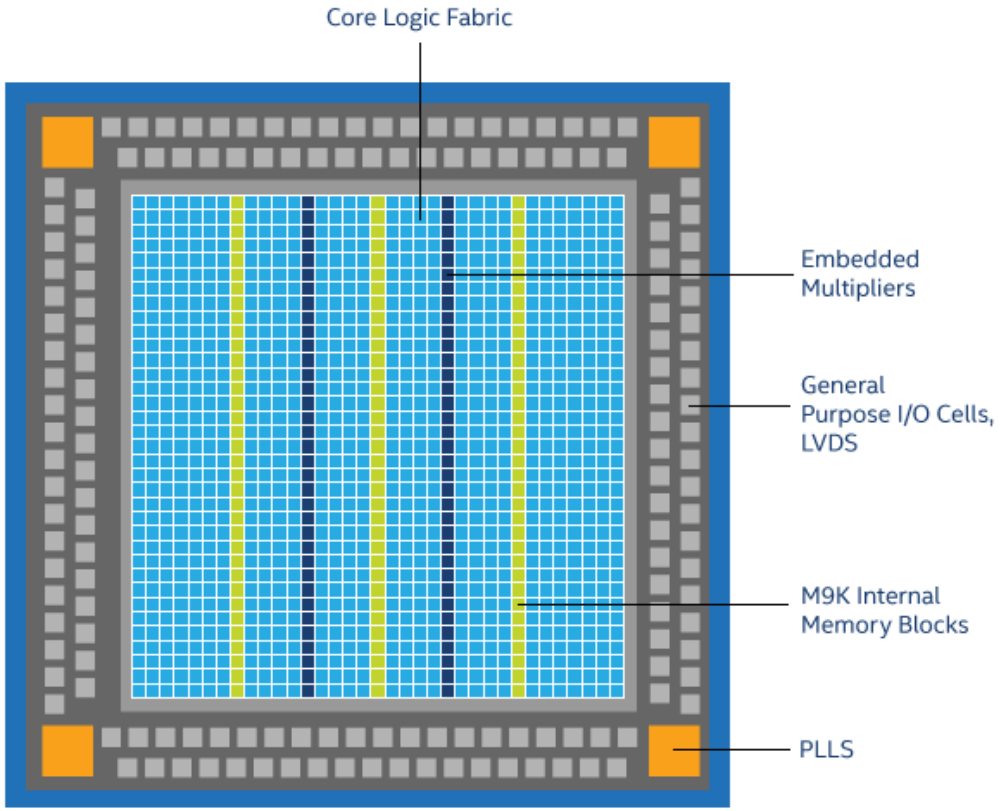
Simplified power distribution network

Saves board costs, board space, & design time

Half the Power at Half the Cost (1)

(1) As compared to previous generation Cyclone V family

Intel® Cyclone® 10 LP FPGA Device Features



- Built on a 60 nm TSMC process technology
- Supports highly integrated, low power and efficient Empirion PowerSoCs
- Only requires two core power supplies
- Supports flexible and integrated Nios® II processor
- Packages starting from 8x8 mm up to 29X29 mm
- Densities beginning from 6KLE up to 120 KLE

Industrial & Automotive qualifications
IEC 61508, AEC-Q100 Grade 2

Low cost and low risk proven technology

Typical Intel® Cyclone® 10 LP FPGA - **End Market and Applications**

End MARKETS

Industrial IoT Medical Test & Measurement Automotive

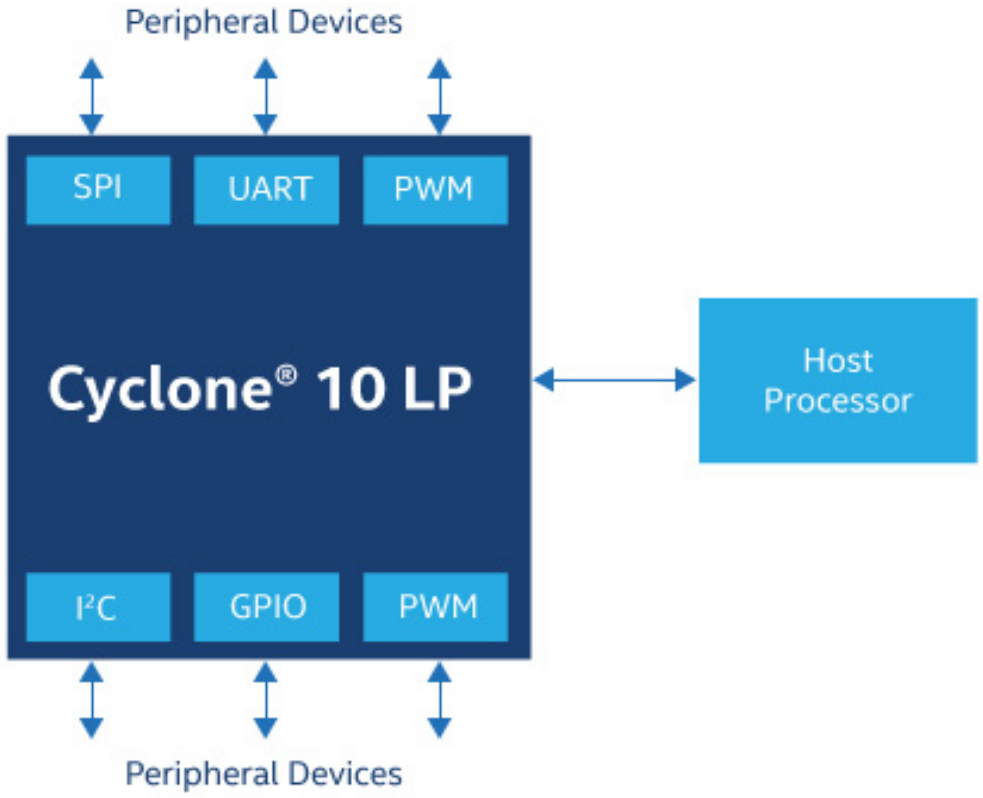
End APPLICATIONS

I/O Modules Interfacing Sensors Actuators Bridging Imaging

Intel® Cyclone® 10 LP FPGA : Control Application Examples

Market Trend: Abundance of evolving connectivity standards, impacts the scalability of:

- Static power
- System cost
- Sensor interfacing needs
- Voltage translation needs
- I/O Expansion
- System synchronization

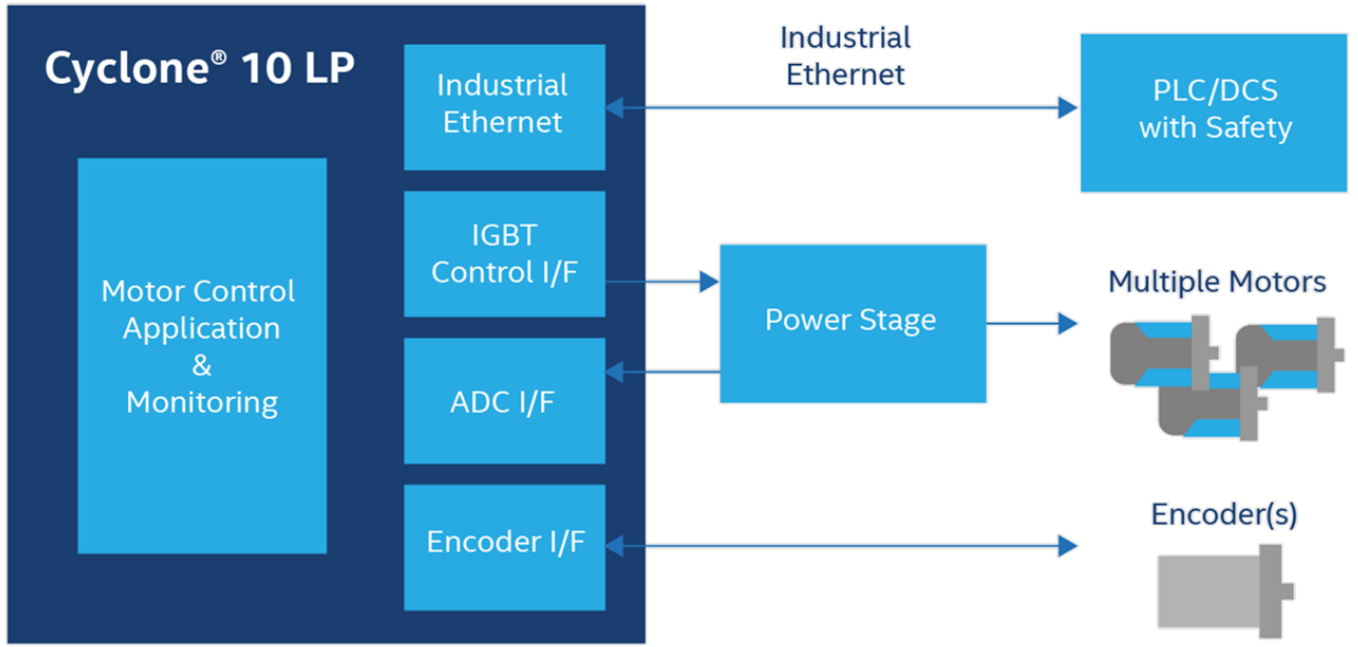


Enables a lower power, cost sensitive and flexible solution

Intel® Cyclone® 10 LP FPGA : Motor Control Examples

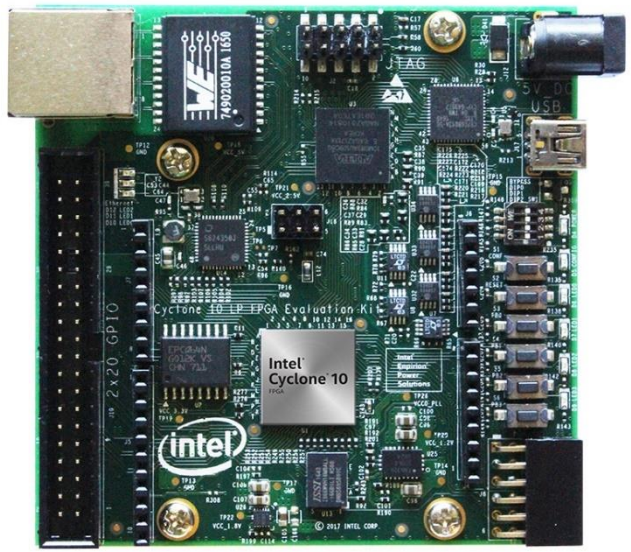
Market Trend: Need for greater integration and motor monitoring:

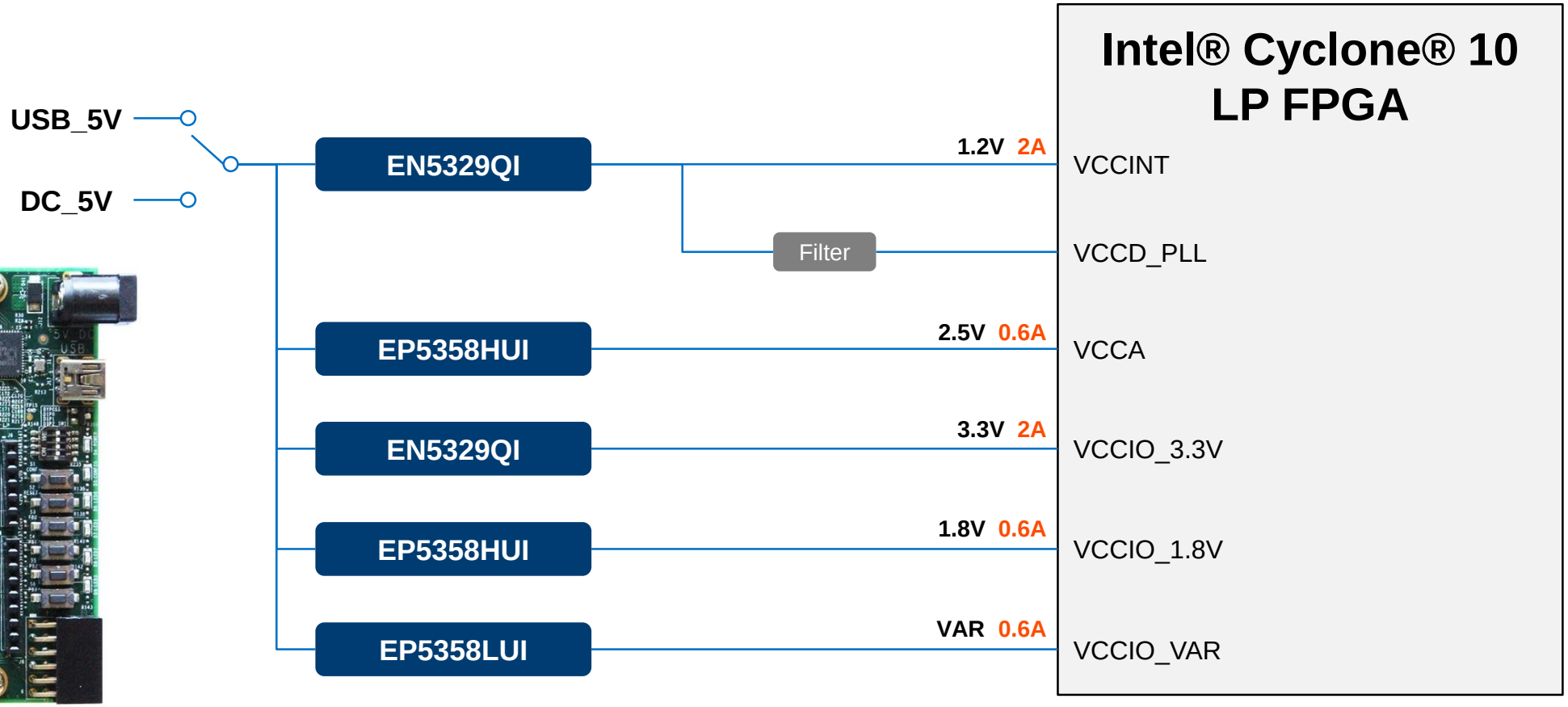
- Drive on a chip integration reduces system cost while increasing performance
- Scalable performance via more advanced control loops
- Functional safety growing in customer importance.



Intel Cyclone 10 FPGA reduces overall cost of ownership

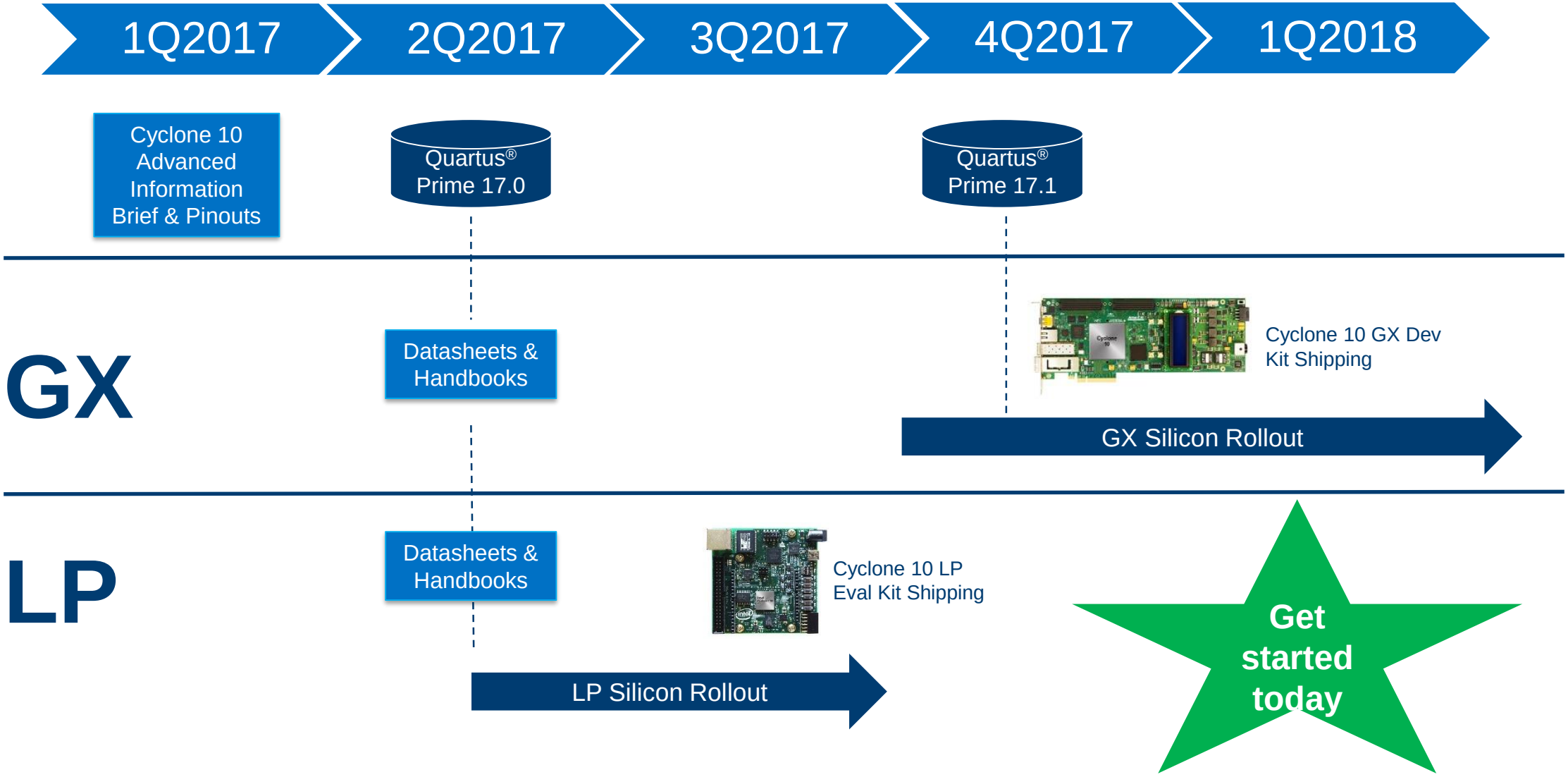
Intel® Cyclone® 10 LP FPGA Dev Kit - **100% Powered by Enpirion**





Power Tree for example reference only. Refer to FPGA "Pin Connection Guidelines" for exact sequencing requirements. Refer to FPGA datasheet for recommended operating conditions and voltage tolerances.

Intel® Cyclone® 10 FPGA Silicon / Software / Kit Rollout- **On Schedule**



Intel® Cyclone® 10 FPGA : Product Table

Product Line	10CL006	10CL010	10CL016	10CL025	10CL040	10CL055	10CL080	10CL120
Logic Elements (LE)	6,000	10,000	16,000	25,000	40,000	55,000	80,000	120,000
M9K Memory Blocks	30	46	56	66	126	260	305	432
Memory Block (Kb)	270	414	504	594	1,134	2,340	2,745	3,888
18x18 Multipliers	15	23	56	66	126	156	244	288
PLLs	2	2	4	4	4	4	4	4
LVDS Channels (0.83 Gbps)	65	65	137	124	124	132	178	230
Ball count, package size, ball pitch	Package Options (number of I/O available)							
M164 (8X8 mm), 0.5 mm		101	87					
U256 (14x14 mm), 0.8 mm	176	176	162	150				
U484 (19x19 mm), 0.8 mm			340		325	321	289	
E144 (22x22 mm), 0.5 mm	88	88	78	76				
F484 (23x23 mm), 1.0 mm			340		325	321	289	277
F780 (29x29 mm), 1.0 mm							423	525

Evaluation Kits

Hardware solutions and tools to enable technology evaluation and / or accelerate the customer design process

Intel® Cyclone® 10 FPGA – Board & Kit Introduction

- Cyclone 10 LP FPGA **Evaluation kit**
  - I/O feature rich kit targeted at technology evaluation
  - $99.95 price
  - EK-10C025U256
  - Shipping September 2017

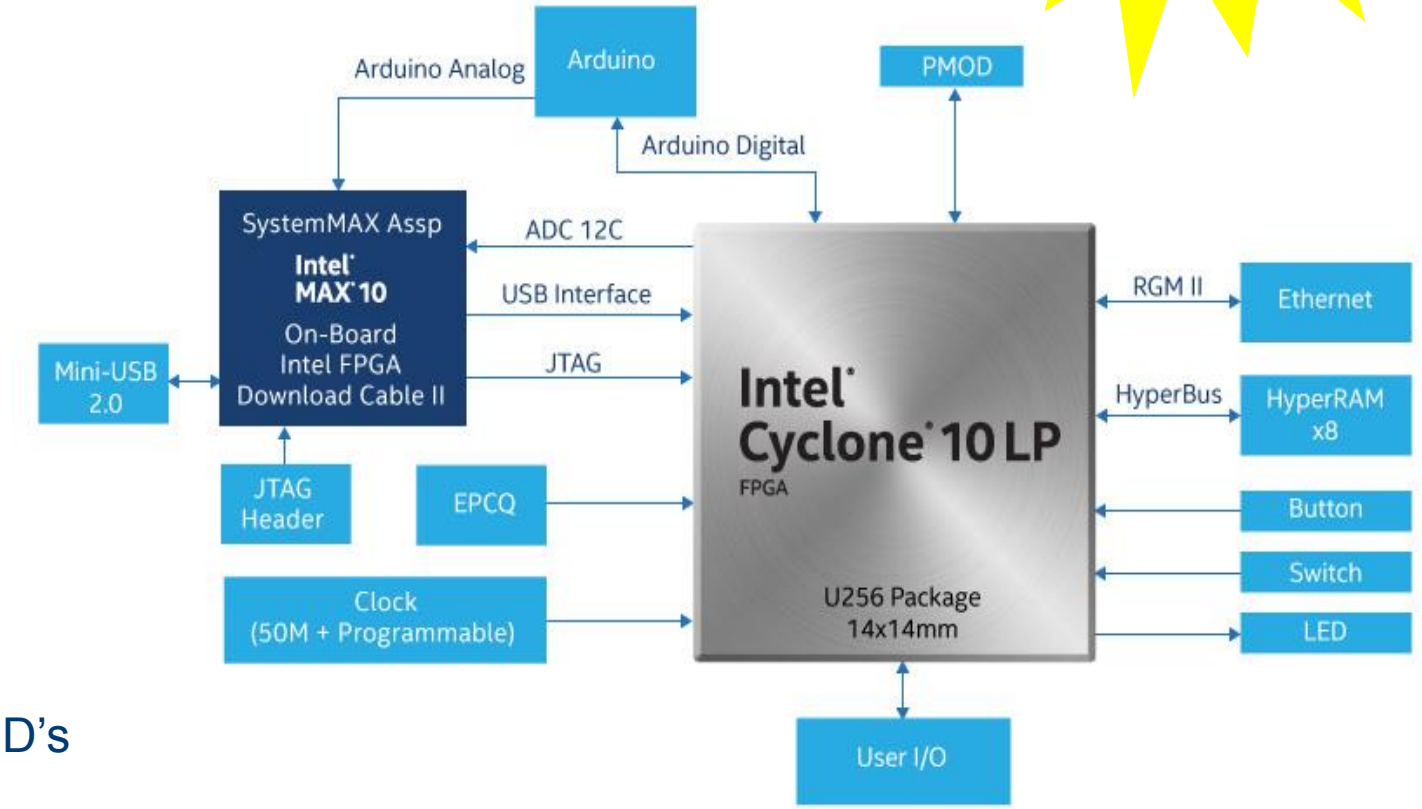
(1) Target Price
(2) Open for bookings October ‘17

Intel® Cyclone® 10 LP FPGA **Evaluation Kit** - $99.95

Shipping Now

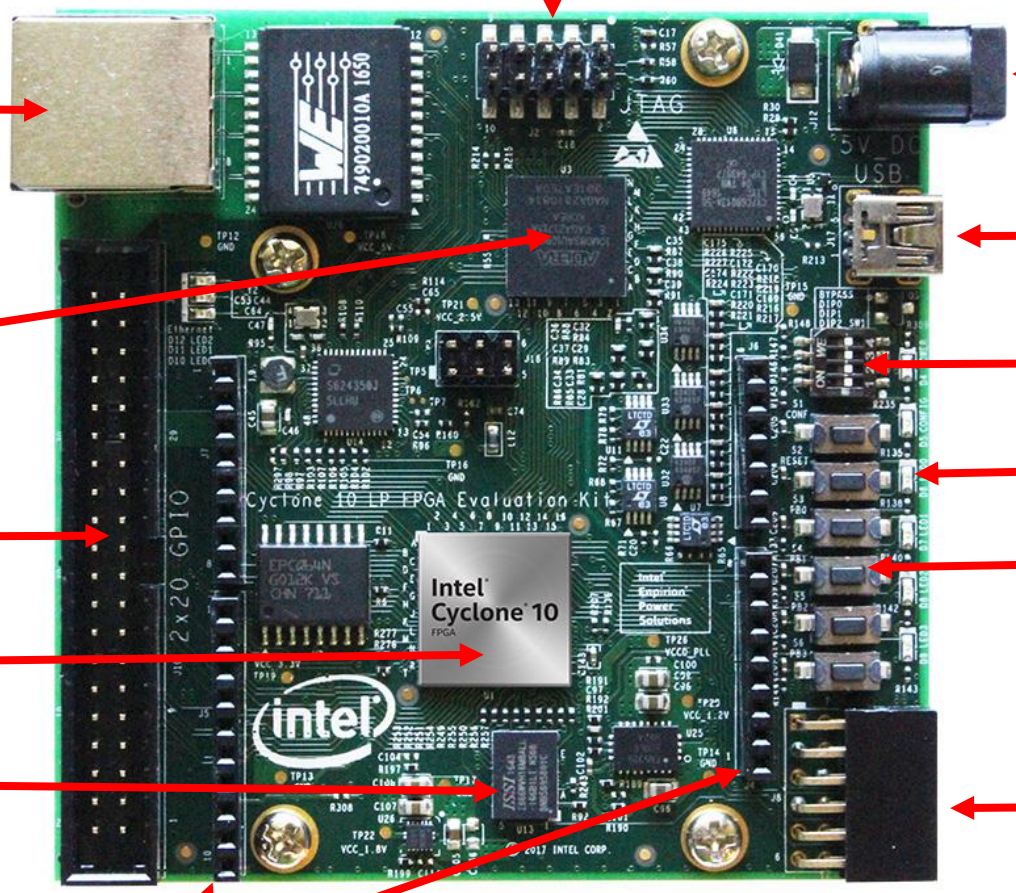
Features:

- Intel Cyclone 10 LP 25KLE
- Intel MAX 10 System Manager
  - Including USB Blaster II
- HyperRAM
- Ethernet 10/100/1000Mbps*
- Diligent PMOD connector
- Arduino Interface connector
- GPIO connector
- Push Buttons / DIP Switch's / Status LED’s



* Supported from Quartus Prime 17.1 onwards

Intel® Cyclone® 10 LP FPGA Evaluation Kit



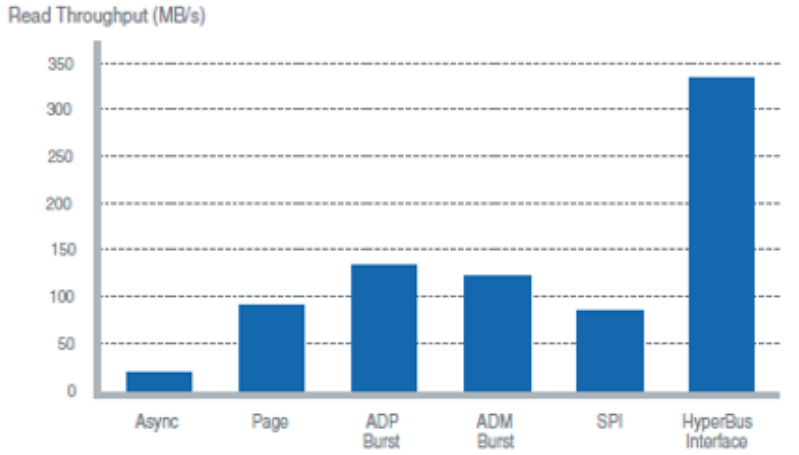
(1) Supported from Quartus 17.1 onwards

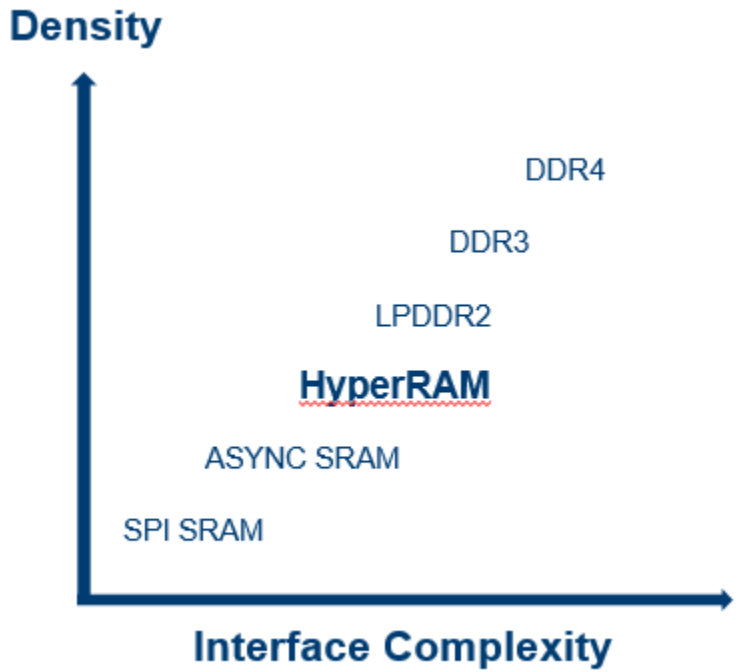
Use of Low-Pin-Count Memories

- When to use HyperRAM memories
  - Where this is no requirement for DDR3/4 widths /speed
  - Requires low access overhead
  - Small footprint

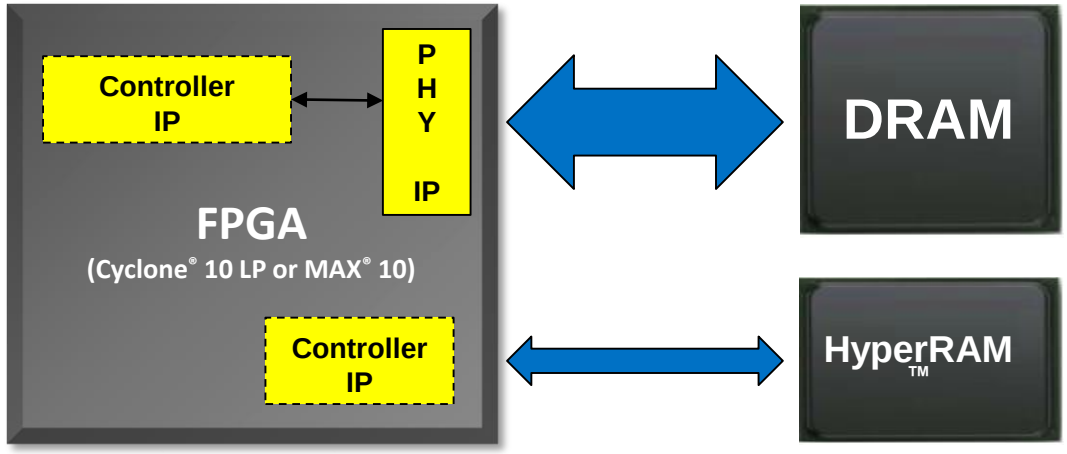
- Target Market examples
  - Automotive Clusters – user settings
  - Board Management – fault logs
  - Instrumentation – data storage
  - Embedded – application storage

- Ideal EMIF devices for Cyclone 10 & MAX 10 FPGA's





Advantages of HyperRAM™?

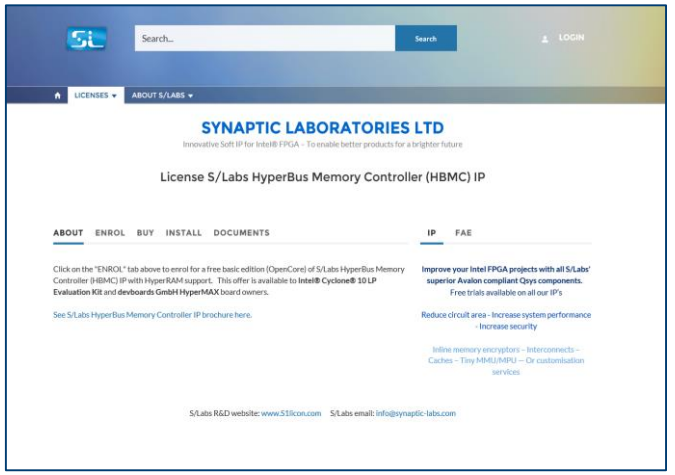


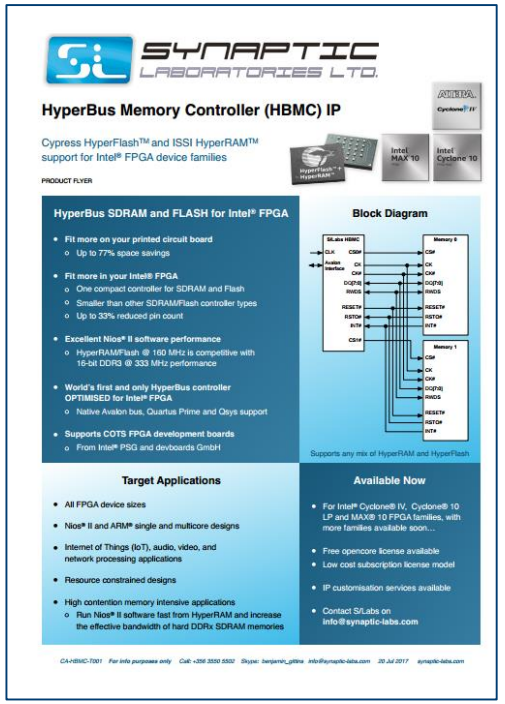
Item	HyperRAM(1)	DDR2	DDR3
# of pins	12 or 13	~50	~50
Controller IP size	400 LE's & 2x M9K's	6,000 LE's & 11x M9K's	6573 & 11x M9K's
Licensing/ cost	Synaptic Labs ($)	PSG p/n = IP-SDRAM/HPDDR2 ($) PSG Altmemphy	$0
Performance	150 MHz (C10-LP)	167 MHz (CIV)	300 MHz (MAX10)
Width	x8	x4, x8, x16	x8, x16, x24
Densities	64 Mb – 128 Mb 256Mb (2017)	512 Mb – 4 Gb	1 Gb – 16 Gb

(1) Synaptic L:abs soft IP core

HyperBUS Memory Controller IP – Synaptic Labs

- Supports HyperRAM & HyperFlash memories
  - Low pin count – 13
  - Low logic utilization
  - Small packages – 8x6mm
  - Dual function – Flash & Ram in same multi chip package variant available
- IP Core available as either Basic or Full versions
  - OpenCore plus free evaluation licenses
- Licenses available direct from Synaptic Labs
  - Request a license here





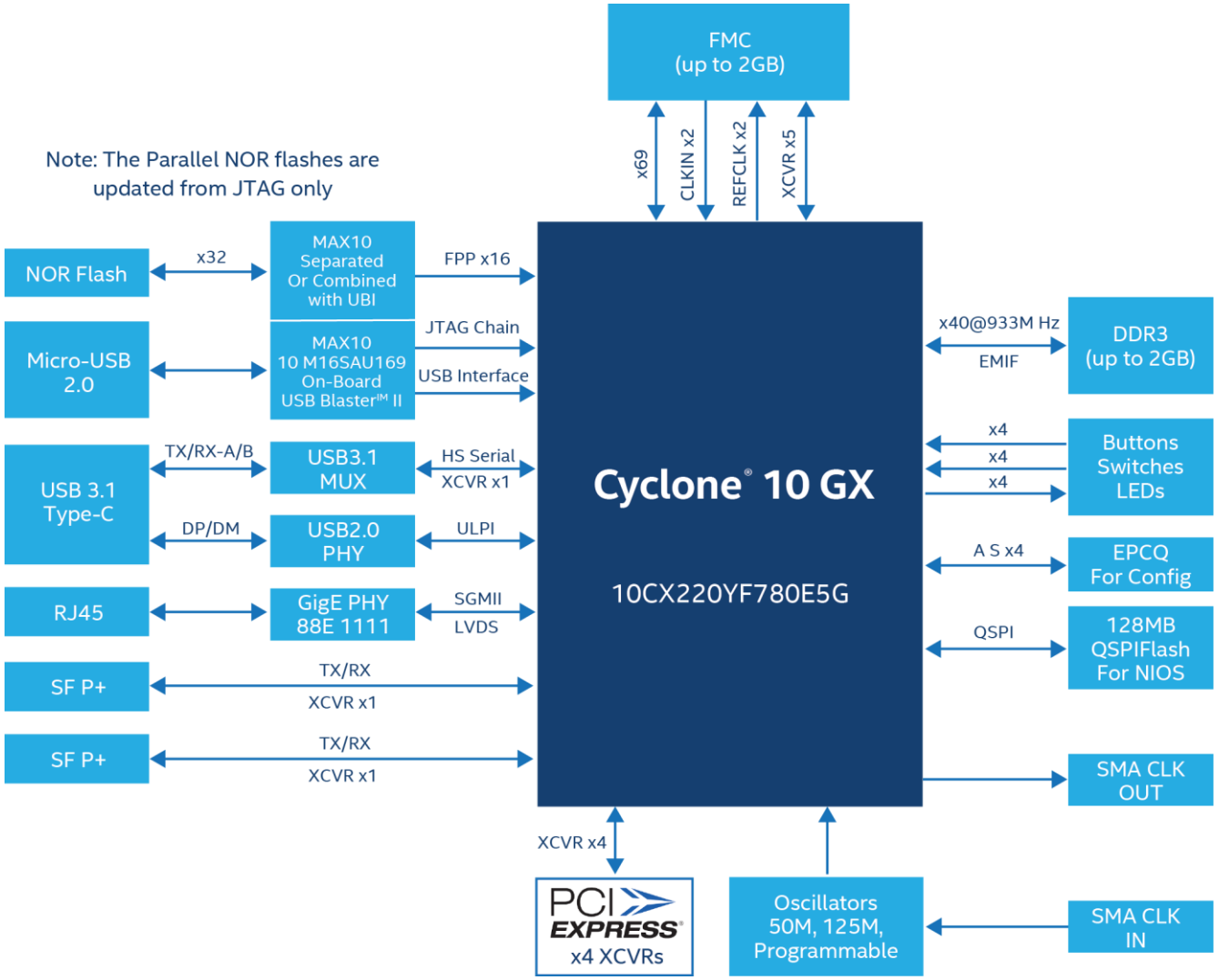
Feature	Basic	Full
Clock Speed (DDR)	100MHz	150MHz
Device(s)	1x HyperRAM	2x HyperRAM or HyperFLASH
LE Count	1000	400
M9K RAM Blks	0	2

Intel® Cyclone® 10 GX FPGA **Development Board**

Features:

- 10CX220YF780E5G + Enpirion power
- MAX 10: USB blaster & BMC
- Memory
  - DDR3: 2 GB x40 @ 933 MHz
- Flash
  - NOR Flash: 128 MB
- Interfaces
  - FMC Connector
  - PCIe Gen2 x4
  - USB 3.1 Gen2
  - Ethernet: 10G x2

Availability : December 2017



New Users Existing Users

Hands on lab Objective

Demonstrate “Ease of Use” of FPGA by building and running an embedded system

Demonstrate Intel® Cyclone® 10 FPGA device and board features

Nios® II Processor – An overview

https://www.altera.com/products/processors/overview.html

Add one or more embedded processors to FPGA design

- Royalty free, 32-bit RISC architecture, 190 DMIPs @ 165 MHz(1), soft IP core, no external RAM or storage needed

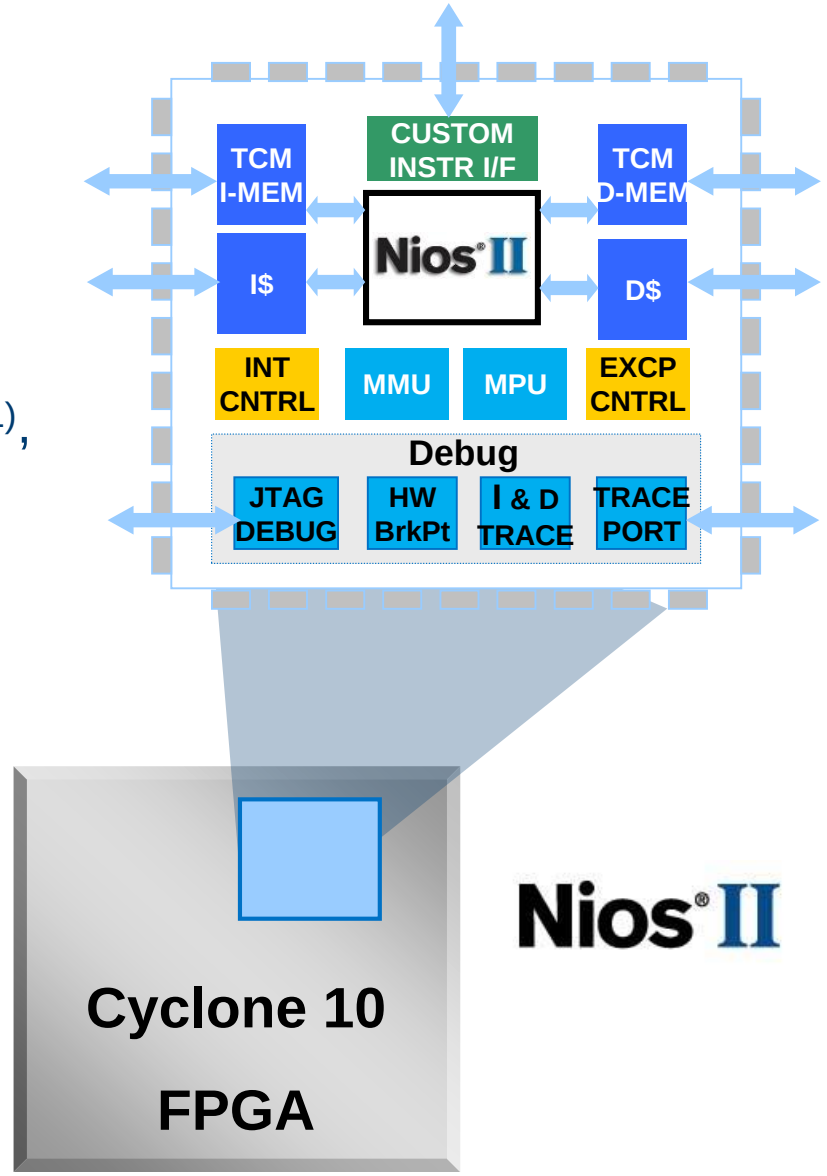
User-customizable processor

- Add or remove peripherals, as needed

Support for real-time applications

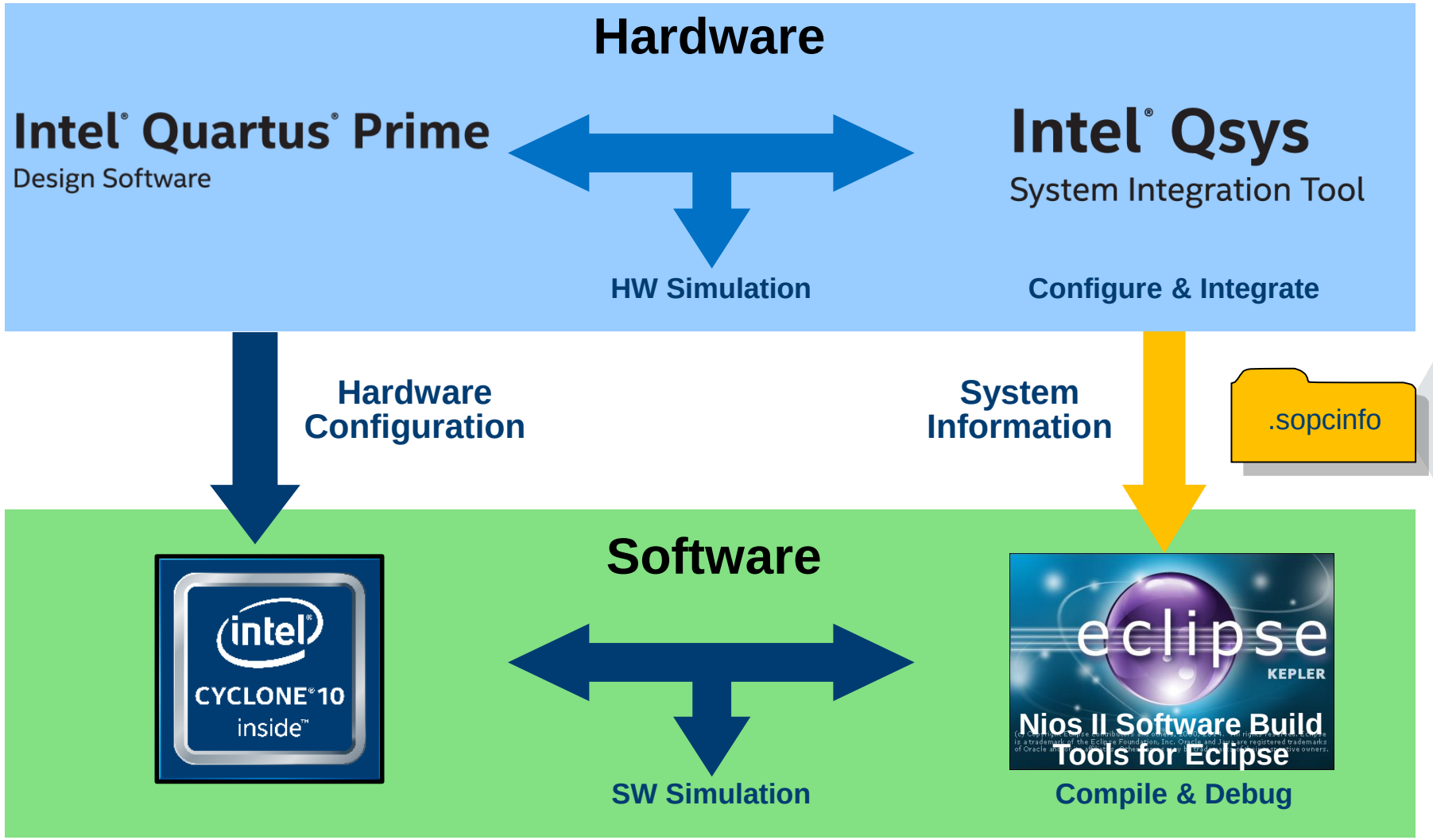
- Configuration in under 10 ms
- Avionic, automotive & industrial compliant versions

Extensive software ecosystem & support



(1) Dhrystones 2.1 benchmark (Intel Estimate)

Flexible and integrated Nios® II development flow



Nios II SW enables ultimate system design flexibility and productivity

My first FPGA design using Nios® II processor

Foundation Exercise

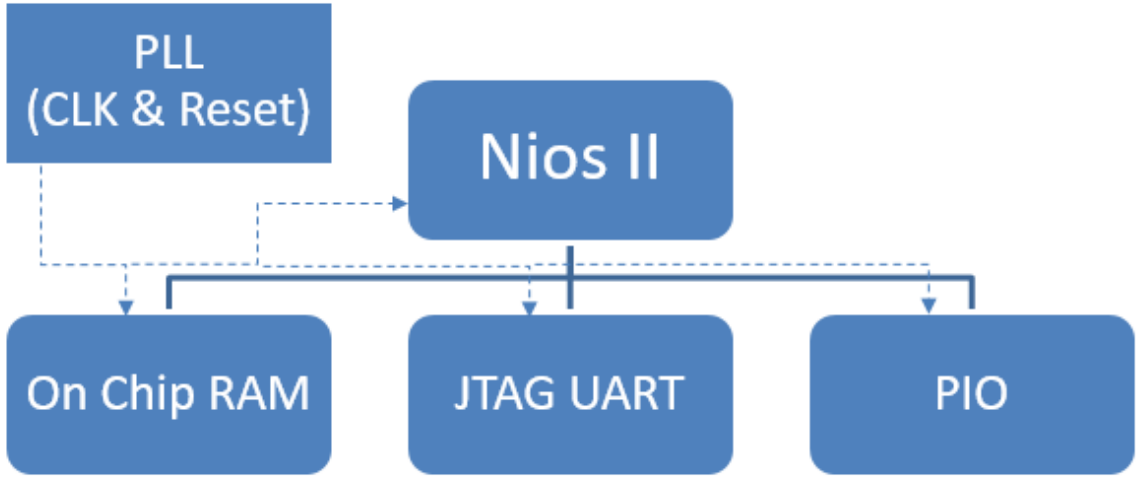
New User

Objective :

1. Demonstrate “ease of use” to a new user.
2. Build a Nios II processor based embedded hardware system, download it to the development board and run “Hello world” software program in ‘C’.

Exercises :

1. Create basic Nios II Processor System using Qsys
2. Run ‘Hello World’ on the Nios II Processor
3. Control LEDs from software



SW/Tools requirements:

1. Quartus® Prime Lite software v17.0 (or later)
2. Design files for exercises

For more information go to altera.com

- www.altera.com/cyclone10
- www.altera.com/nios
- www.altera.com/qsys
- www.altera.com/quartus
- www.altera.com/documentation

- … and more…

Online Training

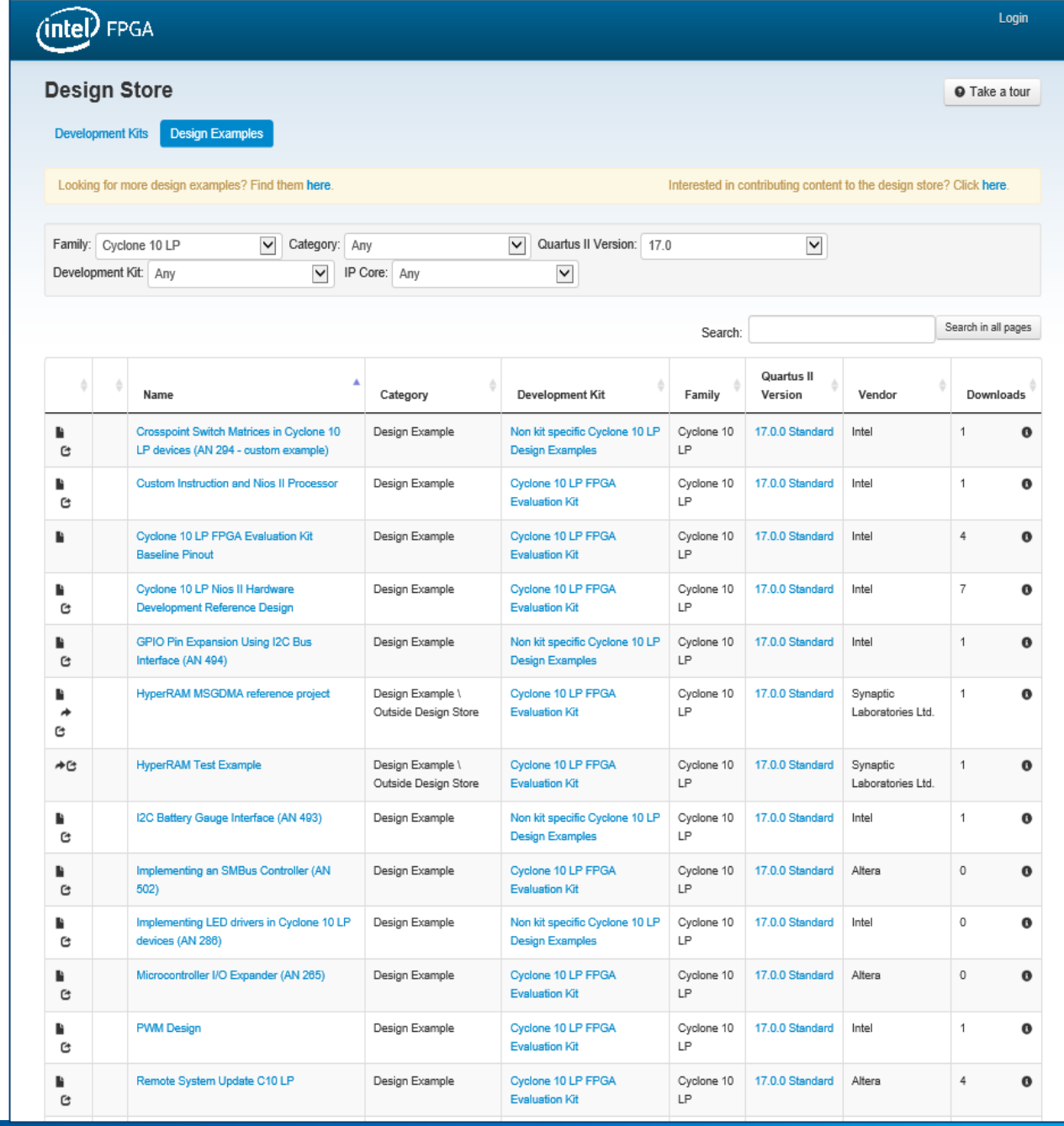
- www.altera.com/training
- Go to catalog and Filter on subject of interest, e.g.

Nios II Online Courses	Qsys II Online Courses
Developing Software for the Nios II Processor: HAL Primer (OEMB1150) 20 Minutes	Advanced System Design Using Qsys: Component & System Simulation (OAQSYSSIM) *28 Minutes*
Developing Software for the Nios II Processor: Nios II Software Build Tools for Eclipse (OEMB1128) 14 Minutes	Advanced System Design Using Qsys: Qsys System Optimization (OAQSYSOPT) *32 Minutes*
Nios II Software Build Tools for Eclipse and BSP Editor (Quartus II Software 10.0 Update) (ONSW1128) 26 Minutes	Advanced System Design Using Qsys: System Verification with System Console (OAQSYSSYSCON) *25 Minutes*
Nios II Software Tools and Design Flow (ONIITOOLSDESIGN) 22 Minutes	Advanced System Design Using Qsys: Utilizing Hierarchy in Qsys Designs (OAQSYSHIER) *22 Minutes*
Using the MAX 10 User Flash Memory with the Nios II Processor (OMAXNIOS) 24 Minutes	Creating a System Design with Qsys (OQSYSCREATE) *37 Minutes*
Using the Nios II Processor: Custom Components and Instructions (ONIICUS) 11 Minutes	Custom IP Development Using Avalon and AXI Interfaces (OQSYS3000) *113 Minutes*
Using the Nios II Processor: Hardware Development (ONIIHW) 27 Minutes	Introduction to Qsys (OQSYS1000) *26 Minutes*
Using the Nios II Processor: Software Development (ONIISW) 10 Minutes	System Design with Qsys Pro (OQSYSPRO) *42 Minutes*

Intel® Cyclone® 10 - Design Examples – Available Today

Design Store

- Cyclone 10 LP FPGA Designs
  - Evaluation Kit targeted – 10 Designs
  - Non targeted LP – 4 Designs
  - More designs added every day ……



Name	Category	Development Kit	Family	Quartus II Version	Vendor	Downloads
Crosspoint Switch Matrices in Cyclone 10 LP devices (AN 294 - custom example)	Design Example	Non kit specific Cyclone 10 LP Design Examples	Cyclone 10 LP	17.0.0 Standard	Intel	1
Custom Instruction and Nios II Processor	Design Example	Cyclone 10 LP FPGA Evaluation Kit	Cyclone 10 LP	17.0.0 Standard	Intel	1
Cyclone 10 LP FPGA Evaluation Kit Baseline Pinout	Design Example	Cyclone 10 LP FPGA Evaluation Kit	Cyclone 10 LP	17.0.0 Standard	Intel	4
Cyclone 10 LP Nios II Hardware Development Reference Design	Design Example	Cyclone 10 LP FPGA Evaluation Kit	Cyclone 10 LP	17.0.0 Standard	Intel	7
GPIO Pin Expansion Using I2C Bus Interface (AN 494)	Design Example	Non kit specific Cyclone 10 LP Design Examples	Cyclone 10 LP	17.0.0 Standard	Intel	1
HyperRAM MSGDMA reference project	Design Example \ Outside Design Store	Cyclone 10 LP FPGA Evaluation Kit	Cyclone 10 LP	17.0.0 Standard	Synaptic Laboratories Ltd.	1
HyperRAM Test Example	Design Example \ Outside Design Store	Cyclone 10 LP FPGA Evaluation Kit	Cyclone 10 LP	17.0.0 Standard	Synaptic Laboratories Ltd.	1
I2C Battery Gauge Interface (AN 493)	Design Example	Non kit specific Cyclone 10 LP Design Examples	Cyclone 10 LP	17.0.0 Standard	Intel	1
Implementing an SMBus Controller (AN 502)	Design Example	Cyclone 10 LP FPGA Evaluation Kit	Cyclone 10 LP	17.0.0 Standard	Altera	0
Implementing LED drivers in Cyclone 10 LP devices (AN 288)	Design Example	Non kit specific Cyclone 10 LP Design Examples	Cyclone 10 LP	17.0.0 Standard	Intel	0
Microcontroller I/O Expander (AN 265)	Design Example	Cyclone 10 LP FPGA Evaluation Kit	Cyclone 10 LP	17.0.0 Standard	Altera	0
PWM Design	Design Example	Cyclone 10 LP FPGA Evaluation Kit	Cyclone 10 LP	17.0.0 Standard	Intel	1
Remote System Update C10 LP	Design Example	Cyclone 10 LP FPGA Evaluation Kit	Cyclone 10 LP	17.0.0 Standard	Altera	4

Summary

Intel is shipping Intel® Cyclone® 10 LP FPGA evaluation kits - Enabling the next generation of low cost and low power FPGA applications

Intel® Cyclone® 10 FPGA “Ease of programmability” enables new FPGA users and gives time to market advantage to all FPGA users

You can get started today!


intel
experience
what's inside™

BACKUP

Intel® FPGA : application specific performance

The right performance and features for the right application

Management, Sensors and edge devices

- Board Management
- Edge Compute
- I/O Expansion
- Automobile sensors, traffic sensors

Vision systems, and purpose-built, application-specific hardware

- Machine Vision
- Embedded Vision
- Robotics
- Infotainment, ADAS, telematics

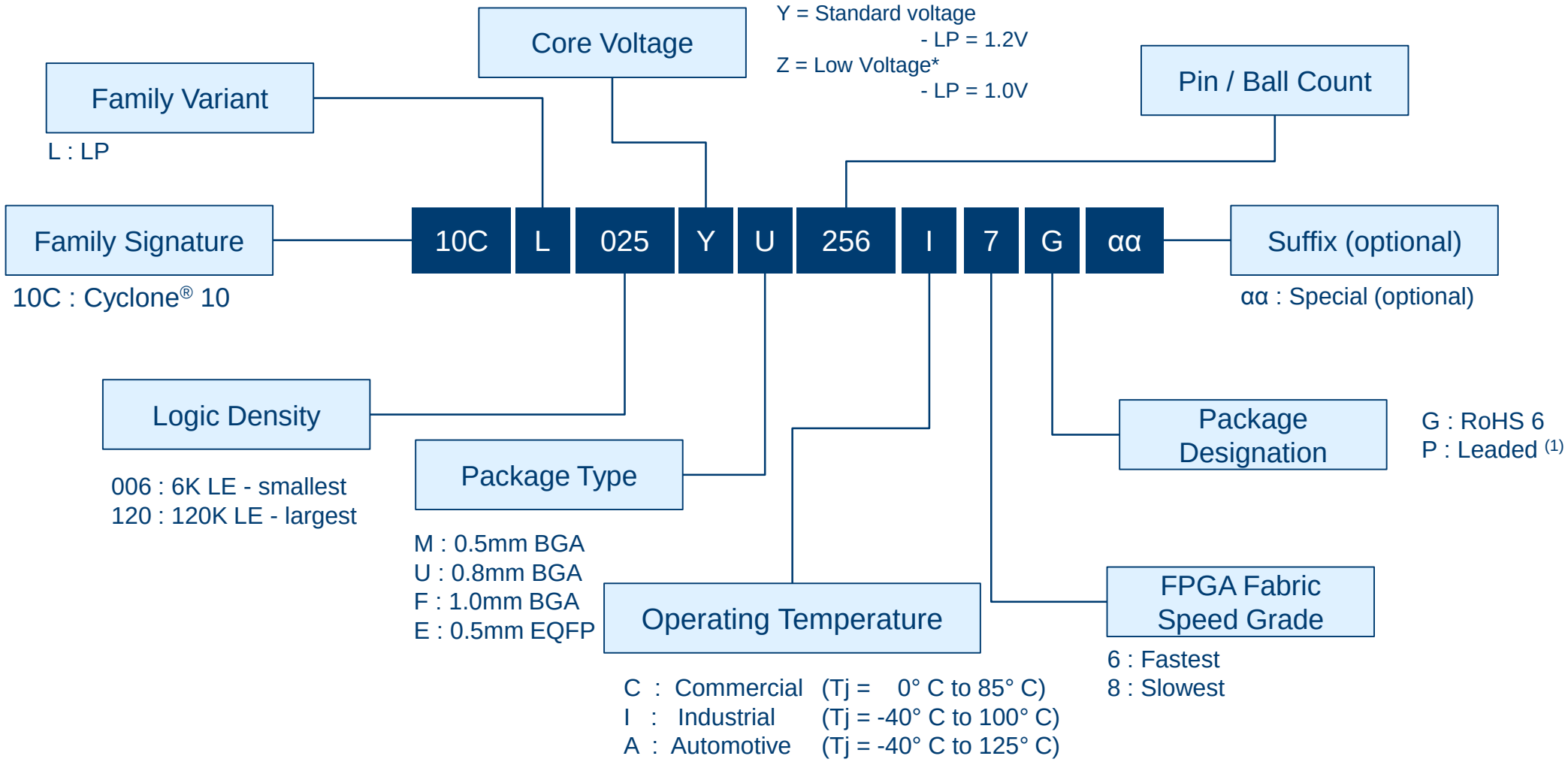
Scalable and efficient computing performance

- Datacenter
- Networking
- Military / Defense
- ADAS

Cloud, datacenter, and HPC

- Datacenter / CSP Acceleration
- 5G Wireless Infrastructure
- Network Communications
- Military / Defense

Cyclone® 10 LP FPGA : Part Number Decoder

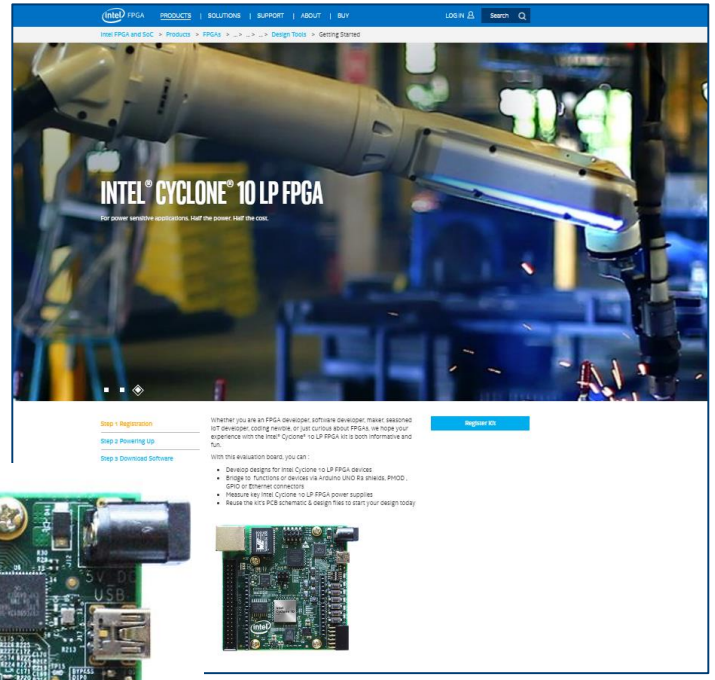


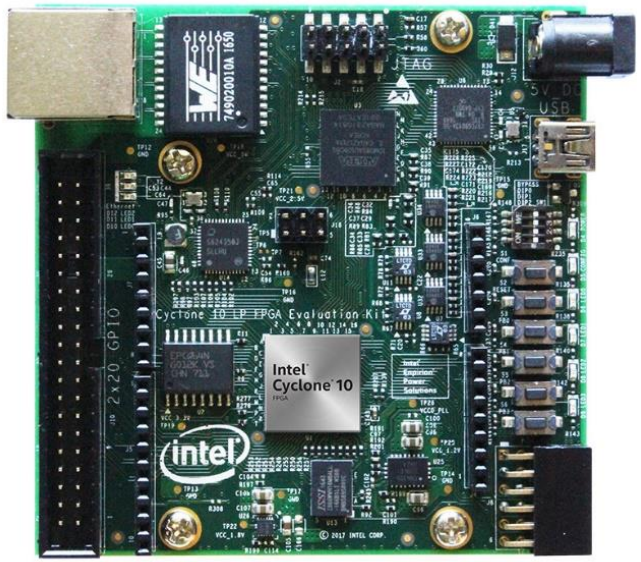
(1) Contact factory

So what's in the Kit ?

- Plastic clam shell packing
  - Evaluation Board
  - USB Cable
  - Card insert with quick start instructions

- Web Based Quick Start Web page
  - altera.com\lp





Other low cost kits…

Intel® Max® 10 FPGA Evaluation Kit -08 - $49.95

Intel® Max® 10 FPGA Evaluation Kit – 50 - $125

Intel® Max® 10 FPGA Evaluation Kit - $199.95

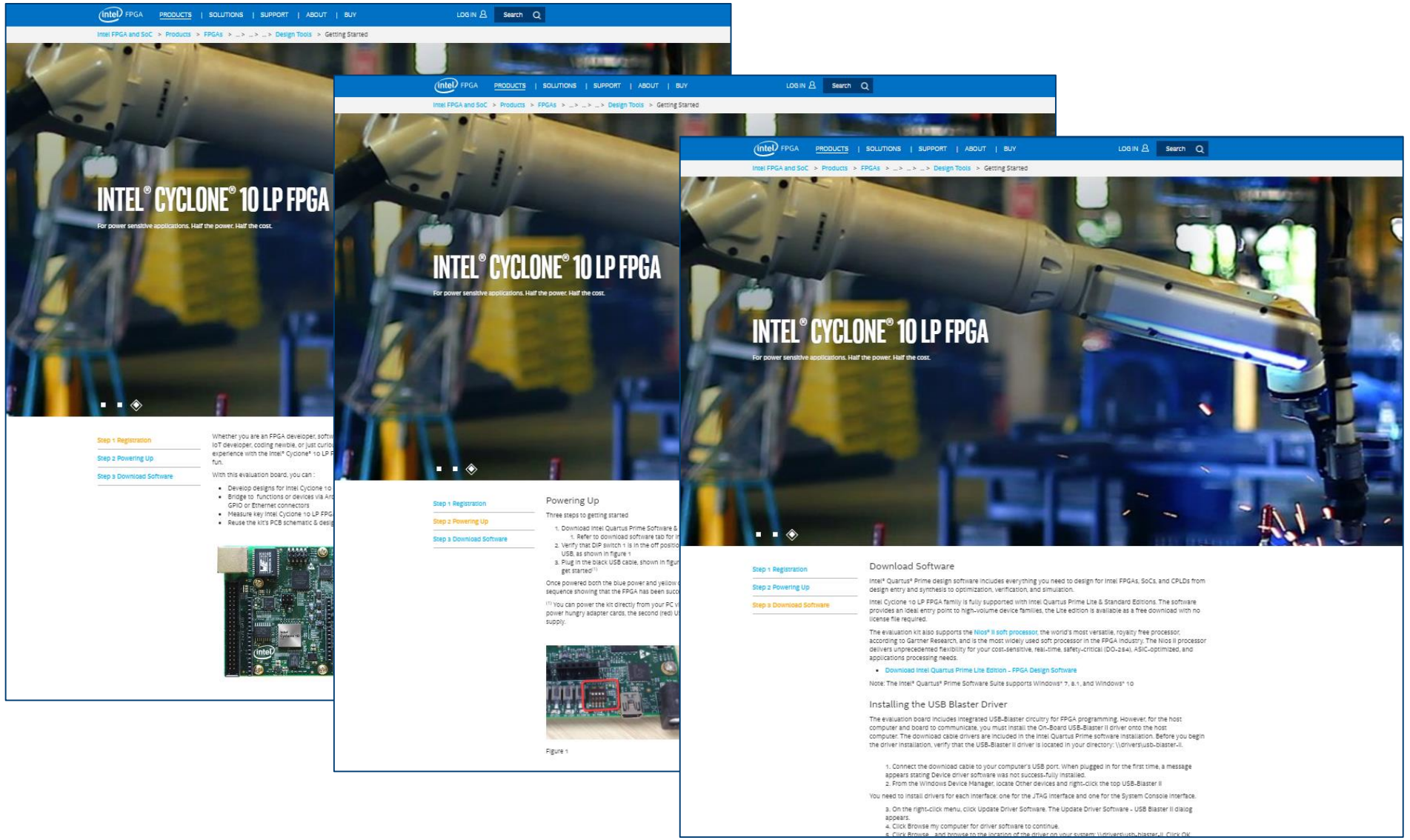
Arrow BeMicro MAX 10 Evaluation Kit - $30

Arrow DECA MAX 10 Evaluation Kit - $65

Arrow MAX1000 Evaluation Kit - $29

Take advantage - Get started today with one of the many low cost development kits!

Intel® Cyclone® 10 LP FPGA Evaluation Kit – On Line Getting Started



HyperRAM IP and Low Power Measurement

Foundation Exercise

New Users Existing Users

Objective :

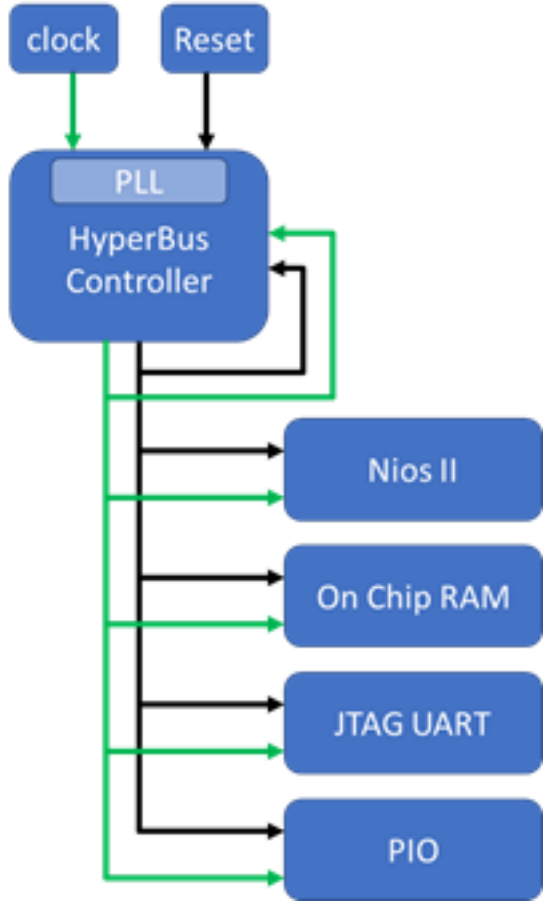
1. Demonstrate product “features” to new and existing users.
2. Become familiar with Qsys, Nios SBT and the Nios II HAL.

Exercises :

1. Build a system with the Synaptic Labs Hyperbus controller
2. Test the HyperRAM and accessing peripherals from software
3. Measure the board power consumption using the MAX10 ADCs

SW/Tools requirements:

1. Quartus® Prime Lite software v17.0 (or later)
2. Design files for exercises



More how to videos to get started today….

Engineer-to-Engineer Videos



https://www.altera.com/support/videos/how-to-videos.html

https://www.altera.com/products/fpga/max-series/max-10/support.html

How-to Videos

- Intel® MAX® 10 Overview
- Benefits of Dual Configuration Flash FPGAs
- MAX 10 Configuration
- MAX 10 Analog Block
- How to Create an ADC Design Using Qsys
- How to Create Simultaneous ADC Sampling - Part 1
- How to Create Simultaneous ADC Sampling - Part 2
- How to export MAX 10 ADC conversion data to the core for post-processing
- How to Configure User Flash Memory
- How to Boot Nios® II - Part 1
- How to Boot Nios II - Part 2
- How to Implement Remote System Update Part 1
- How to Implement Remote System Update Part 2
- How to Implement Remote System Update Part 3
- Board Management Bus Controller - Part 1
- Board Management Bus Controller - Part 2
- How to Create Your First LED Blinking Design - Part 1
- How to Create Your First LED Blinking Design - Part 2
- How to Create Your First LED Blinking Design - Part 3
- GPIO
- SEU and Security
- PLLs and Clocking
- Generation of ISC file for IEEE1532 Programming
- How to use the Internal Oscillator
- External Memory Interface Design Guideline
- External Memory Interface Implementation & debug - Part 1
- External Memory Interface Implementation & debug - Part 2
- Ethernet Ping Test Using Telnet from PC to MAX10 Development Kit - **NEW**