정확한 S-parameter 측정과 PCB Material 특성 추출

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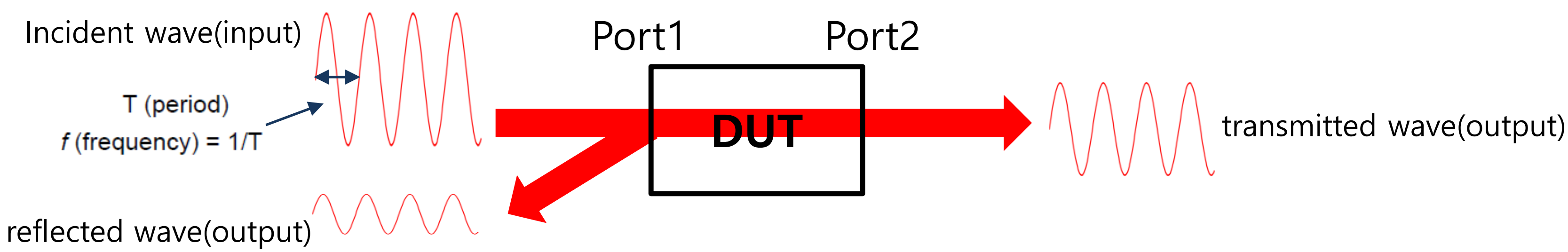
내 용

1. S-parameter란 무엇이고, 신호전송에 어떤 영향을 주는가?
2. S-parameter에서 Causality error란 무엇이고 왜 발생하는가?
3. Causality error가 발생하지 않는 Fixture De-embedding 방식
4. In-Situ De-embedding (ISD) tool 과 일반 방식의 비교 사례
5. PCB의 Material Property (Dk, DF, Roughness)가 S-parameter에 주는 영향
6. MPX(Material Property Extractor)를 이용한 PCB 시뮬레이션과 실제 측정 비교 사례
7. 최대의 성능을 확보하는 PCB와 RF 커넥터 연결 디자인 방법

S-parameter란 무엇인가?

S-parameter(Scattering Parameter): 주기(주파수)가 다양한 사인파를 어떤 구조체(DUT)에 입력(input)하여 통과된(transmitted) 파형과 반사된(reflected) 파형을 "주파수 도메인"에서 최초 입력파형(Incident wave)과 비교해 표현한 것.



✓Incident wave scatter back into the source, reflected wave: **S11 or Return Loss**

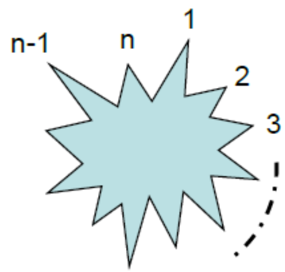
✓Incident wave scatter through the device, transmitted wave: **S21 or Insertion Loss**

$$\mathrm{mag}(S) = \frac{\textbf{amplitude of output sine wave}}{\textbf{amplitude of input sine wave}}$$

$S_{dB} = 20 \times \log_{10}(\mathrm{mag}(S))$ **Phase(S)= Phase(output sine wave) – Phase(input sine wave)**

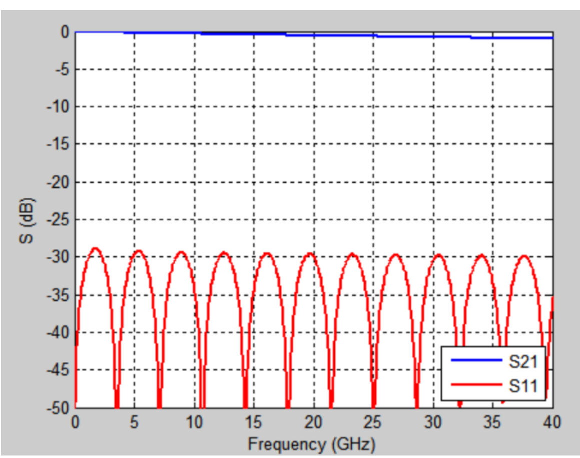
S-parameter란 무엇인가?

- For an n-port (or I/O) device, S parameter is an n x n matrix:



$$[S_{ij}]_{n\times n} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & \dots & S_{1n} \\ S_{21} & S_{22} & S_{23} & \dots & S_{2n} \\ \vdots & \vdots & \vdots & & \vdots \\ S_{n1} & S_{n2} & S_{n3} & \dots & S_{nn} \end{bmatrix}$$

- S_{ij} is called the S parameter from Port j to Port i.
- S_{ij} has a unique property that its magnitude is less than or equal to 1 (or, 0 dB) for a passive device.

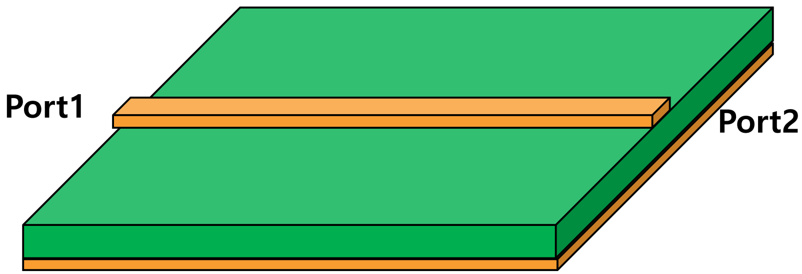


$$|S_{ij}| \le 1$$

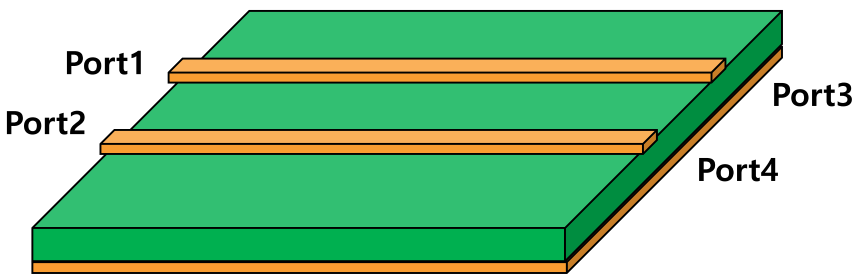
$$S_{ij}(dB) = 20 \times \log_{10}|S_{ij}| \le 0 \ \ dB$$

S-parameters of Single & Differential T.line

Single-end Line



Differential Line



2Port S-parameters

S11 S12
S21 S22

➡ Touchstone file: .S2P

4Port S-parameters

S11 S12 S13 S14
S21 S22 S23 S24
S31 S32 S33 S34
S41 S42 S43 S44

➡ Touchstone file: .S4P

4Port Mixed-Mode S-parameters

			Stimulus			
			Differential		Common Mode	
			Port 1	Port 2	Port 1	Port 2
Response	Differential	Port 1	SDD11	SDD12	SDC11	SDC12
		Port 2	SDD21	SDD22	SDC21	SDC22
	Common Mode	Port 1	SCD11	SCD12	SCC11	SCC12
		Port 2	SCD21	SCD22	SCC21	SCC22

Touchstone (.sNp) file

- S parameter at each frequency is expressed in Touchstone file format.

in GHz

S param

in dB and phase angle

Reference impedance

```
! Total number of ports = 4
! Total number of frequency points = 800
# GHZ  S  DB  R  50
0.025  -36.59296  48.77486  -41.40676  79.91354  -0.08648679  -6.544144  -49.50045  -105.618
       -41.39364  79.94686  -36.35592  51.52433  -49.4886  -105.5124  -0.09038406  -6.527076
       -0.08421237  -6.537903  -49.44814  -105.644  -36.0317  49.60022  -41.37105  79.91856
       -49.44393  -105.8186  -0.09834136  -6.542909  -41.36758  79.9318  -36.05645  48.98348
0.05  -32.22576  48.03161  -35.59394  74.15976  -0.1277169  -12.82876  -43.90183  -112.0995
       -35.58736  74.16304  -32.12694  50.92389  -43.90926  -112.0764  -0.132402  -12.7985
       -0.1242117  -12.82302  -43.89  -112.0248  -32.10987  50.3115  -35.56998  74.078
       -43.88424  -112.0517  -0.1381616  -12.80199  -35.56758  74.06782  -31.94136  50.49276
0.075  -29.88861  42.02766  -32.19713  68.06704  -0.1589249  -19.05252  -40.67476  -118.8188
       -32.19116  68.0941  -29.7086  45.41557  -40.63857  -118.837  -0.1635606  -19.01593
       -0.1603356  -19.0376  -40.63557  -118.8543  -29.89064  47.63852  -32.16917  67.94677
       -40.65711  -118.8021  -0.1737256  -19.02956  -32.16865  67.93389  -29.65444  46.15548

   :        :          :
```

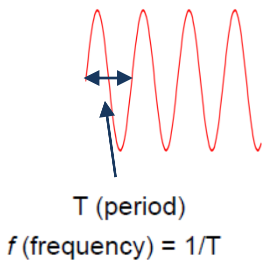
Frequency in GHz

S11, S12, …, S44 in dB and phase angle

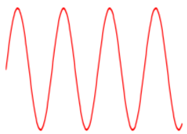
S-parameter란 무엇인가?

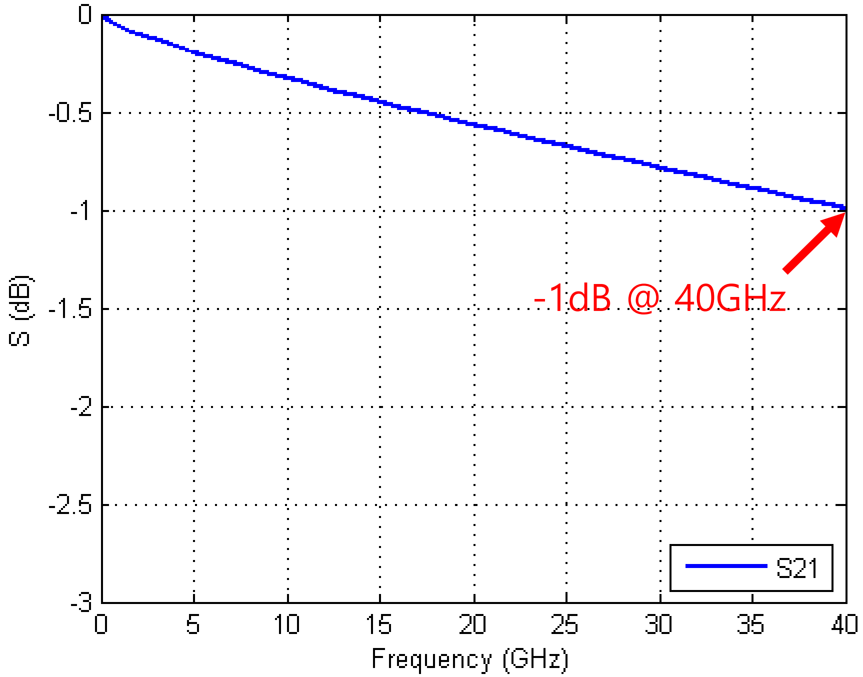
- **S21 or Insertion Loss**

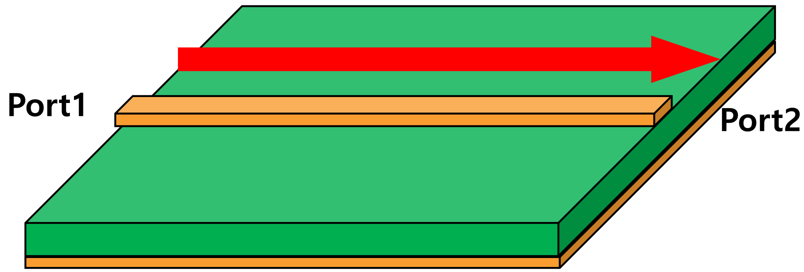
Incident wave:
1V, 40GHz



Transmitted wave:
0.89V, 40GHz



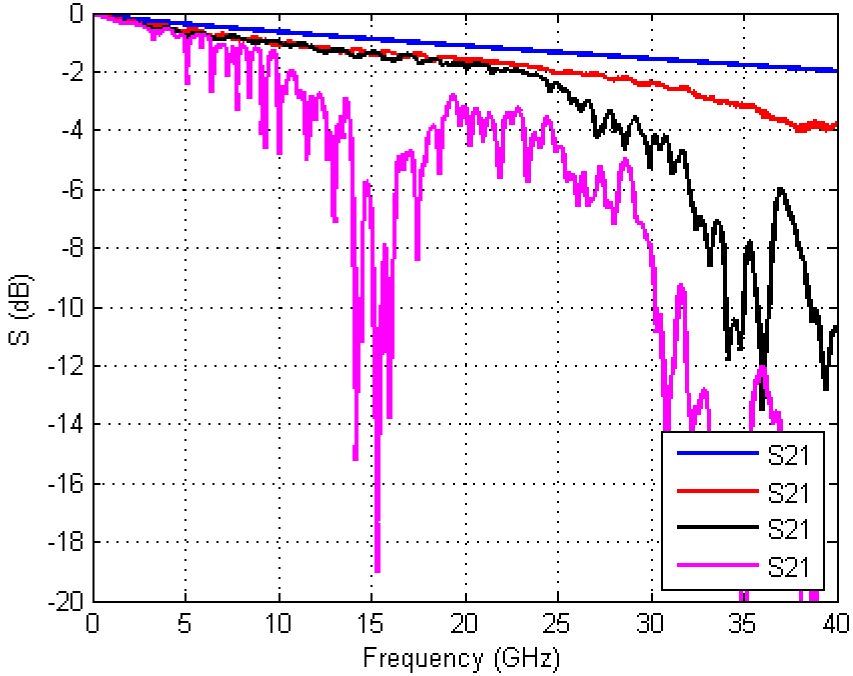


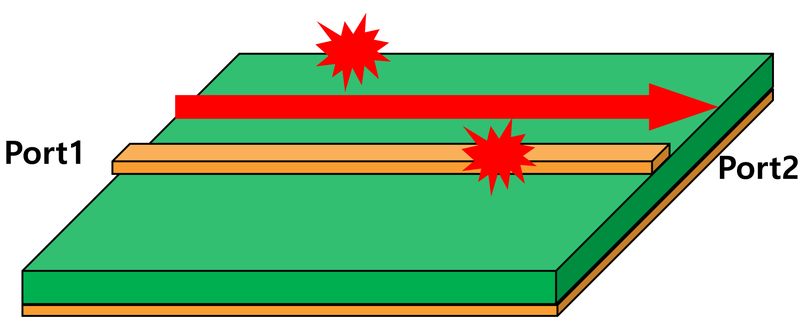


✓ **Passive Device에서는 S21과 S12는 대체로 동일하다.**

S-parameter란 무엇인가?

- **S21 or Insertion Loss: 문제 발생**
  - ✓ Loss
  - ✓ Resonance
  - ✓ Skew(Differential)
  - ✓ Impedance mismatching

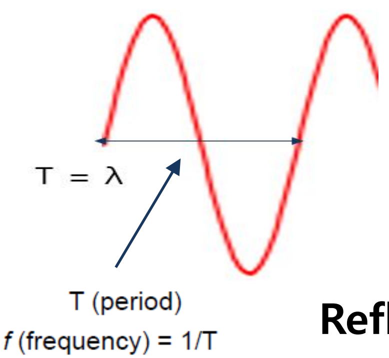




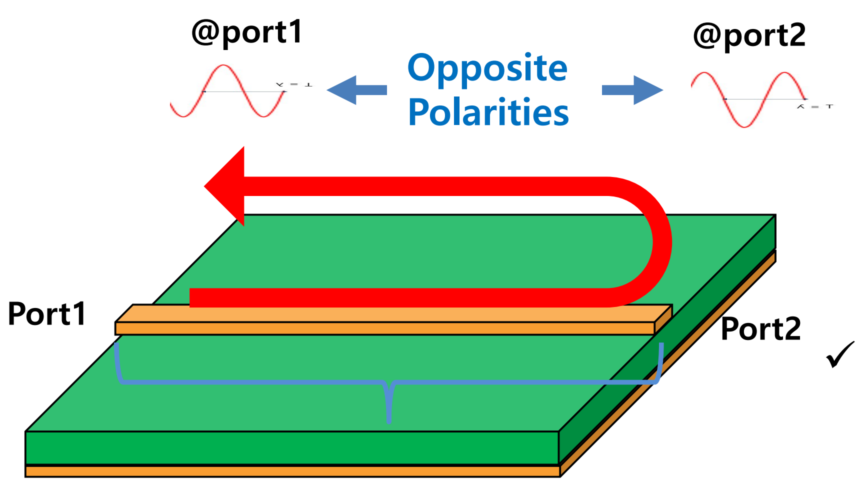
S-parameter란 무엇인가?

- **S11 or Return Loss**

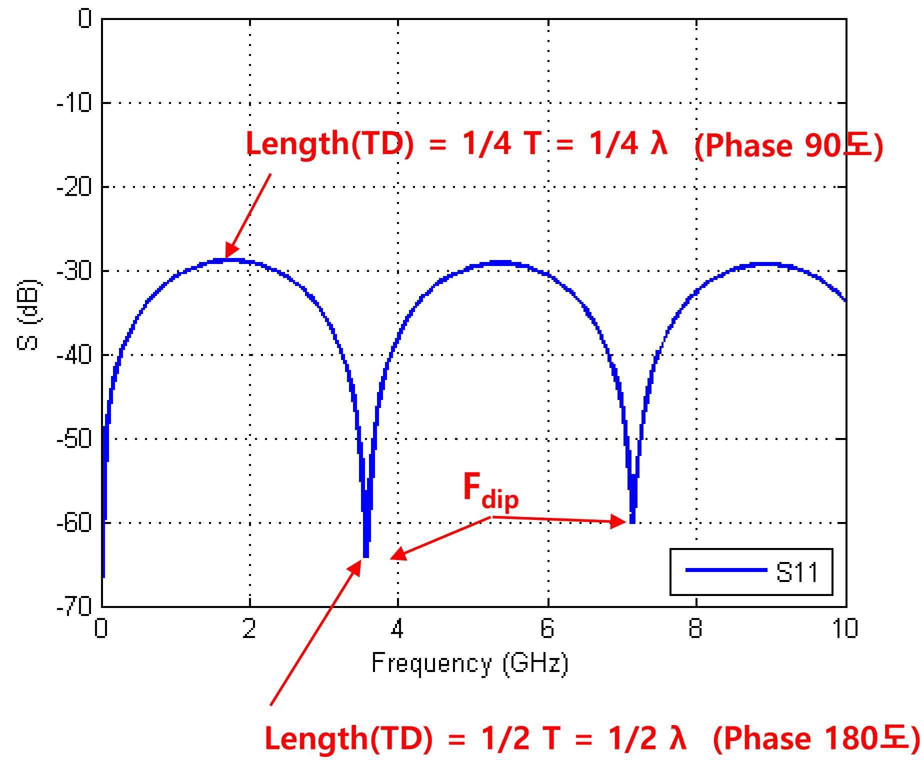
Incident wave



Reflected wave: $Z_{dut} \neq Z_{ref}$



Length=Time delay

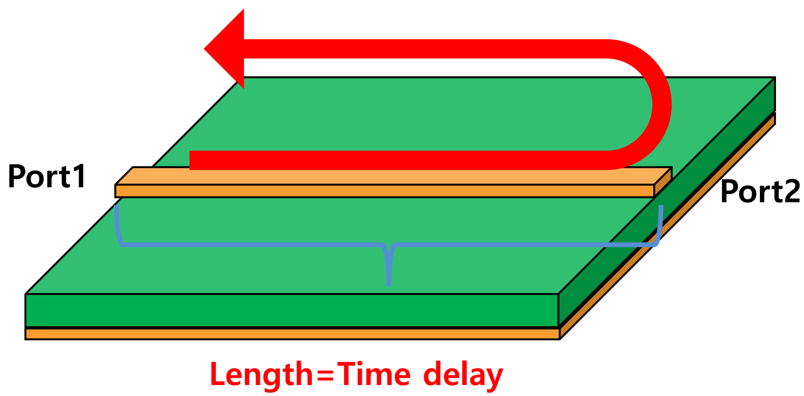


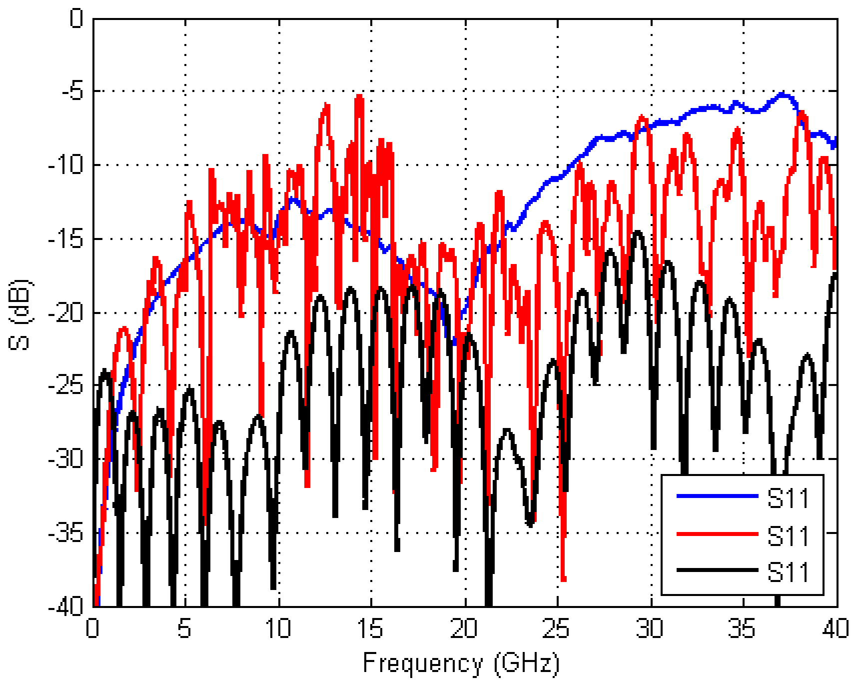
✓ Port1 & Port2 방향에서 특성이 동일한 symmetric 구조에서는 S11과 S22는 동일하다.

✓ F_{dip} 간격은 짧은 DUT에서 넓고, 긴 DUT에서 좁다. F_{dip} 간격= 1/(2*TD)

S-parameter란 무엇인가?

- **S11 or Return Loss: 문제 발생**
  - ✓ Impedance mismatching
  - ✓ Resonance
  - ✓ Multi reflection
  - ✓ Causality Error

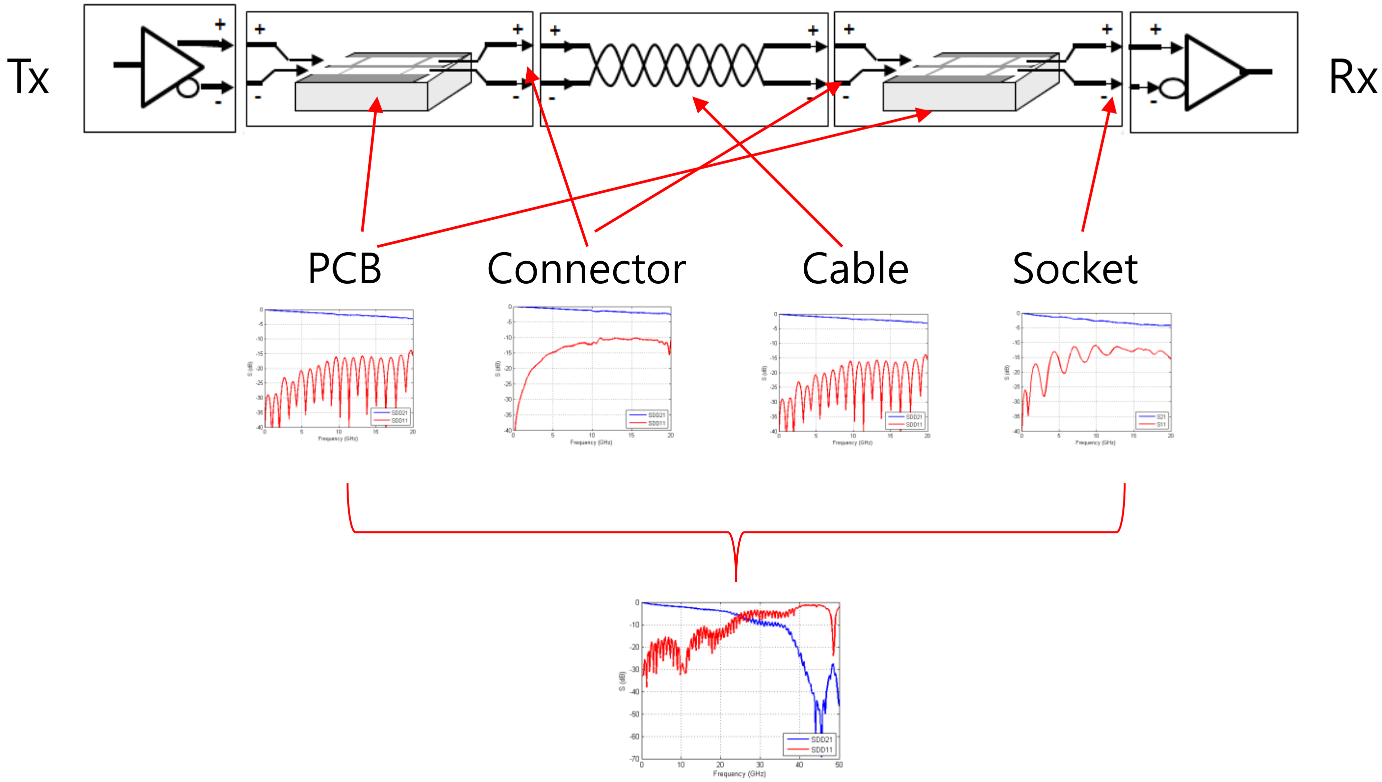




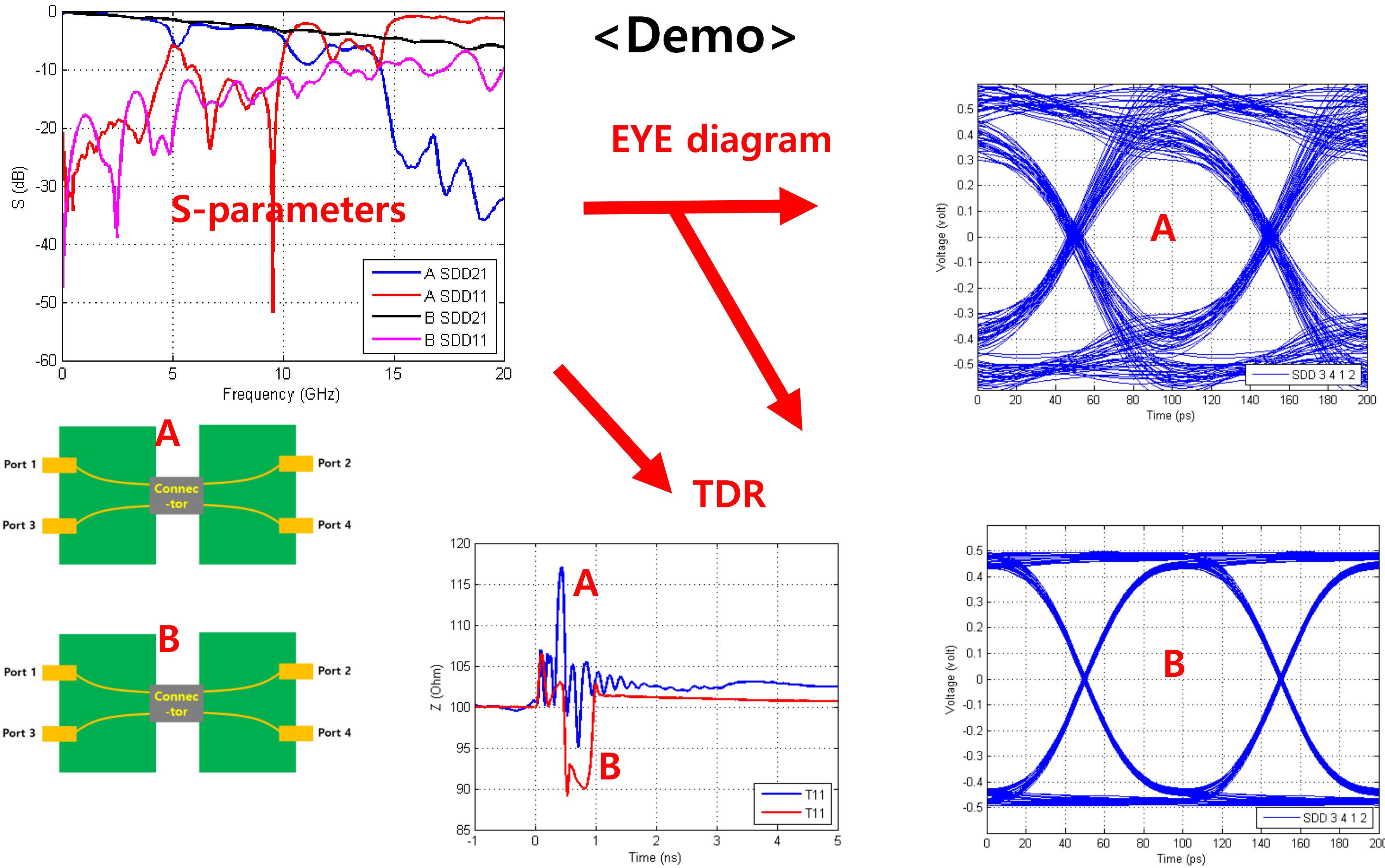
S-parameter란 무엇인가?

- **Interconnect system(Channel)의 S-parameters**

  Component, Channel, System의 Black Box 모델이자, 분석을 위한 정보



S-parameter란 무엇인가?



S-parameter에서의 에러: Causality

cau·sal·i·ty

/kôˈzalədē/

noun

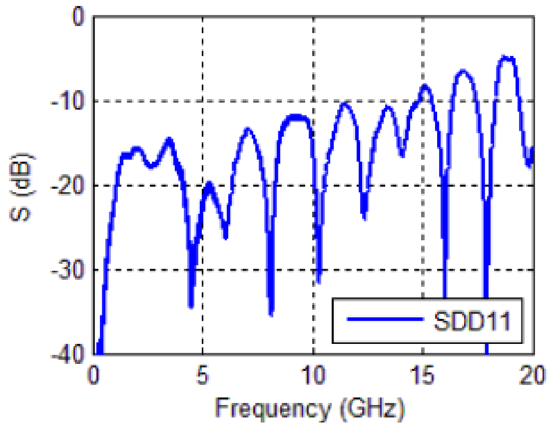
1. the relationship between cause and effect.
2. the principle that everything has a cause.

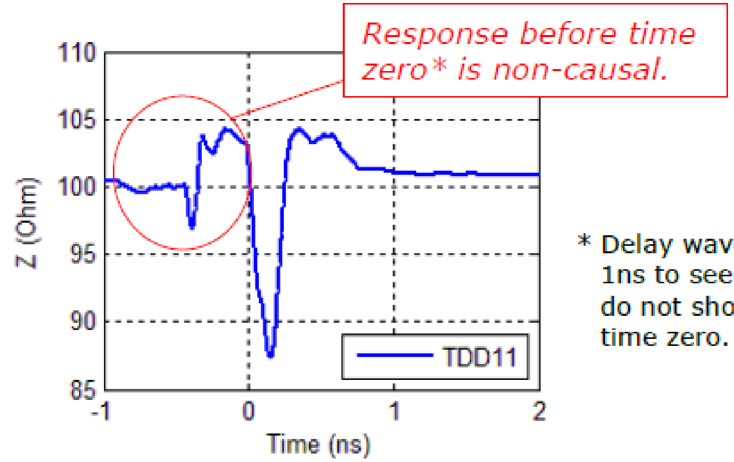
In other words:

Can not get something from nothing.

Non-causal S-parameter 현상

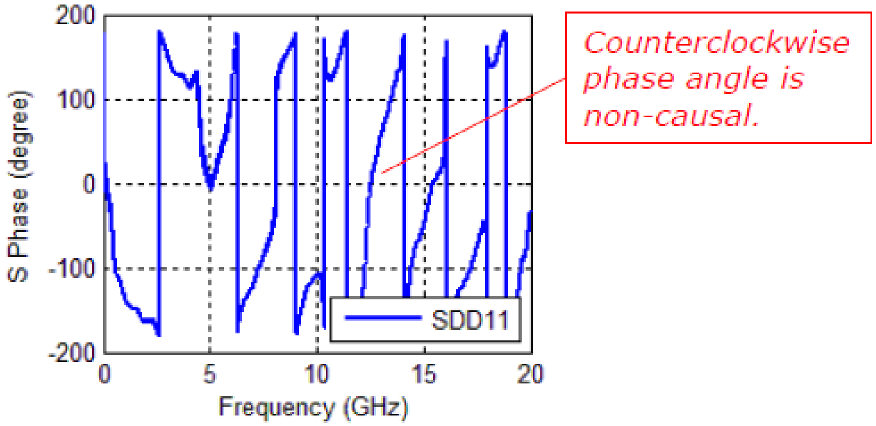
- Convert S parameter into TDR/TDT.





* Delay waveform by 1ns to see if tools do not show before time zero.

- Check phase angle.

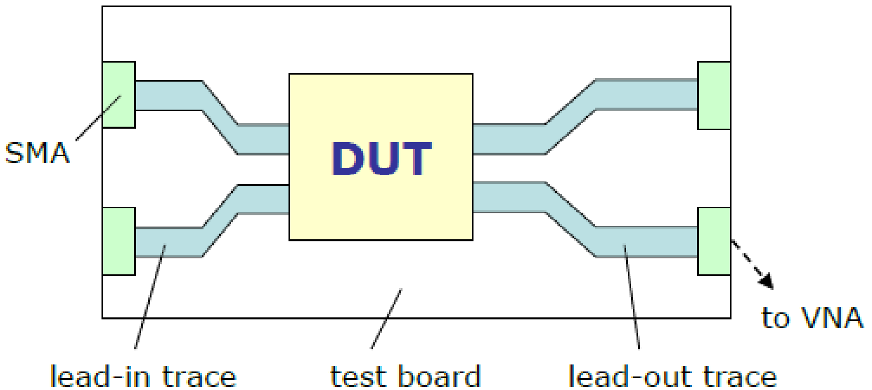


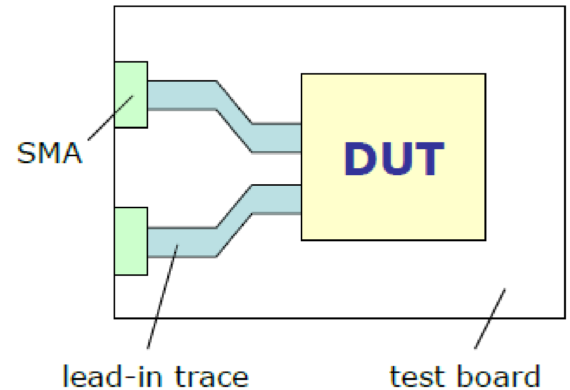
S-parameter가 causality를 위반하는 이유

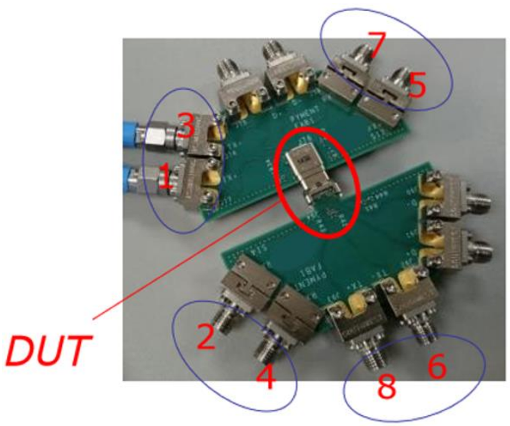
- Measurement error (de-embedding), simulation error (material property) and finite bandwidth of S parameter all contribute to non-causality.

De-embedding이란?

- To remove the effect of fixture (SMA connector + lead-in/out) and extract the S parameter of DUT (device under test).



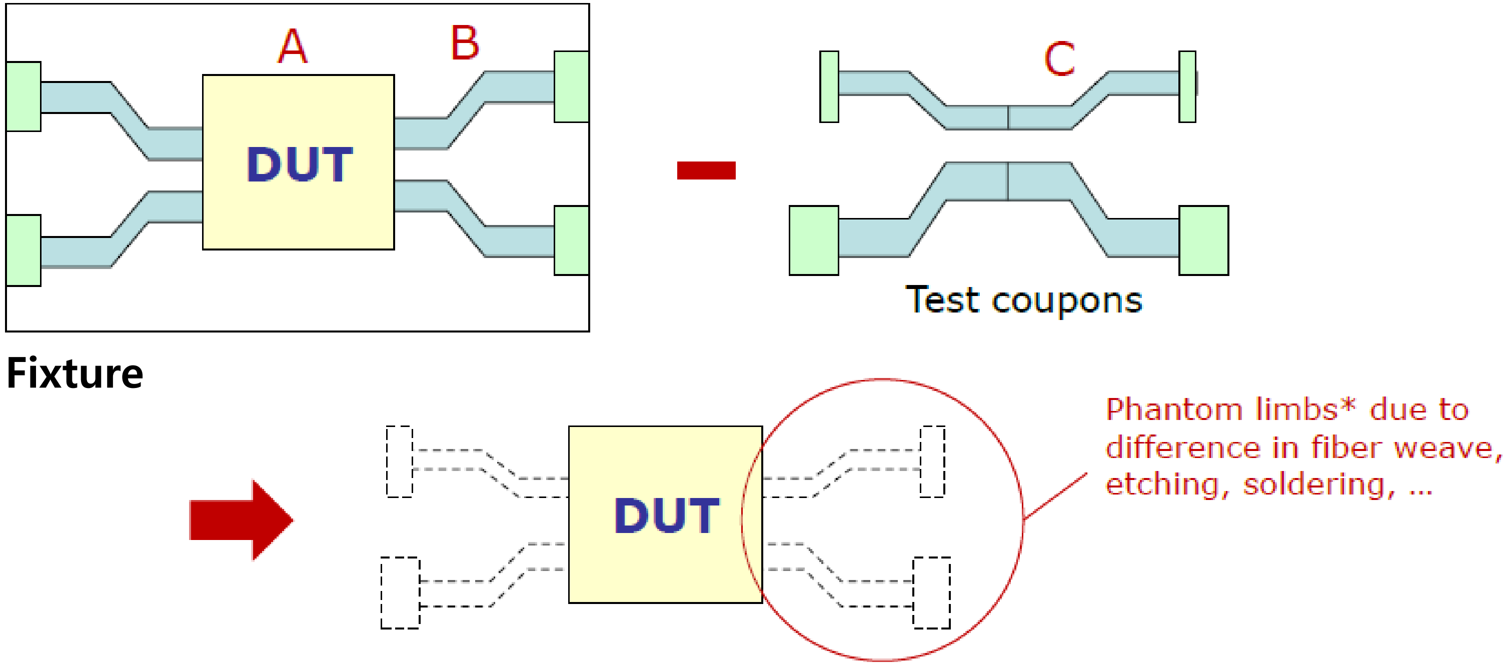




- The lead-ins and lead-outs don't need to look the same.
- There may even be no lead-outs (e.g., package).

왜 De-embedding 할 때 causality error가 발생하는가?

- Most tools use test coupons directly for de-embedding, so difference between actual fixture and test coupons gets piled up into DUT results.

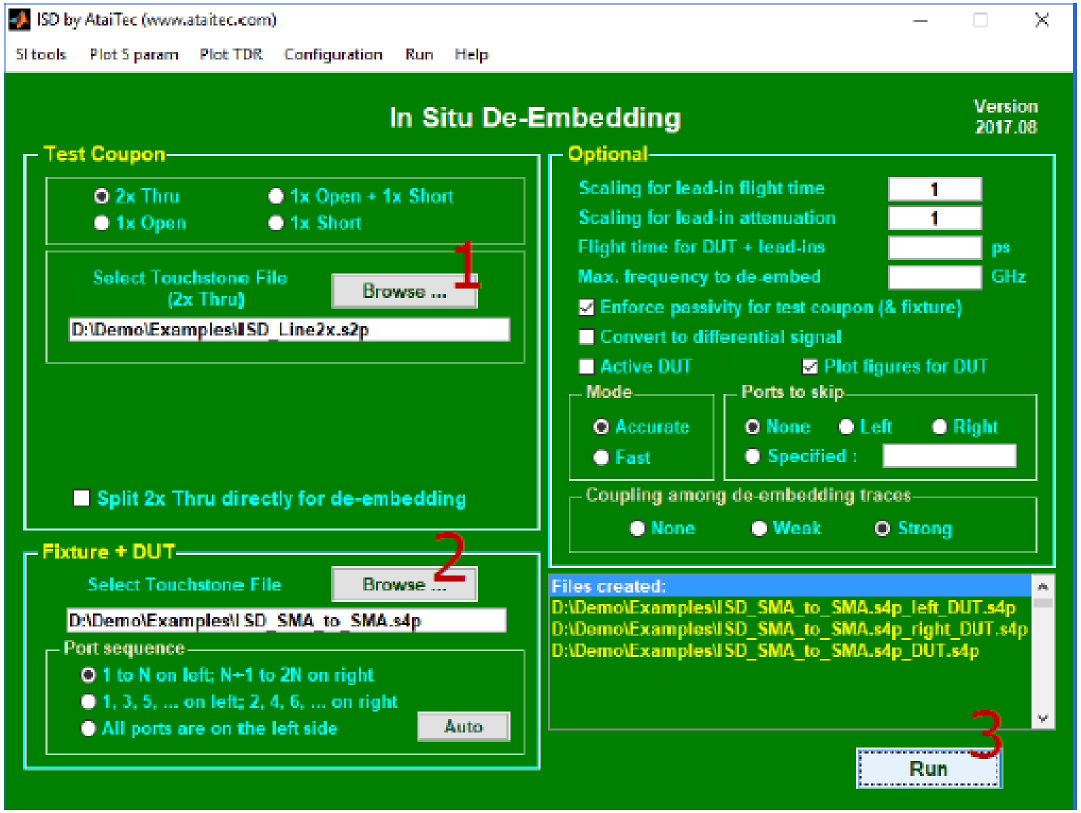


* http://www.edn.com/electronics-blogs/test-voices/4438677/Software-tool-fixes-some-causality-violations by Eric Bogatin

In-Situ De-embedding(ISD)이란?

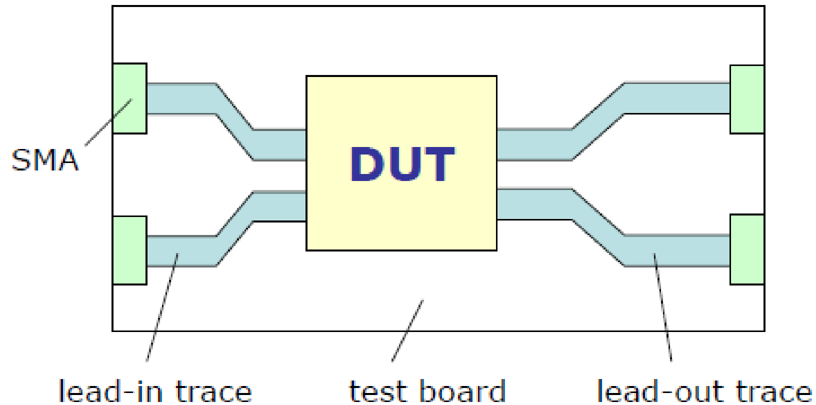
- Use "2x thru" or "1x open / 1x short" as reference and de-embed fixture's actual impedance through numerical optimization.

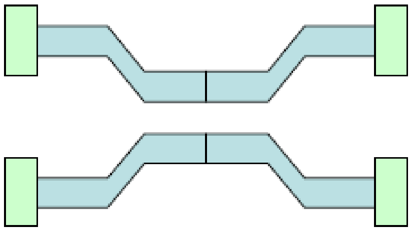
In Situ



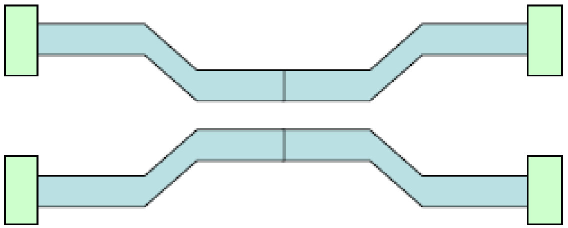
2x thru

- "2x thru" is 2x lead-ins or lead-outs.





2x thru for lead-ins

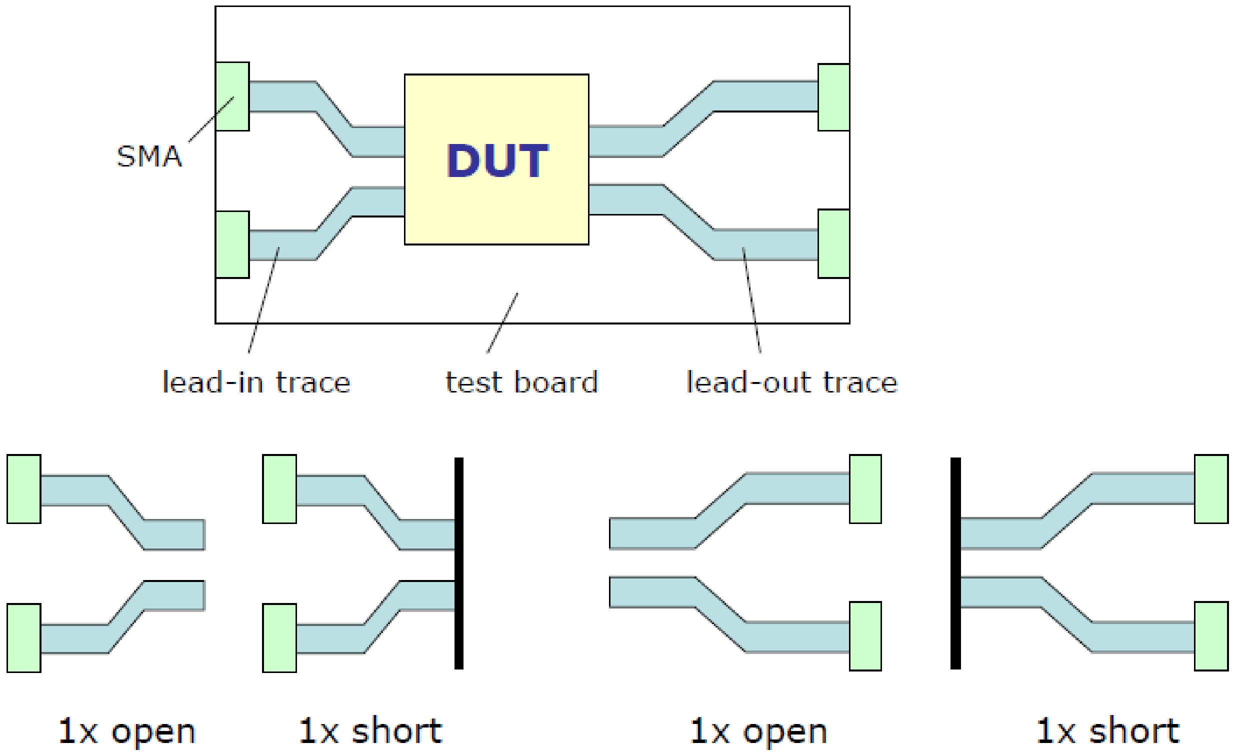


2x thru for lead-outs

2 sets of "2x thru" are required for asymmetric fixture.

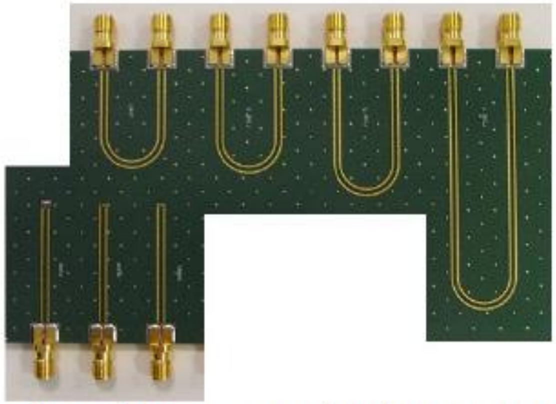
1x open / 1x short

- "1x open / 1x short" is useful when "2x thru" is not possible (e.g., connector vias, package, ...).



ISD가 더 정확하고 비용절감에 유리한 이유

TRL calibration board



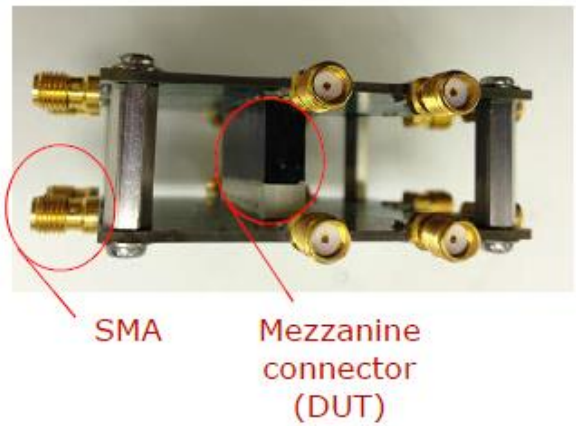
- More board space - Multiple test coupons are required.
- Test coupons are used directly for de-embedding.
- All difference between calibration and actual DUT boards gets piled up into DUT results.
- Expensive SMAs, board materials (Roger) and tight-etching-tolerance are required.
  - Impossible to guarantee all SMAs and traces are identical (consider weaves, etching, …)
- Time-consuming manual calibration is required.
  - Reference plane is in front of DUT.

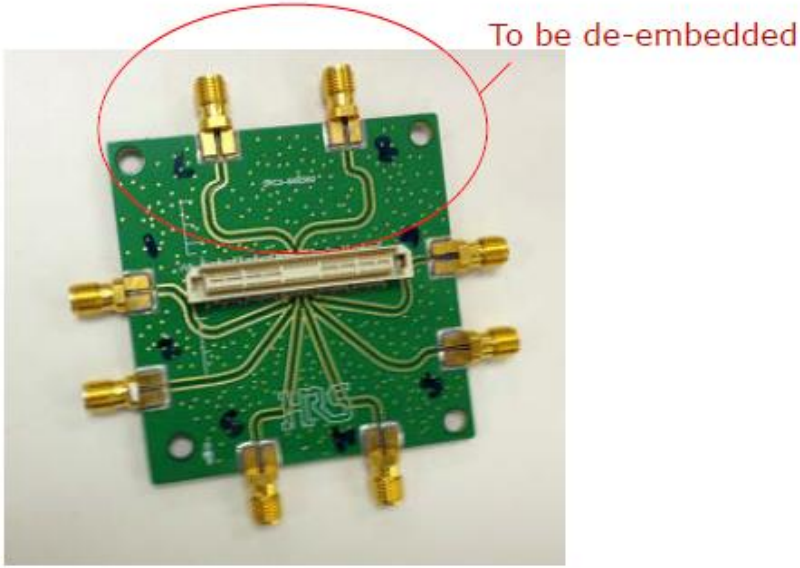
ISD test coupon

- Only one 2x thru test coupon is needed.
- Test coupon is used only for reference, not for direct de-embedding.
- Actual DUT board impedance is de-embedded.
- Inexpensive SMAs, board materials (FR4) and loose-etching-tolerance can be used.
- ECal can be used for fast SOLT calibration.
  - Reference plane is in front of SMA.
  - De-embedding requires only two input files: 2x thru and DUT board (SMA-to-SMA) Touchstone files.
  - More information: Both de-embedding and DUT files are provided as outputs.

예제 1: Mezzanine connector, ISD vs TRL

- In this example, we will use ISD and TRL to extract a mezzanine connector and compare their results.

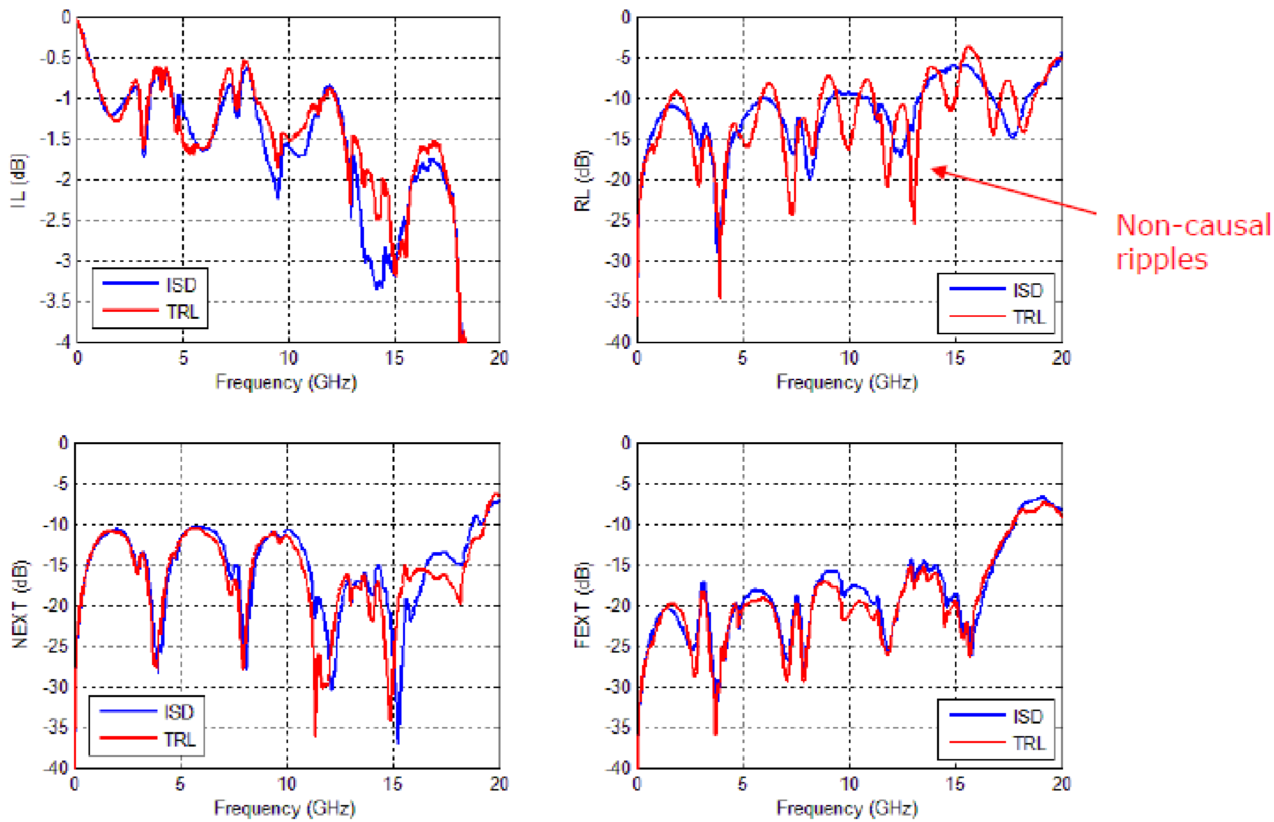




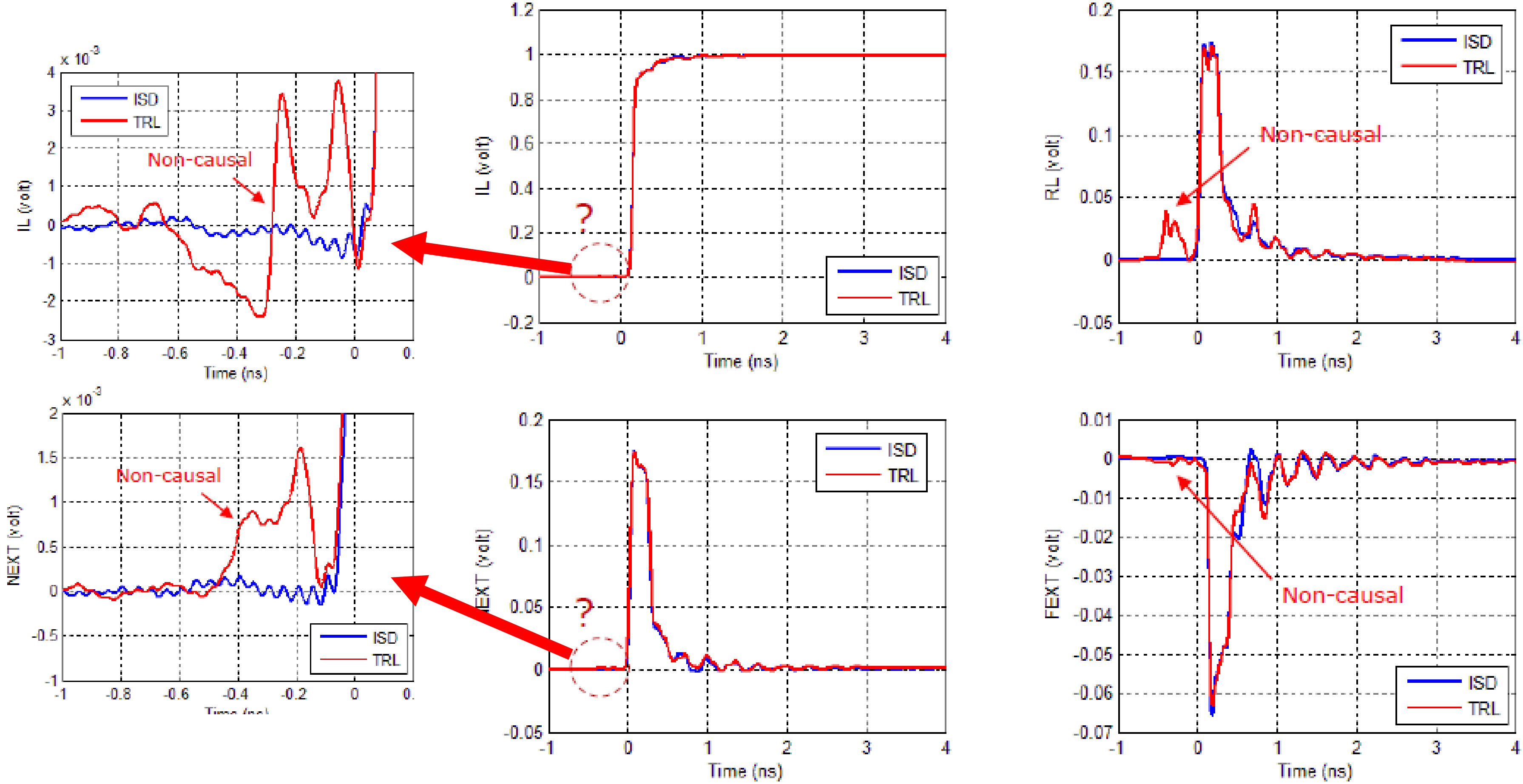
*Courtesy of Hirose Electric

De-embedding 결과

- TRL gives too many ripples in return loss (RL) for such a small DUT.

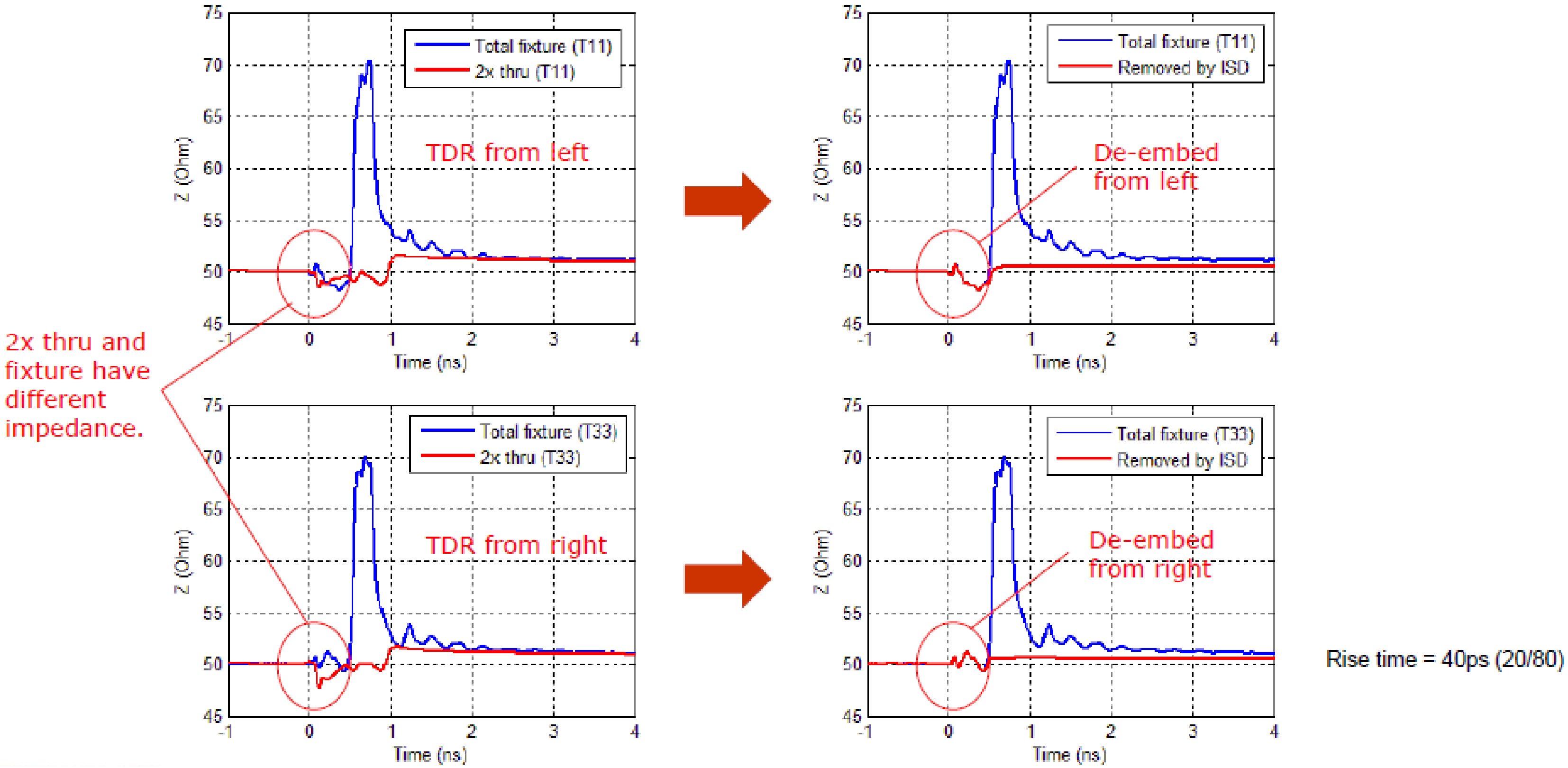


S-parameter를 TDR/TDT로 변환했을 때의 Causality 에러



ISD의 De-embedding 방식

- Through numerical optimization, ISD de-embeds fixture's impedance exactly, independent of 2x thru's impedance.



예제 2. 큰 사이즈의 보드(fixture)로부터 De-embedding

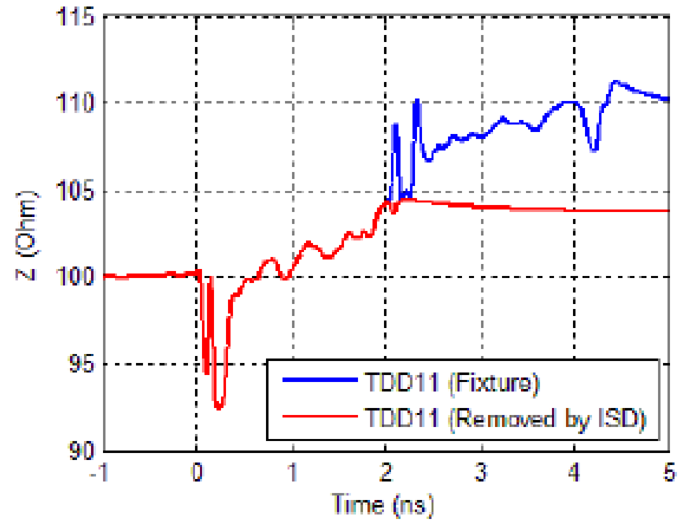
- TRL에서 DUT에 비해 매우 긴 Fixture의 Lead-in/out을 정확하게 매칭하는 것은 현실적으로 거의 불가능

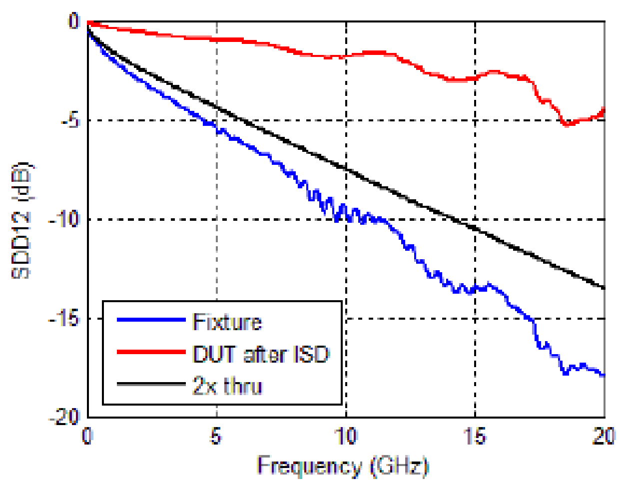
Fixture

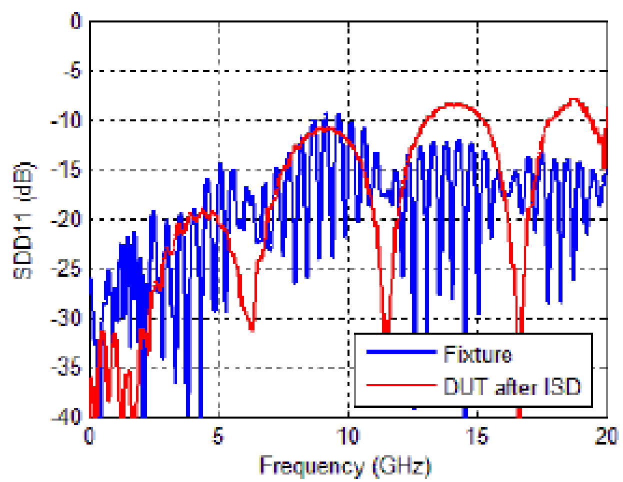
2x thru
(12″ total)

Mezzanine
connector
(DUT)

ISD의 De-embedding 결과

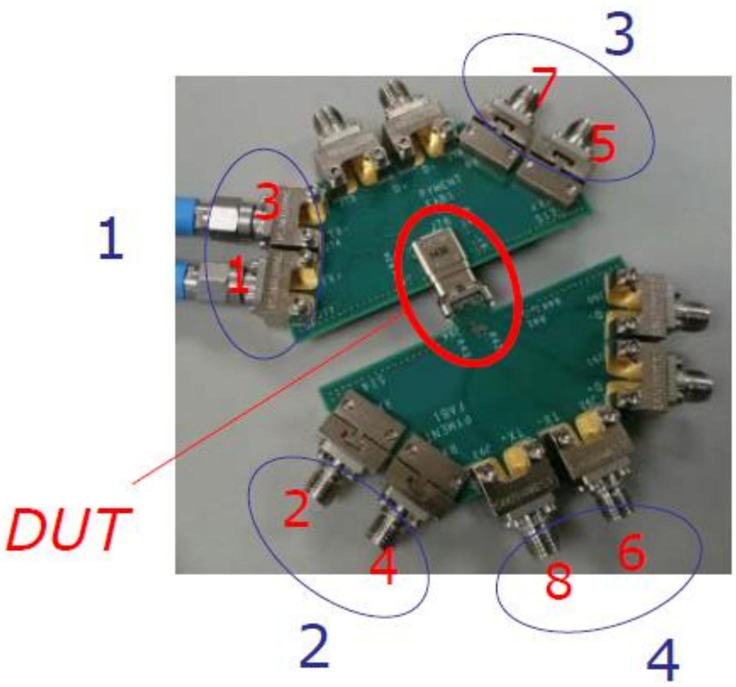


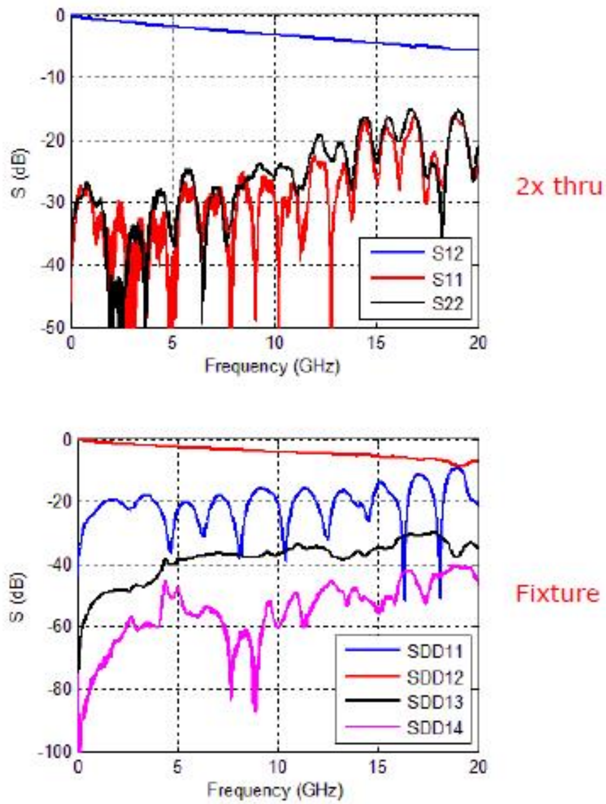




예제 3. USB type C 커넥터: ISD와 다른 SW tool A 비교

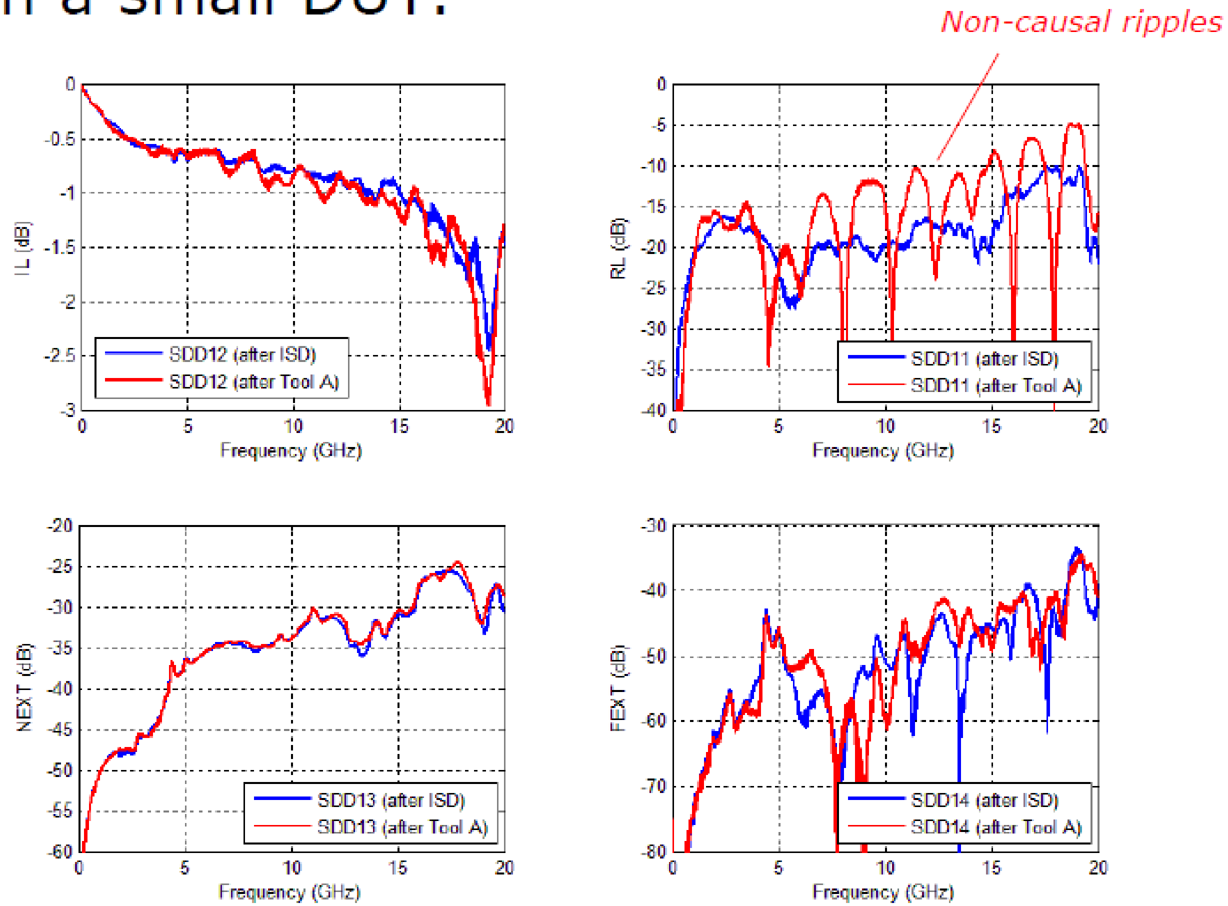
- Good de-embedding is crucial for meeting compliance spec.





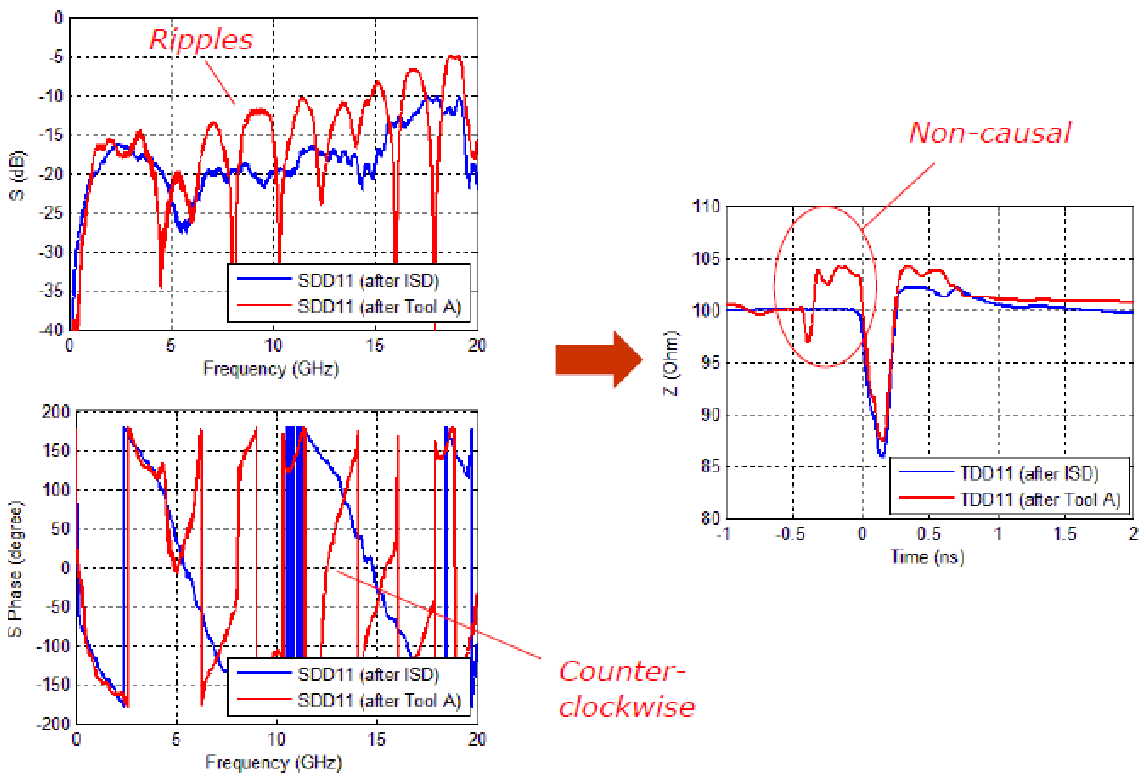
ISD와 Tool A의 결과 비교

- Tool A gives too many ripples in return loss (RL) for such a small DUT.



TDR/TDT로 변환했을 때의 Non-causality 비교

- Counter-clockwise phase angle is another indication of non-causality.

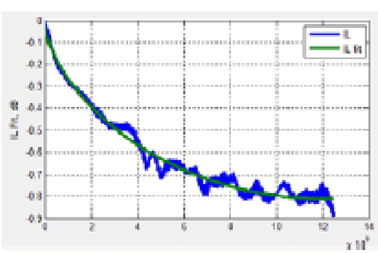


Compliance spec에 미치는 De-embedding 결과

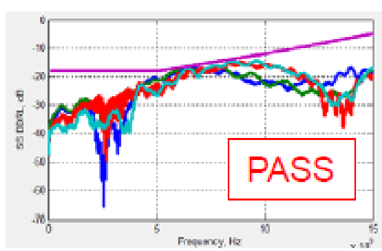
- ISD improves IMR and IRL (from compliance tool).

ISD

	Value (Pass/Fail)
ILfit@2.5GHz	-0.4
ILfit@5.0 GHz	-0.6
ILfit@10.0GHz	-0.8
IMR	-45.1
IRL	-23.2
INEXT	-41.5
IFEXT	-49.2
SCD12/SCD21	-23



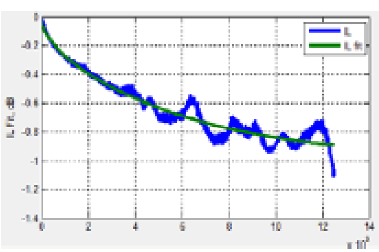
IL



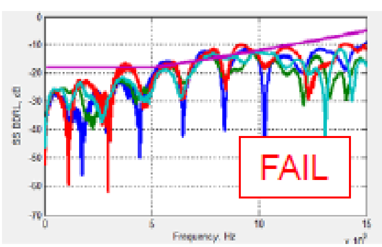
RL

Tool A

	Value (Pass/Fail)	Spec
ILfit@2.5GHz	-0.4	-0.6
ILfit@5.0 GHz	-0.6	-0.8
ILfit@10.0GHz	-0.9	-1.0
IMR	-43.7	-40
IRL	-20.8	-18
INEXT	-41.5	-44
IFEXT	-49.3	-44
SCD12/SCD21	-23.2	



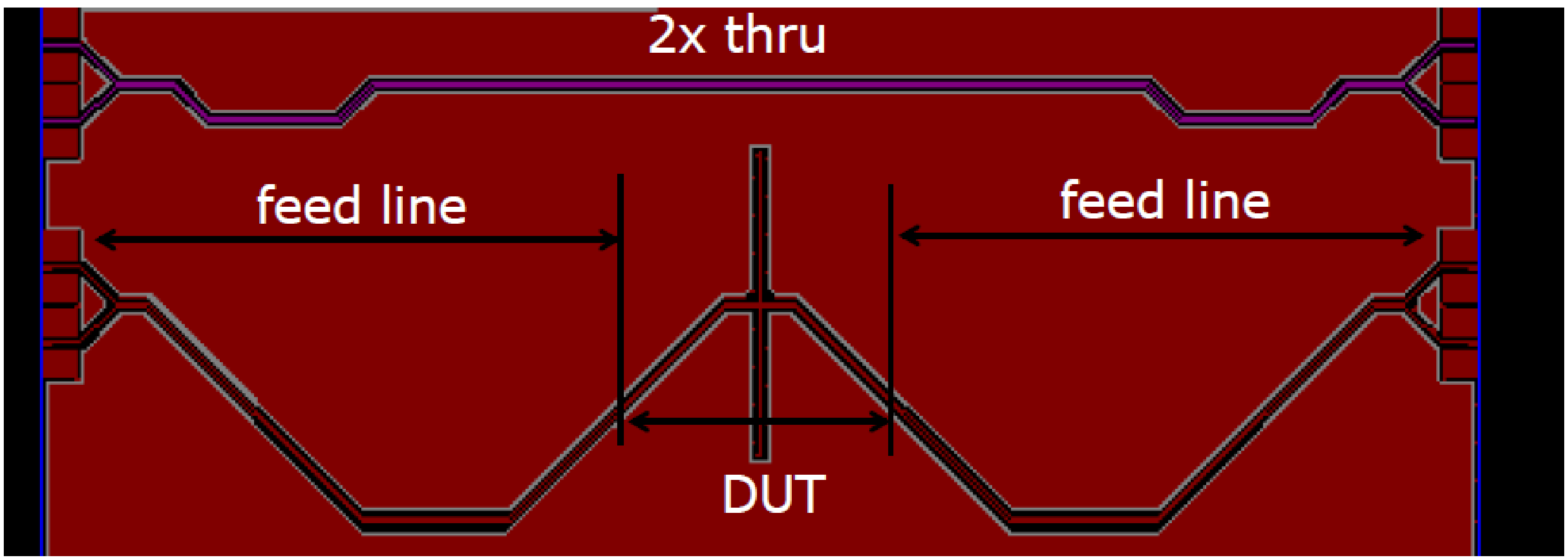
IL



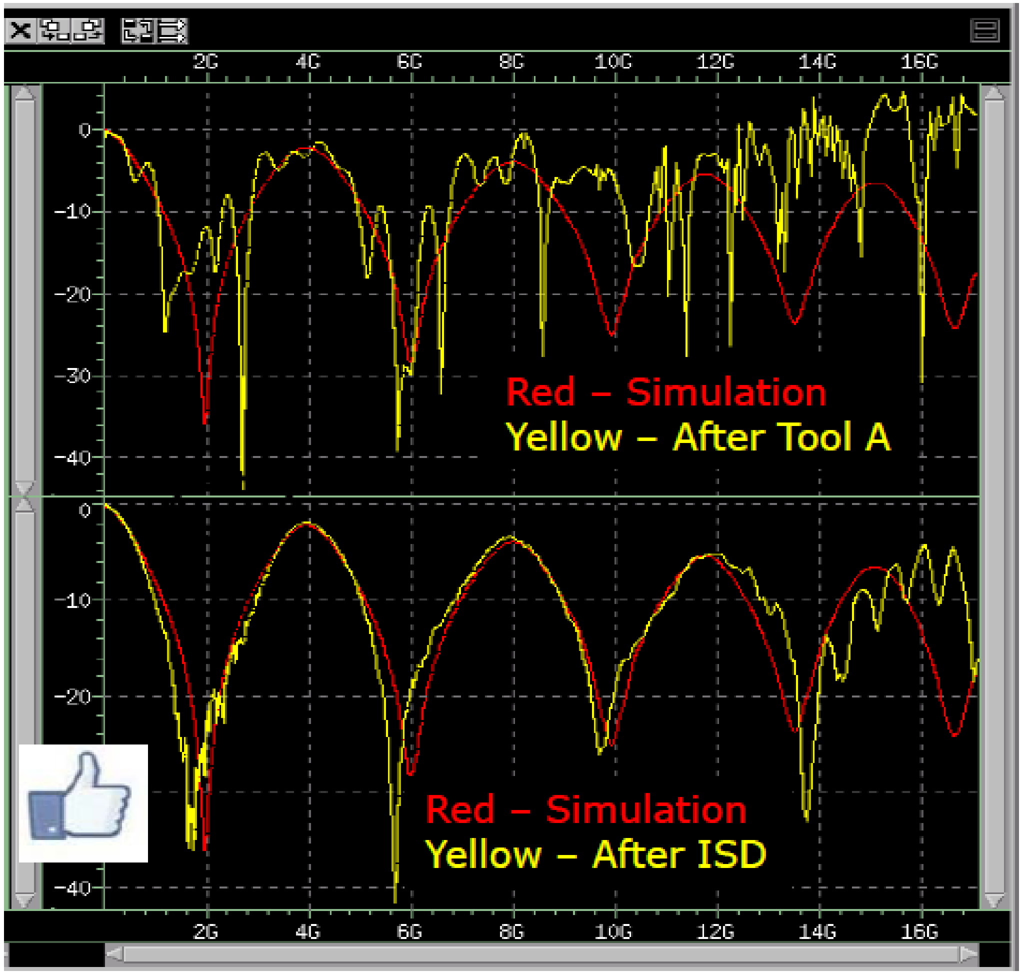
RL

예제 4. Resonator: ISD vs Tool A vs simulation

- Good de-embedding is crucial for design verification (i.e., correlation) and improvement.

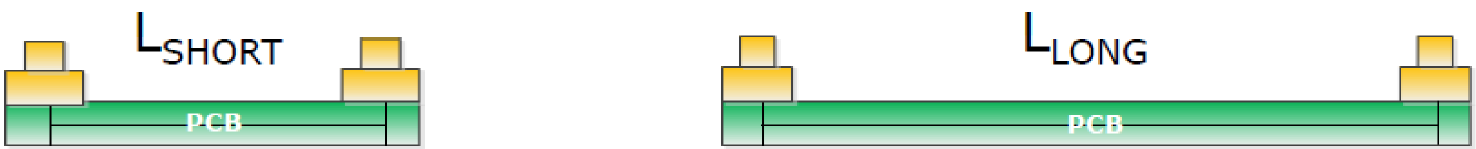


SDD11: ISD vs Tool A vs simulation

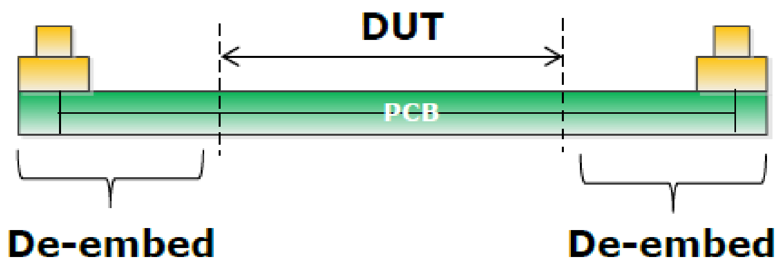


예제 5. PCB trace attenuation: ISD vs eigenvalue

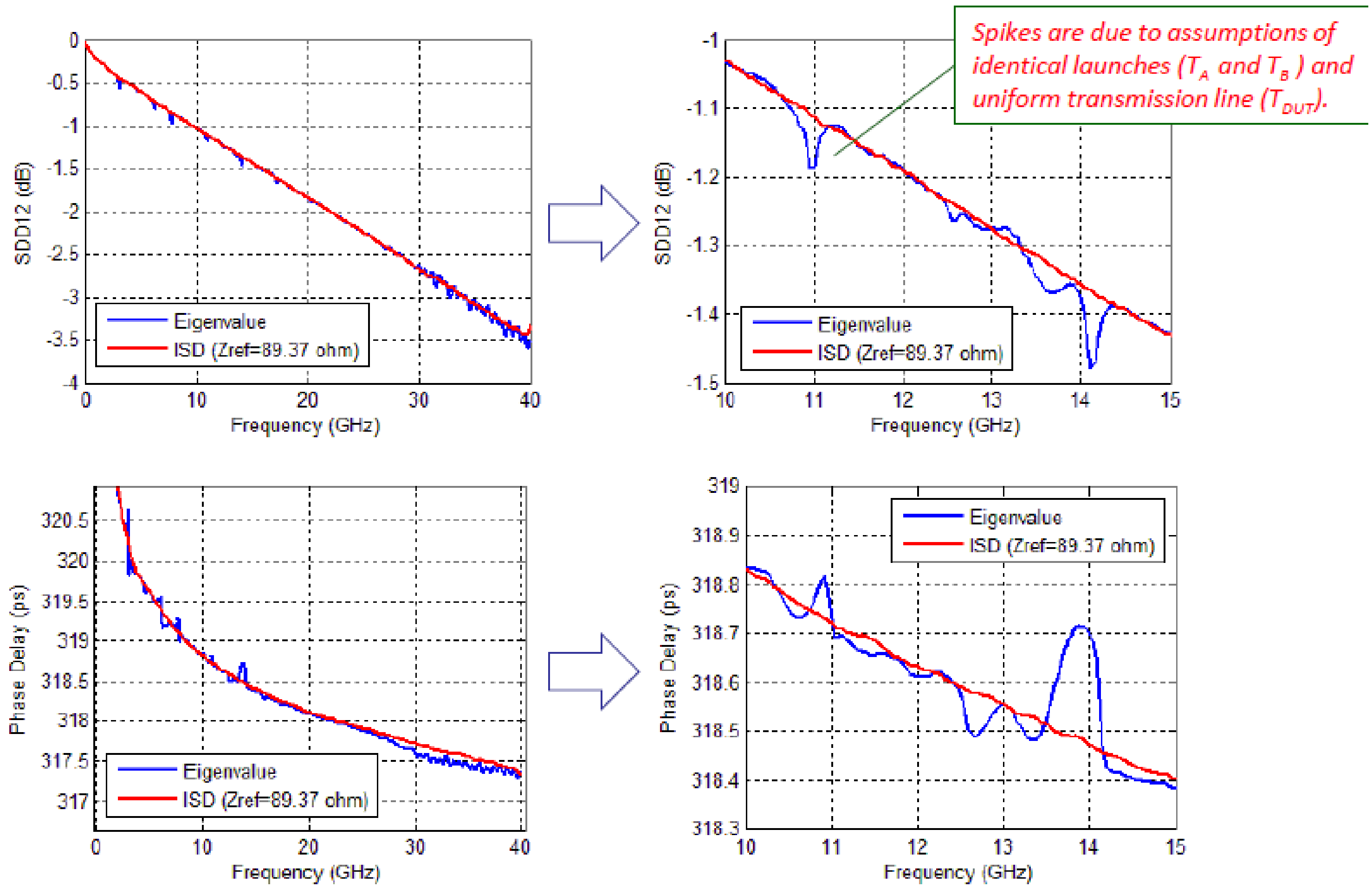
- De-embed short trace (+ launch) from long trace (+ launch) to get trace-only attenuation.



$$L_{DUT} = L_{LONG} - L_{SHORT}$$



2” (=7”-5”) trace attenuation



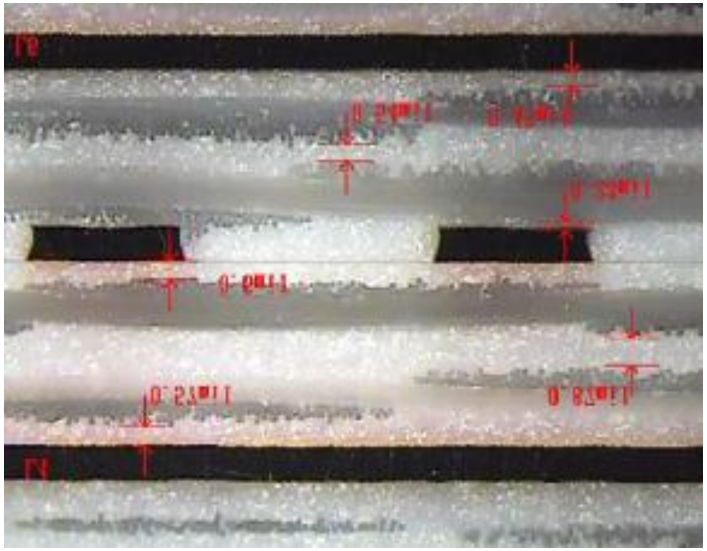
ISD’s spike-free results help DK and DF extraction later.

Material Property Extraction

Dk, DF and roughness

PCB의 Material Properties와 S-parameter에 주는 영향

Metal(Conductor)의 특성:
Conductivity
Roughness



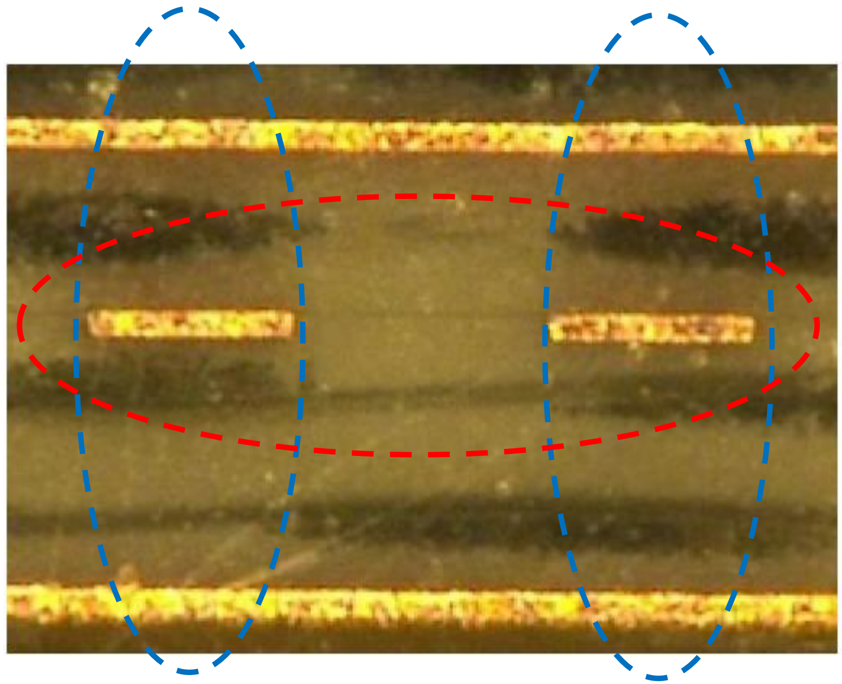
Dielectric Material 특성:
DK (Dielectric Constant; ε_r)
DF (Loss tangent)

Material Property가 PCB 특성에 주는 영향:

Conductivity → Insertion Loss(IL)
Roughness → Insertion Loss(IL)
DK → Impedance(TDR/TDT), Return Loss(RL), Phase(delay)
DF → Insertion Loss(IL)

MPX에서 DK, DF, roughness을 추출하기 위해 사용하는 fitting parameters

Single-end:
Insertion loss
Return loss
TDR, TDT

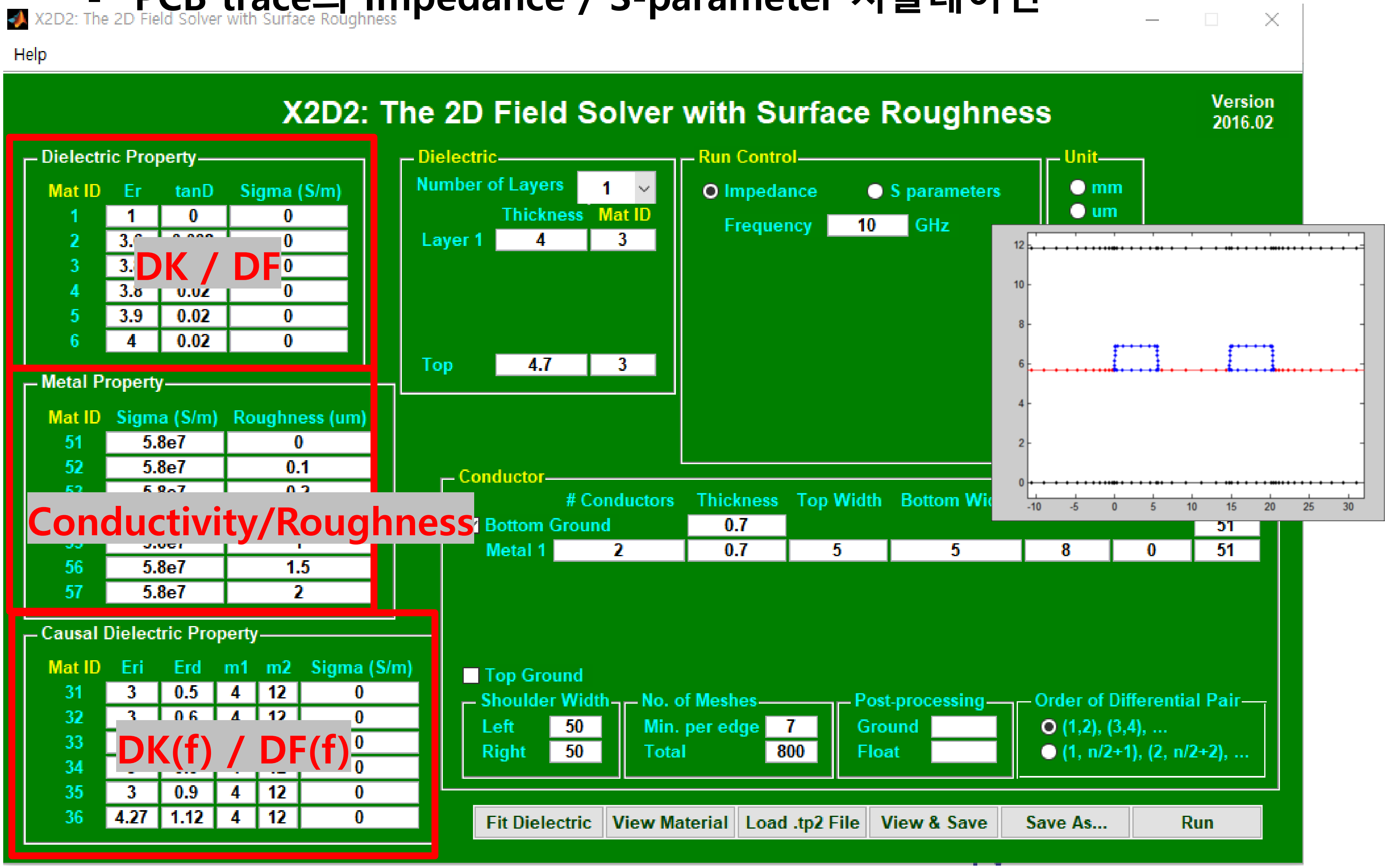


Differential:
Insertion loss
Return loss
TDR, TDT

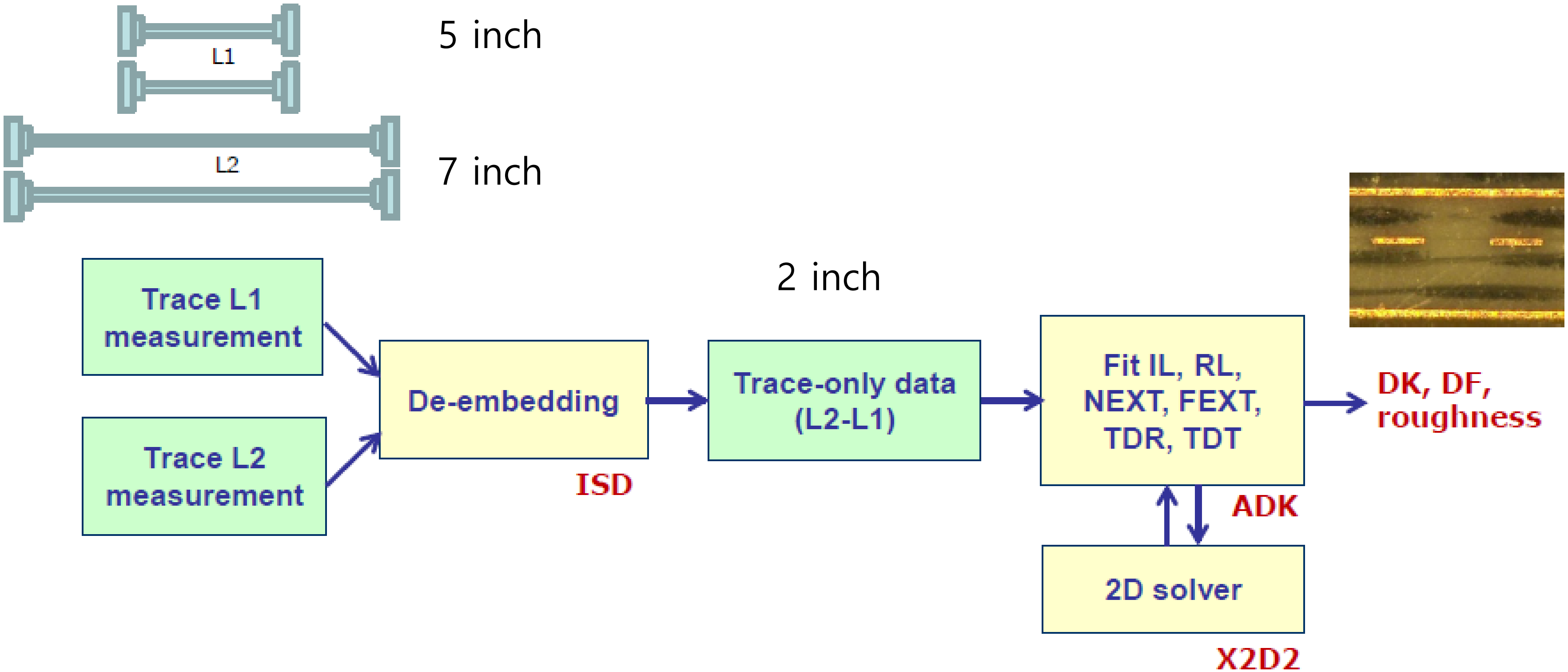
NEXT/FEXT

Material Property Setup: X2D2 2D solver

- PCB trace의 Impedance / S-parameter 시뮬레이션

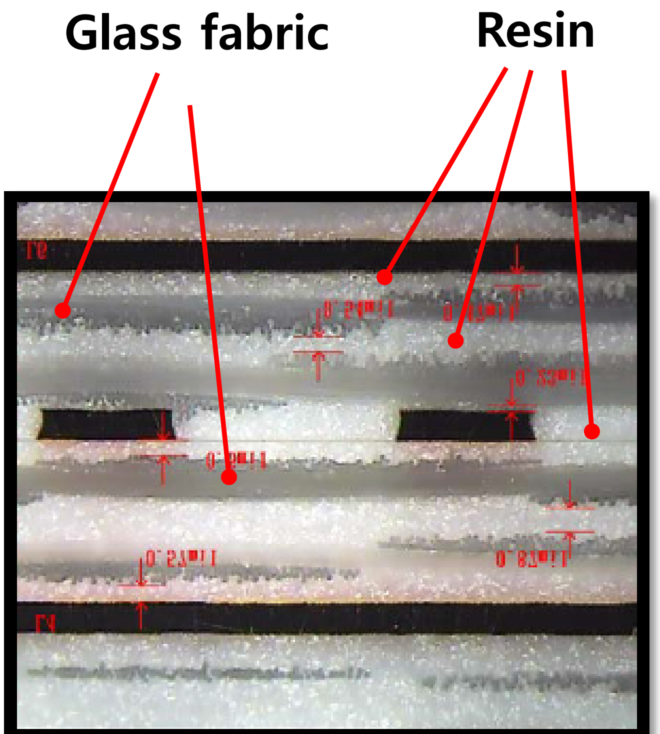


MPX의 automated flow

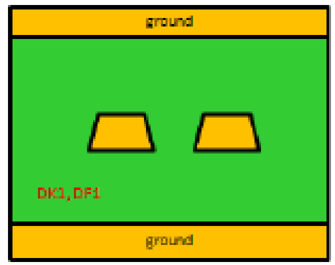


Automated extraction flow

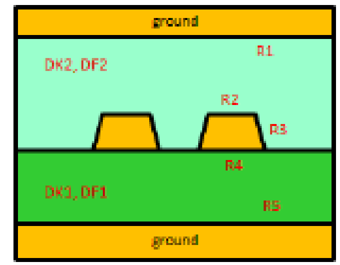
Cross section Models



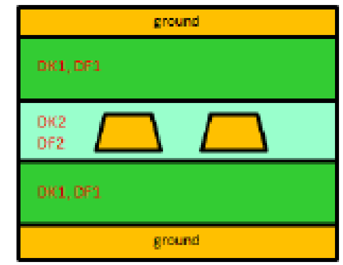
Optimized variables:
DK1, DF1, DK2, DF2
R1, R2, R3, R4, R5 (roughness)
Metal width and spacing



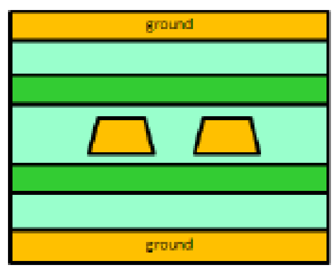
Model 1



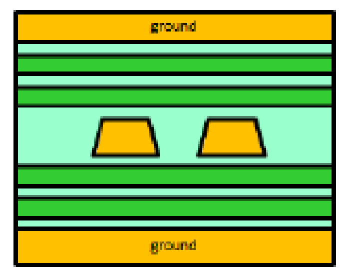
Model 2



Model 3



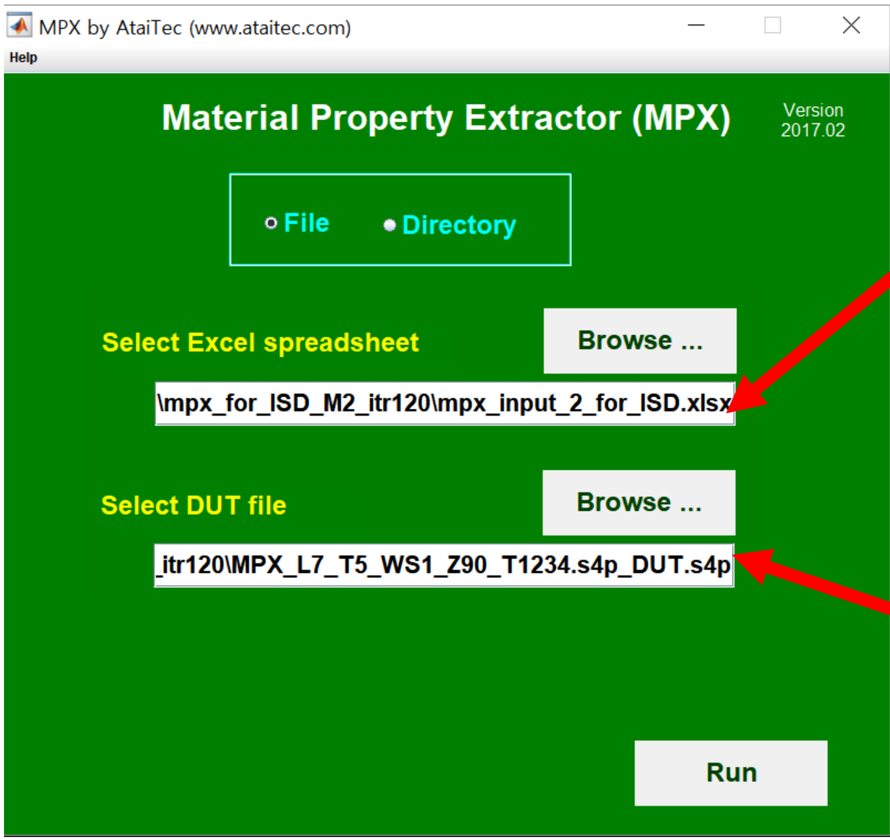
Model 4

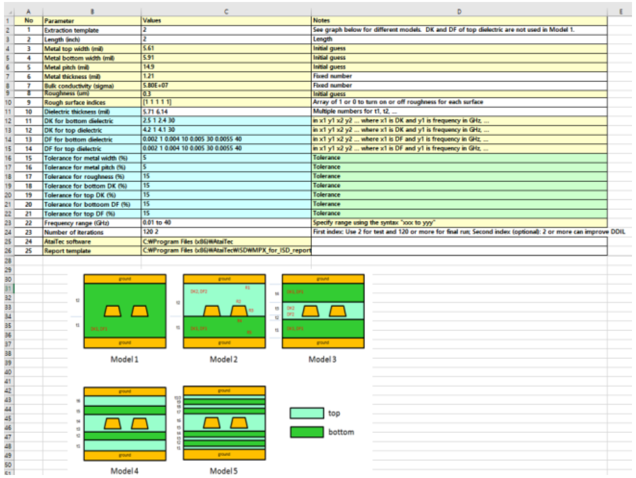


Model 5

- 다른 모델 추가 가능

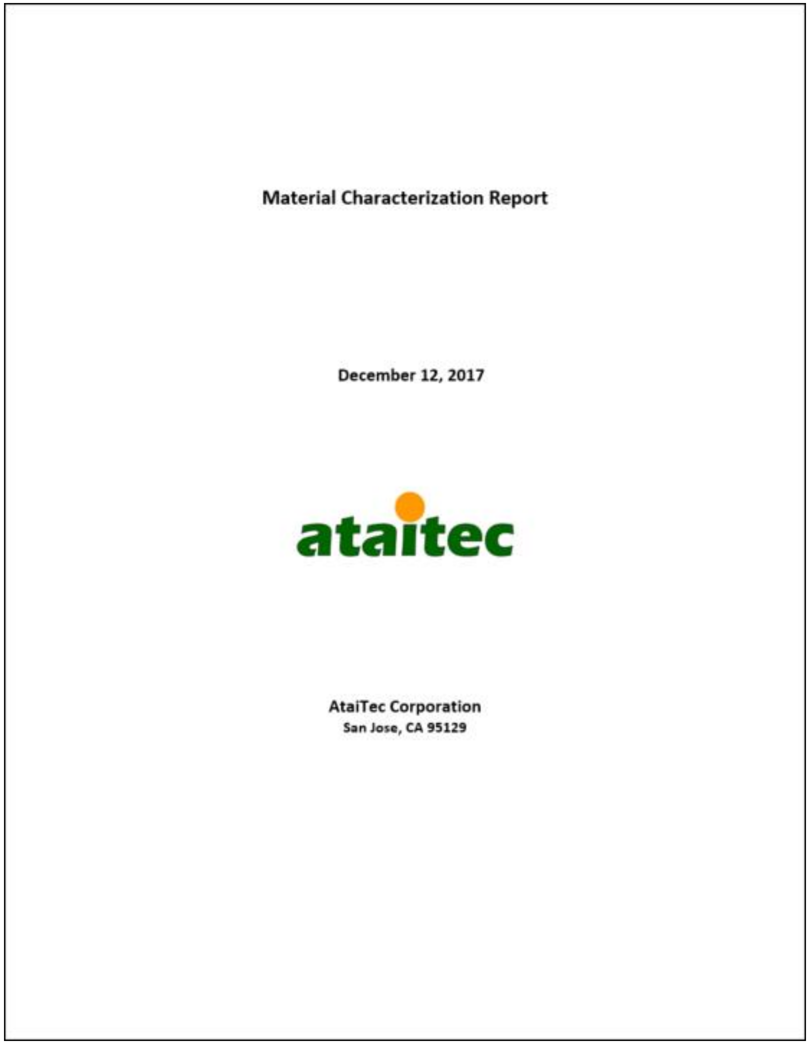
MPX의 실행 방법





이름	수정한 날짜	유형	크기
measured_sparameter	2017-02-05 오전 9:20	S4P 파일	530KB

MPX의 실행 결과


Material Characterization Report

December 12, 2017

ataitec

AtaiTec Corporation
San Jose, CA 95129

Report 생성
Properties Summary 결과
Properties와 S-parameter, TDR/TDT plots

Conductivity(f), DK(f), DF(f) 데이터
Properties Summary 결과
Properties와 S-parameter, TDT/TDT plot

X2D2용 셋업 파일
Measurement와 fitting한 properties 적용

MPX의 실행 결과

- Extract된 Properties / Measurement 와 fitting 데이터의 correlation 결과 (report 중 일부 plot)

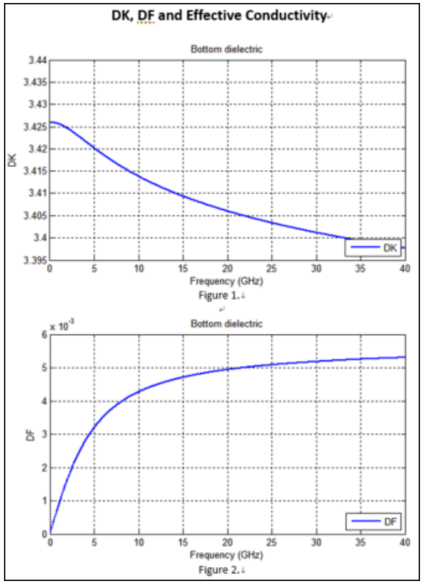


Figure 1.

Figure 2.

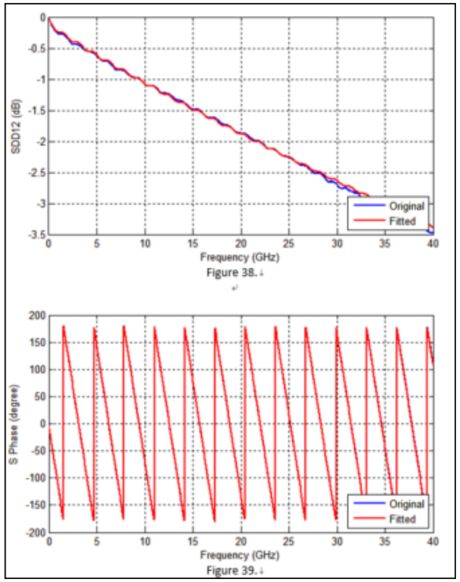


Figure 38.

Figure 39.

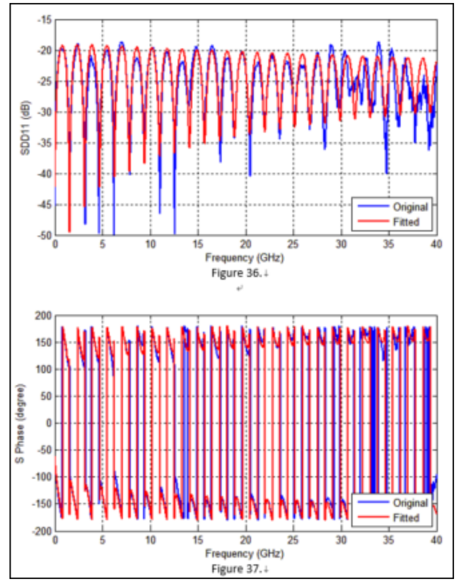


Figure 36.

Figure 37.

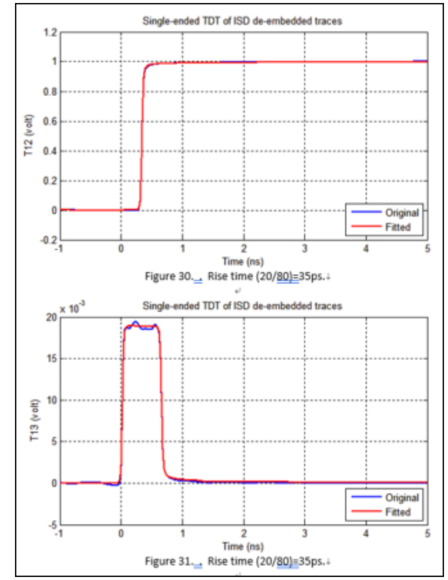


Figure 30. Rise time (20/80)=35ps.

Figure 31. Rise time (20/80)=35ps.

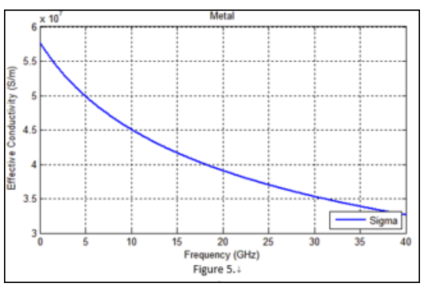


Figure 5.

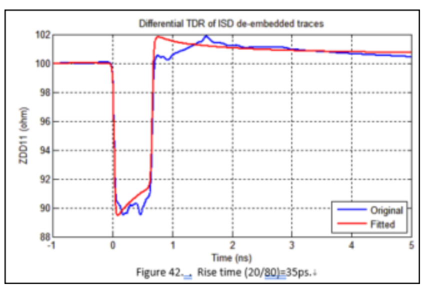


Figure 42. Rise time (20/80)=35ps.

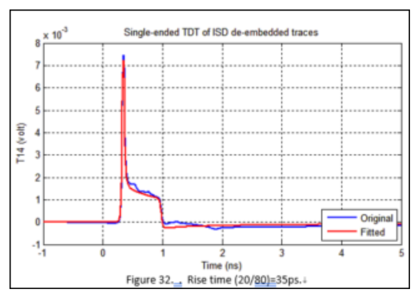


Figure 32. Rise time (20/80)=35ps.

Extracted Material Property

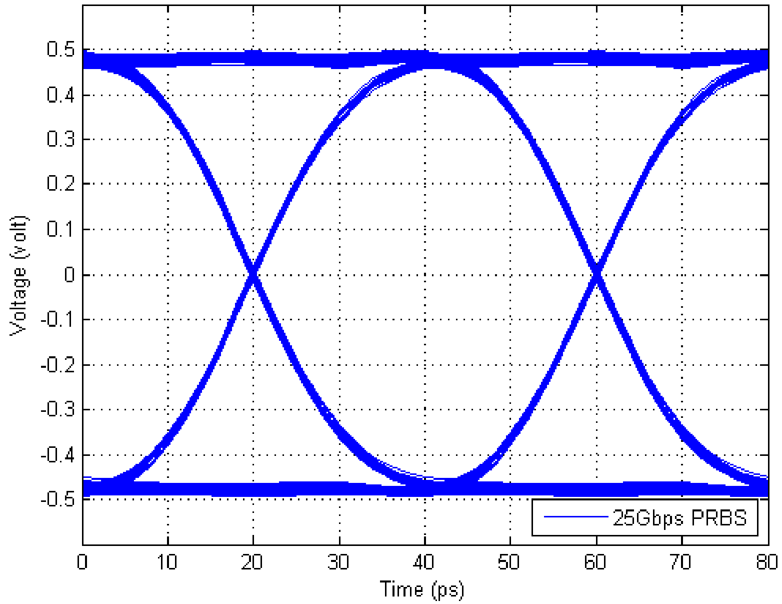
Directory: F:\OneDrive\Datafiles\Project\ataitec\MPX_demo\mpx_for_ISD_M3_240_3
File name: MPX_L7_T5_WS1_Z90_T1234.s4p_DUT.s4p

Extracted material property: (Model 3)
--- Dielectric ---
Bottom -> eri_1=3.27709, erd_1=0.148874, m1_1=9.60239, m2_1=14.8785
Top -> eri_2=3.48384, erd_2=0.150664, m1_2=9.60337, m2_2=15.0213
Equivalent model:
Bottom -> eri_1=3.27709, a_1=0.0122542, fh_1=7.56044e+14 Hz, fl_1=4.00303e+09 Hz
Top -> eri_2=3.48384, a_2=0.0120771, fh_2=1.05024e+15 Hz, fl_2=4.01212e+09 Hz
--- Metal ---
Sigma=5.8e+07 S/m, Roughness=0.30455 um
Top width (wt)=5.39893 mil, Bottom width (wb)=5.68764 mil
Pitch=14.9689 mil

Additional info:
No. of iterations=240 3
--- Dielectric ---
Bottom (constant approx.) -> DK1=3.36994, DF1=0.00589451
Top (constant approx.) -> DK2=3.57756, DF2=0.00547152
Thickness (mil) -> td=4.65 ,1.19 ,2.38 ,3.85
--- Metal ---
Roughness index=[1 1 1 1 1]
Thickness (tm)=1.21 mil, Length=2 inch
Approx. impedance (Z)=89.7785 ohm
--- Generated files ---
DK, DF, sigma table -> MPX_L7_T5_WS1_Z90_T1234.s4p_DUT.s4p_fit.csv
Fitted S-param file -> MPX_L7_T5_WS1_Z90_T1234.s4p_DUT.s4p_fit.s4p
Scalable X2D2 file -> MPX_L7_T5_WS1_Z90_T1234.s4p_DUT.s4p_fit.tp2

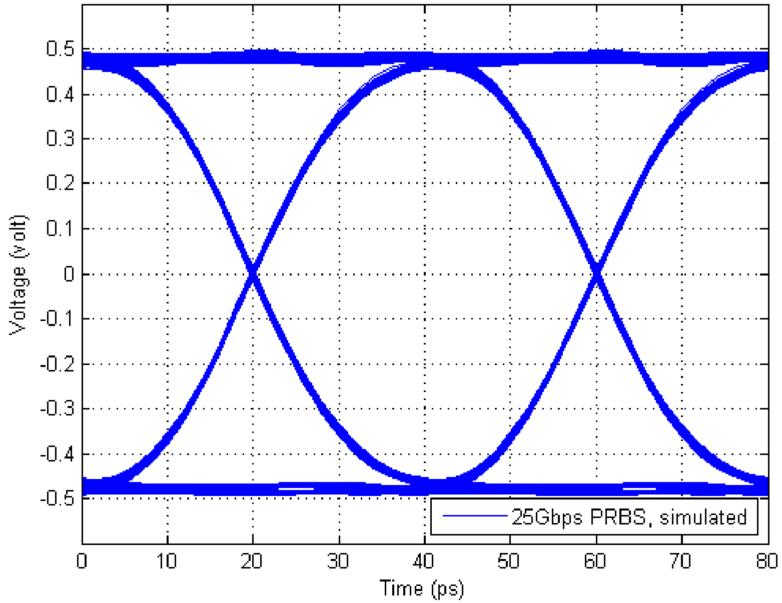
(참고) EYE diagram 비교 : 25Gbps, PRBS

From measured S-parameter



----- Outputs -----
>>> Deterministic:
*** Threshold voltage = 0 volt
Eye height = 0.911855 volt
Eye width = 39.2379 ps
Jitter = 0.762092 ps

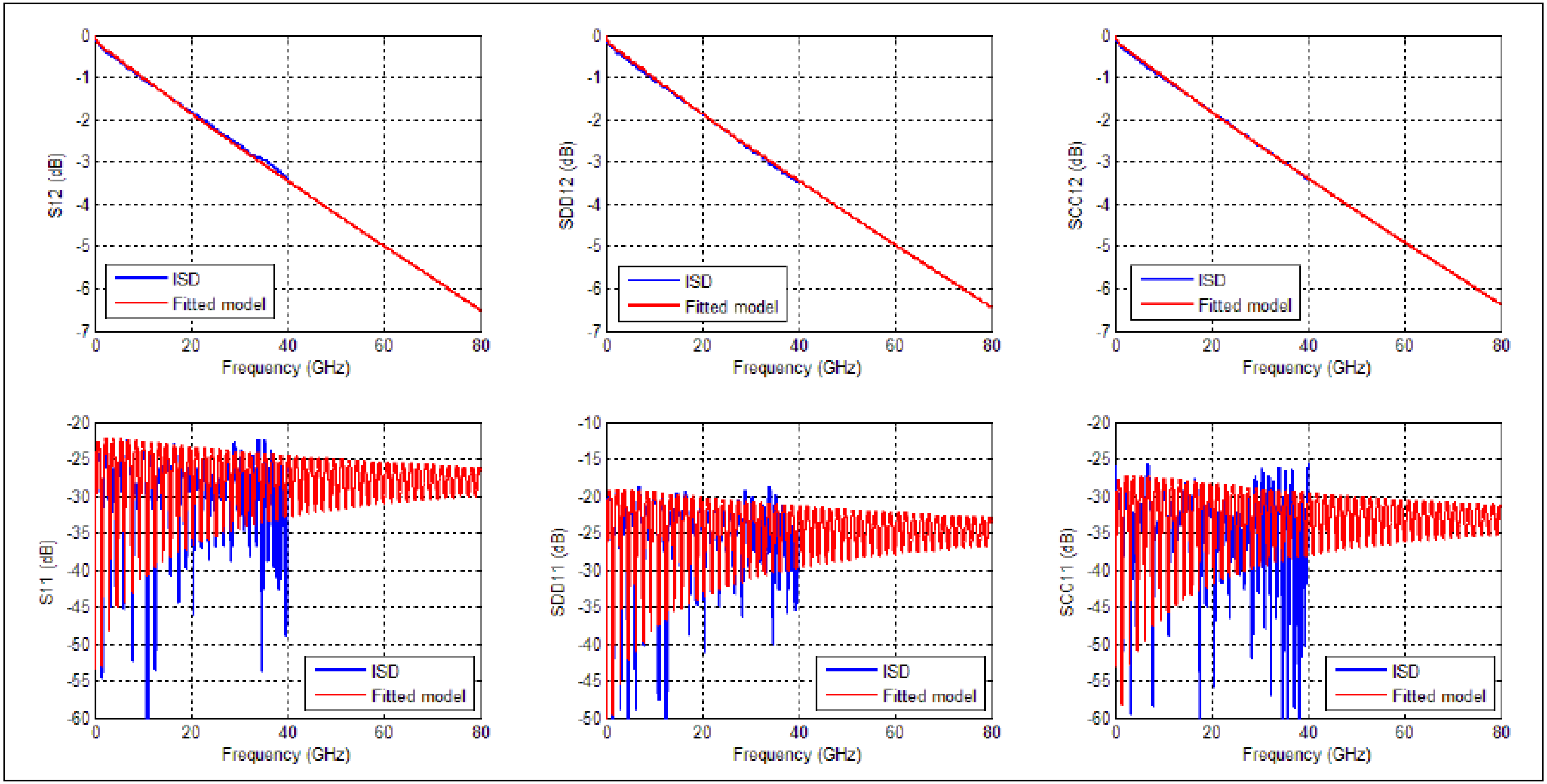
From simulated S-parameter



----- Outputs -----
>>> Deterministic:
*** Threshold voltage = 0 volt
Eye height = 0.914876 volt
Eye width = 39.3227 ps
Jitter = 0.677314 ps

이후 프로젝트에서 정확한 시뮬레이션에 활용 예

추출한 Material properties 셋업 파일로, 주파수나 길이를 변경하여 정확한 S-parameter를 얻을 수 있다.

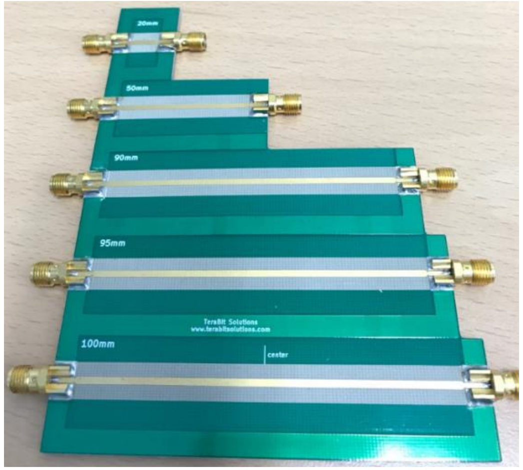


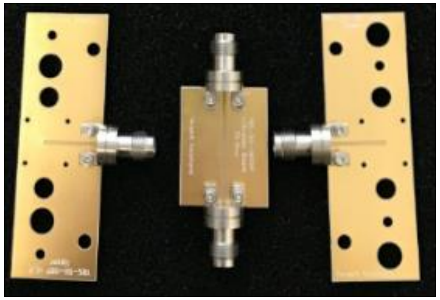
최대의 성능을 확보하는,
PCB와 RF Connector 연결 디자인

Measurement: up to 67GHz

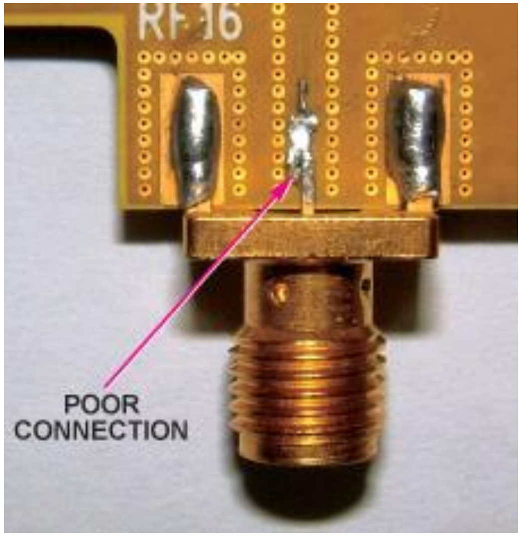
Edge Mount RF connectors

- ✓ **Chip test Board**
- ✓ **PCB Material Property test**
- ✓ **Socket, Connectors, cables test**
- ✓ **Etc.**

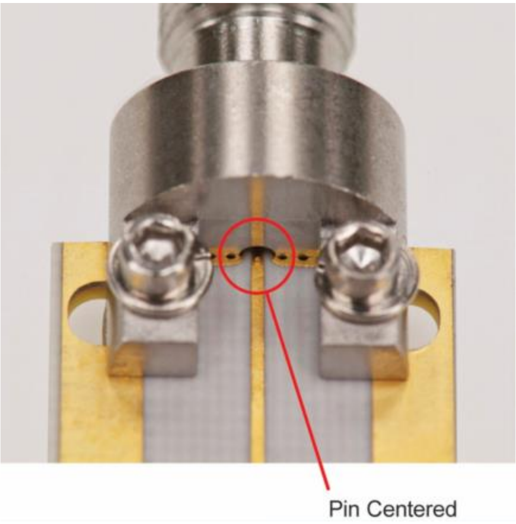




Solder type과 Solderless type RF connector

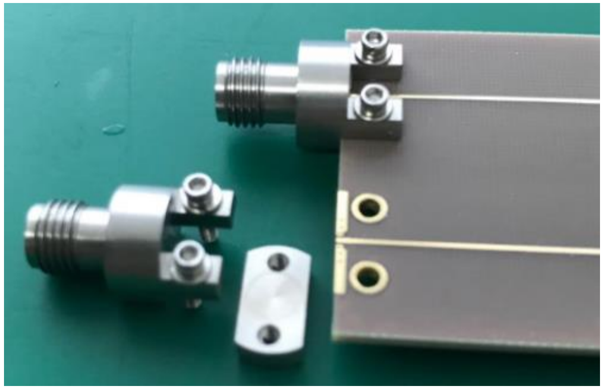


- ✓ PCB에 고정시 signal 핀(및 Body)을 solder로 연결
- ✓ 통상 18GHz이하에서 사용 (SMA)
- ✓ Soldering 품질이 S-parameter에 큰 영향을 줌
- ✓ 낮은 가격



- ✓ PCB에 고정은 screw 사용. signal 핀은 No solder(Press fit)
- ✓ 통상 40GHz 이상에서 사용
  (2.92mm, 2.4mm, 1.85mm, 1mm 등)
- ✓ Soldering이 없으므로 안정적인 S-parameter 확보
- ✓ 상대적 고가
- ✓ 재사용 가능

새로운 type의 고대역 Edge Mount 커넥터

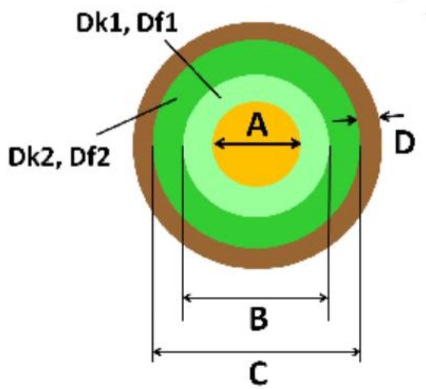


- ✓ 단순한 구조로 쉬운 사용:
  Connector Body, Bottom clamp, screws
- ✓ Solderless (press fit)
- ✓ 고대역, 고품질: 40GHz (2.92mm)
  67GHz (1.85mm)
  110GHz (1mm)
- ✓ 합리적인 가격
- ✓ 제조국: USA (Signal Microwave)

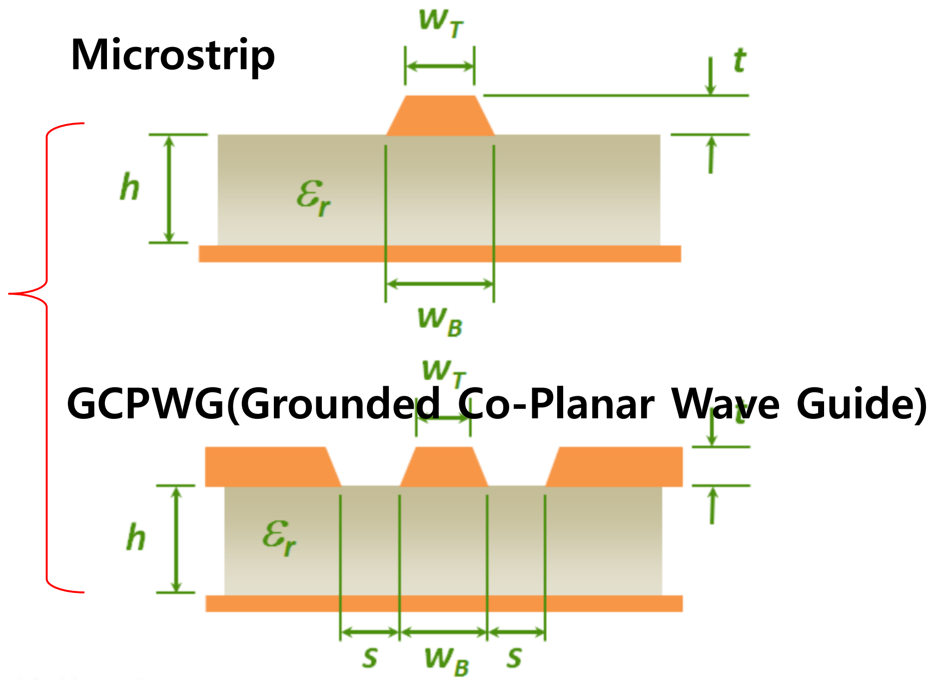
Narrow profile Standard profile

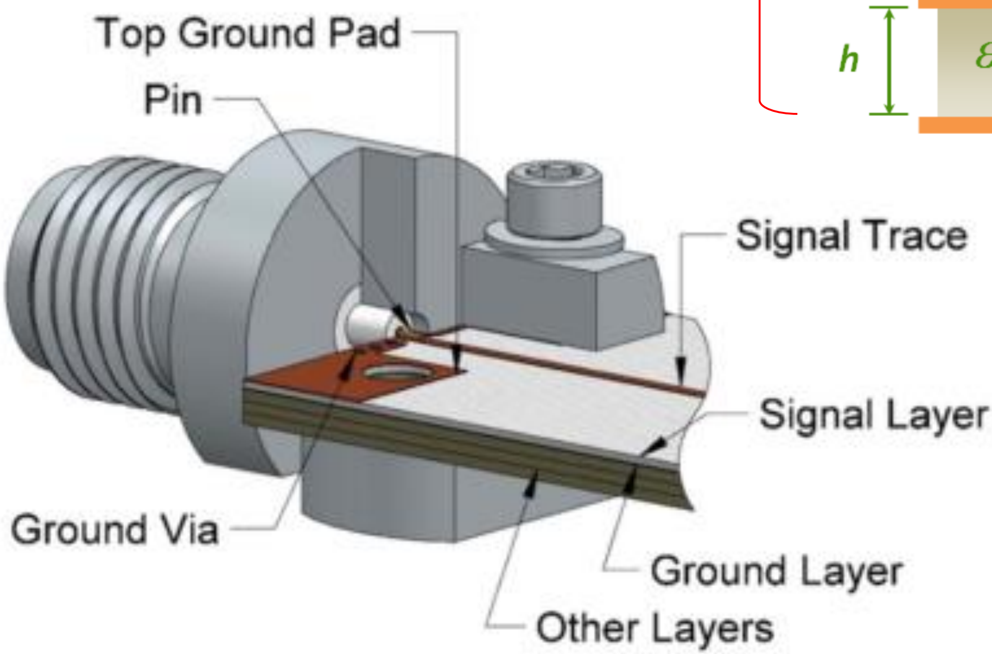
TeraBit Solutions Part Number:
TBS-EM-40-001/002
TBS-EM-67-001/002
TBS-EM-110-001/002

Transmission Line 관점에서 다른 구조의 결합



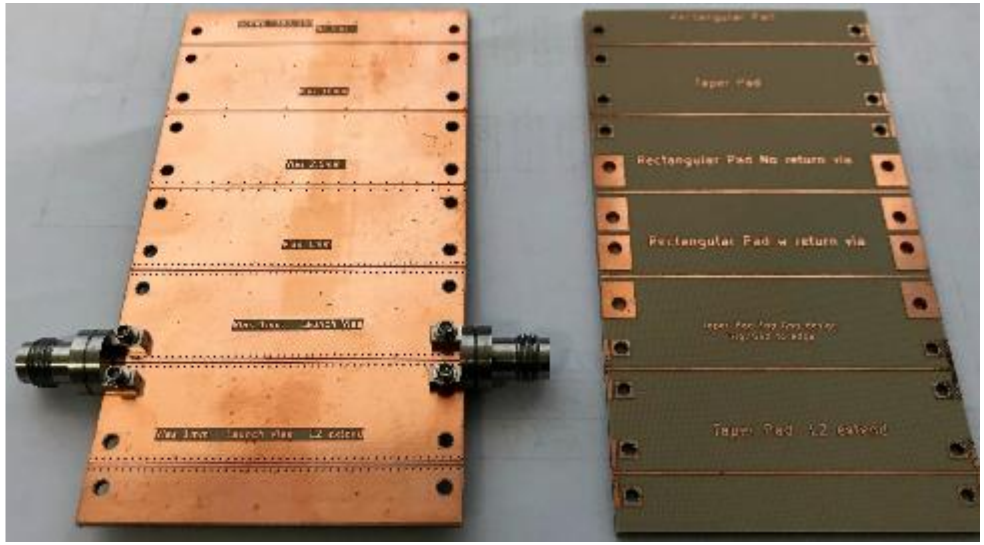
+





- ✓ Signal/Return Path 변화
- ✓ H/E Field의 변화
- ✓ Mode Resonance 주의

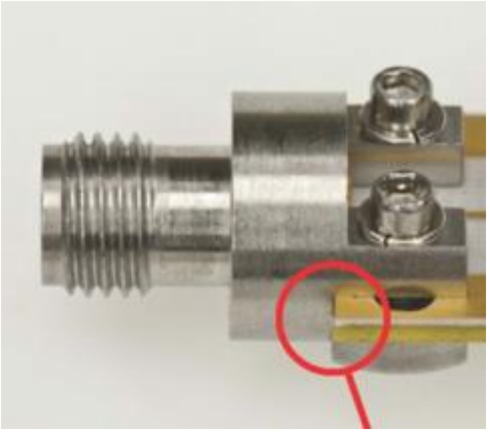
Test Board

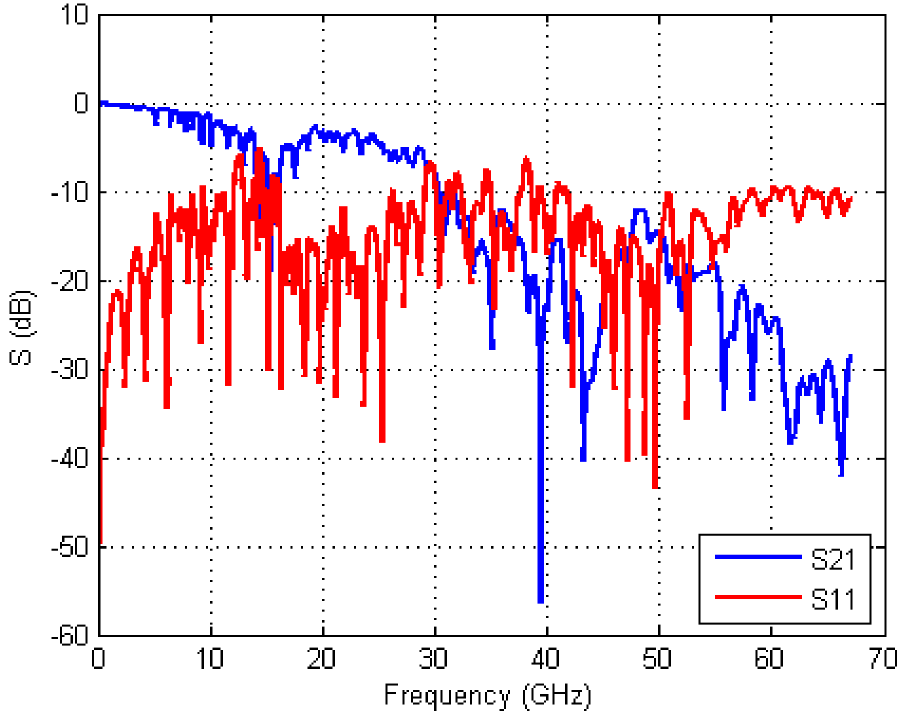


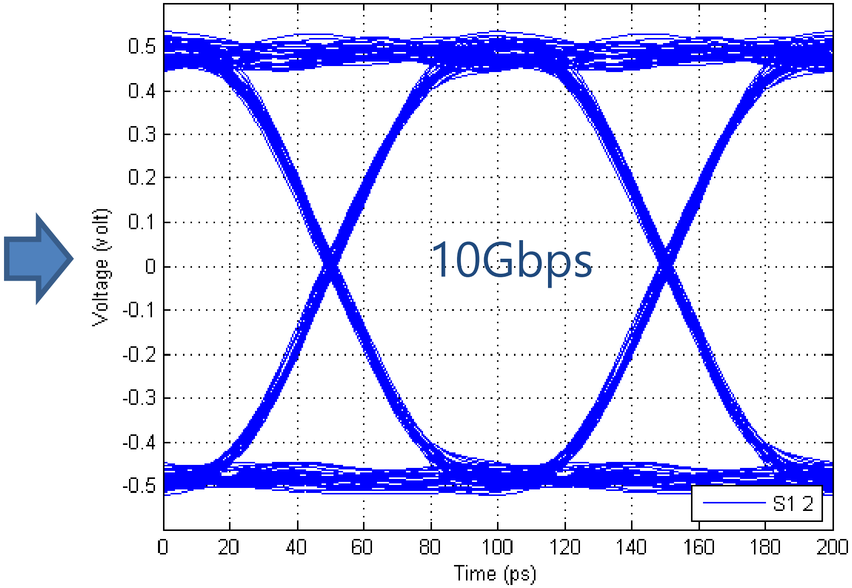
- ✓ **Board: ISOLA I-Tera MT40**
- ✓ **Structure: GCPWG / MS 2inch, appx 50ohm ±5%**
- ✓ **No surface finish(Cu plating)**
- ✓ **Edge Mount Connector: TBS-EM67-001**

- ✓ **Measurement Frequency: ~67GHz**

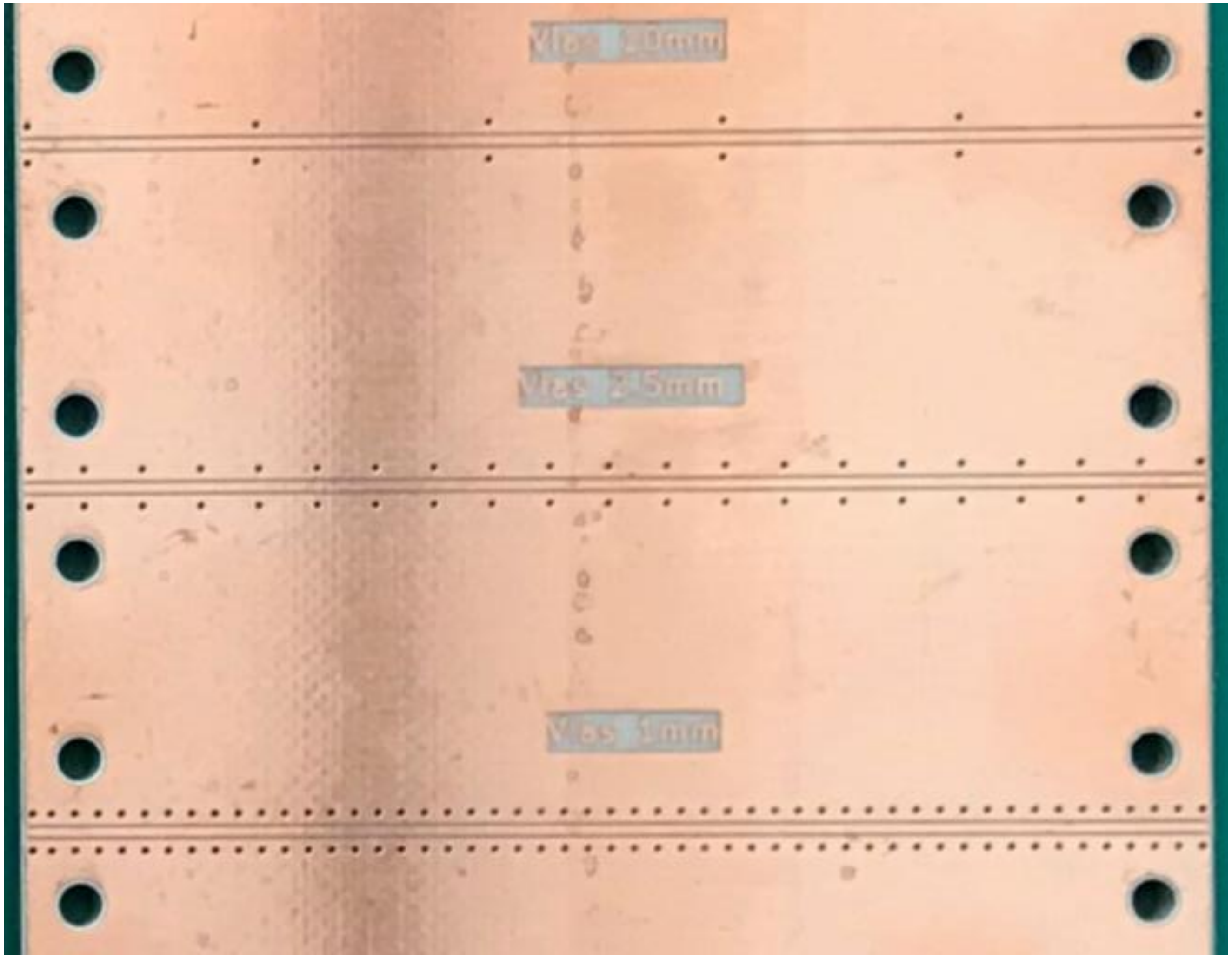
Case 1: GCPWG_No stiching Vias besides signal T



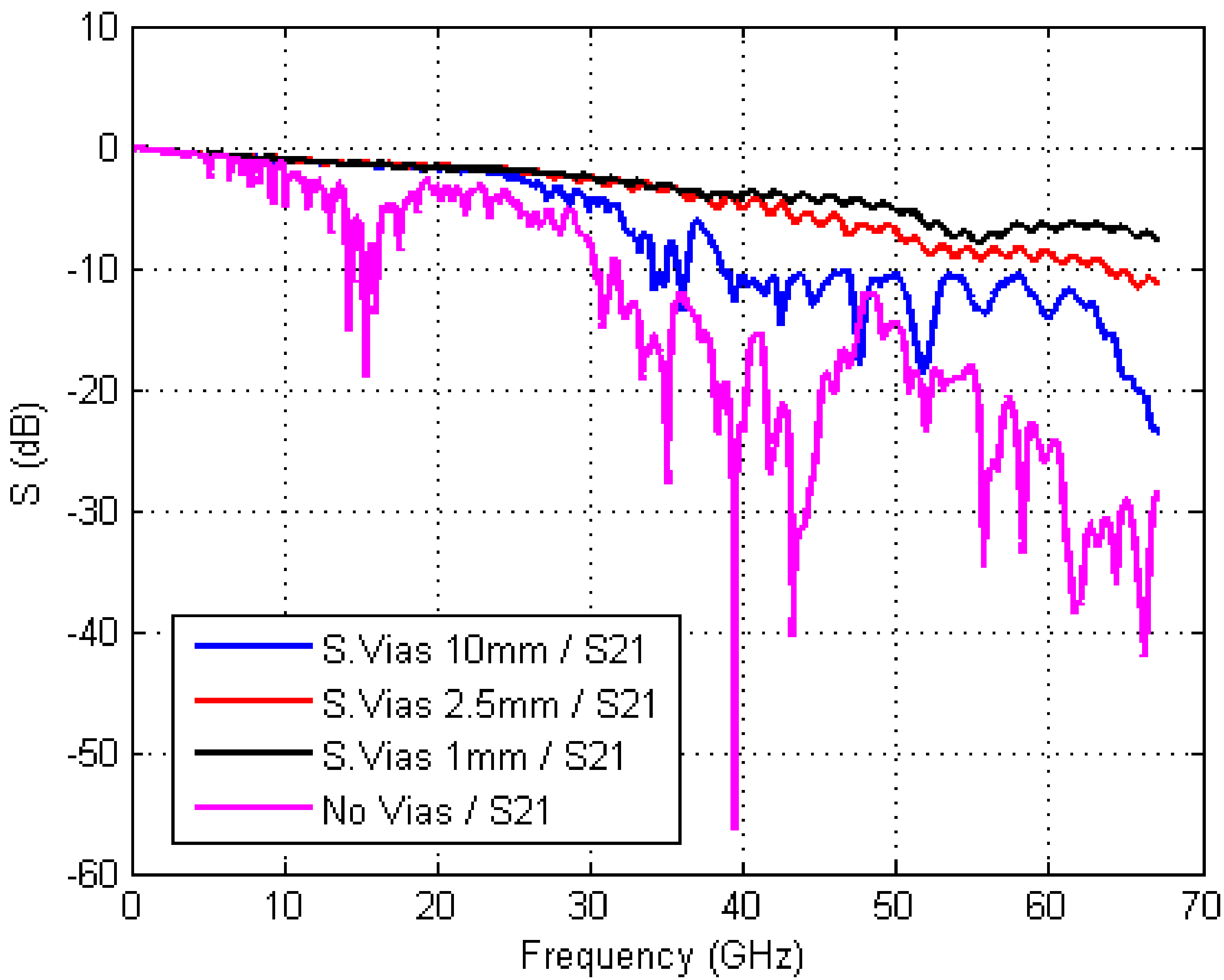




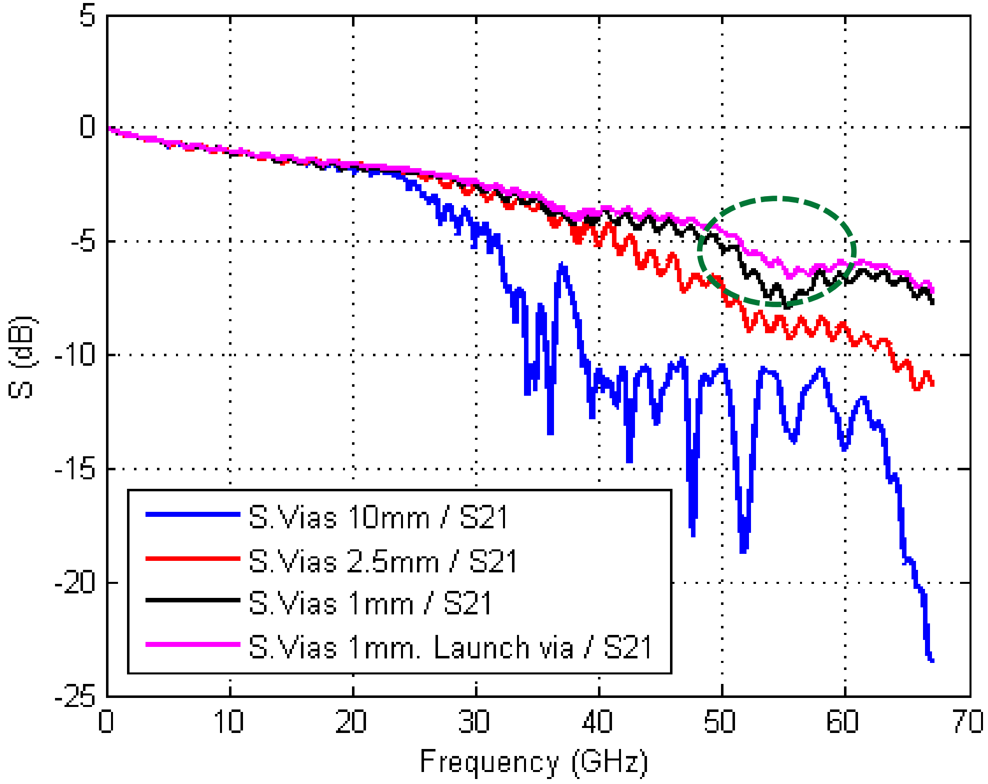
Case 2: GCPWG_stiching Vias: 10mm, 2.5mm, 1mm

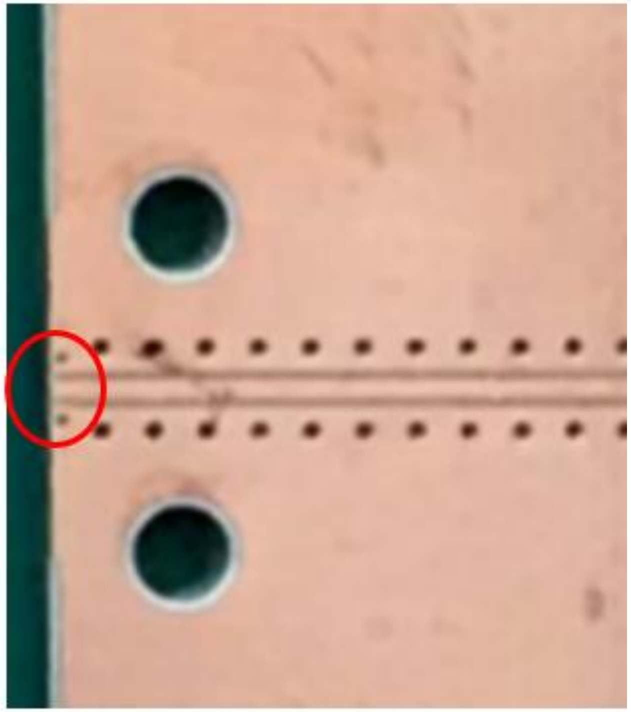


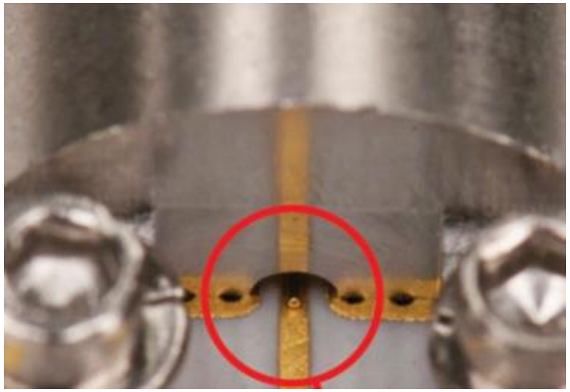
Case 2: GCPWG_stiching Vias: 10mm, 2.5mm, 1mm



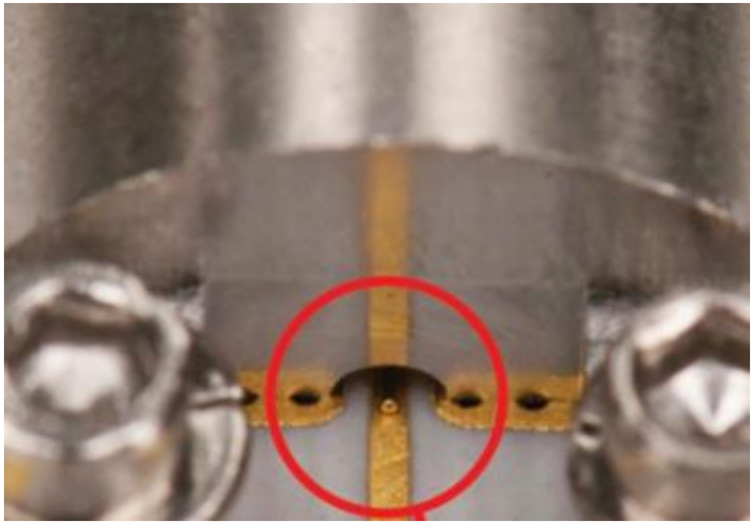
Case 3: GCPWG_stiching Vias: 1mm w/Launch via

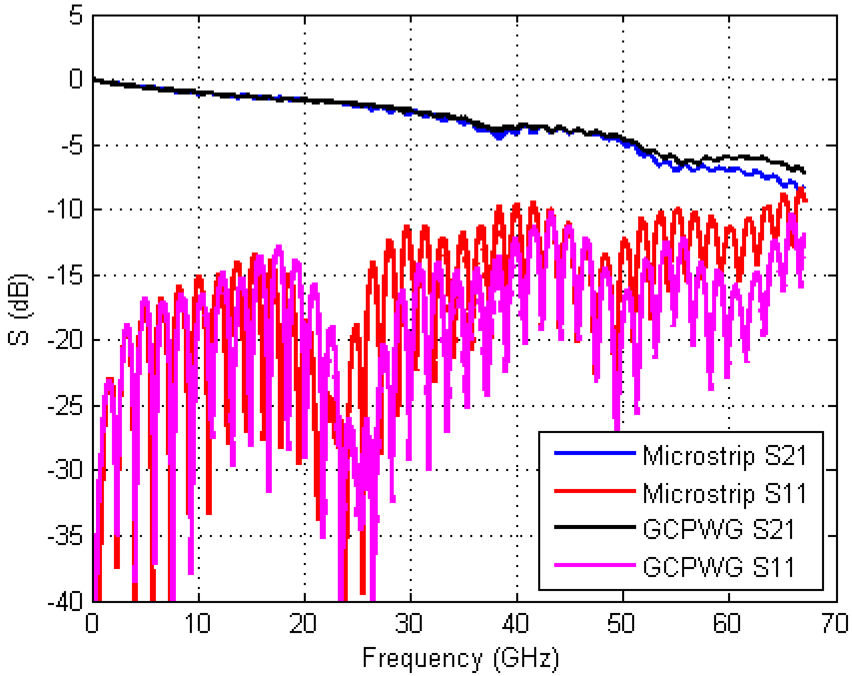




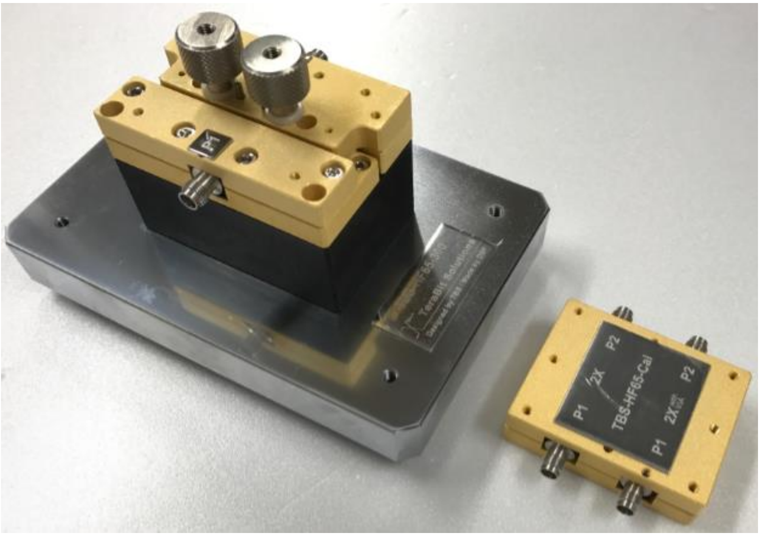


Case 4: Micro Strip_Launch Vias

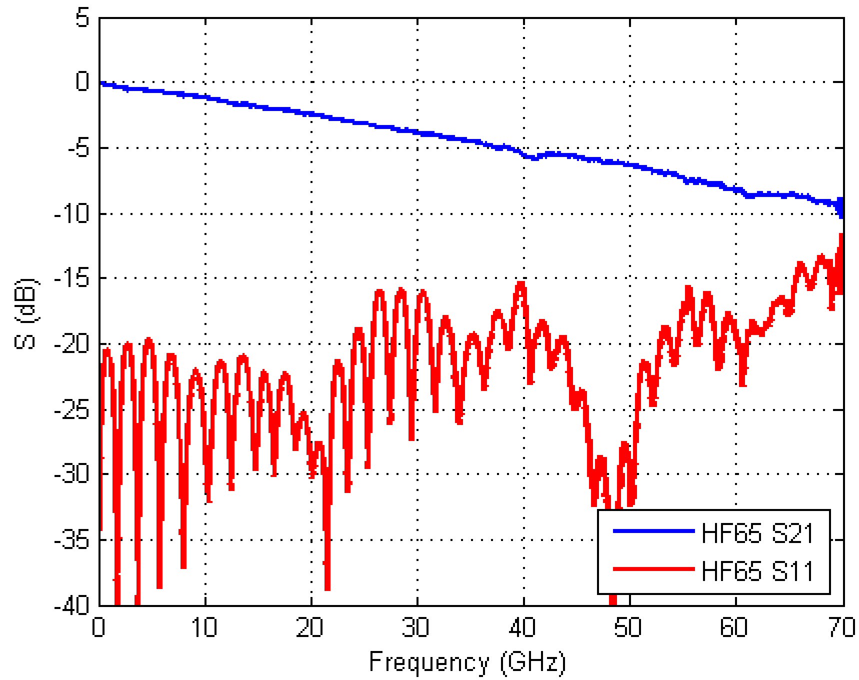




실제 제품에 적용한 성능 예



<Pin, socket Test fixture: TBS-HF65-xxx>



- ✓ **Board: ISOLA I-Tera MT40**
- ✓ **Structure: GCPWG, 2X thru Length ~2inch**
- ✓ **ENIG surface finish(No PSR)**
- ✓ **Edge Mount Connector: TBS-EM67-001**

- ✓ **Measurement Frequency: ~70GHz**

사용한 소프트웨어: ISD, X2D2, ADK, MPX,
(Ataitec, USA)

사용한 RF Connector: TBS-EMxx-xxx
(Signal Microwave, USA)

문의: sales@terabs.com
010-7459-0902

감사합니다!