Optimizing Precision Signal Chain Performance

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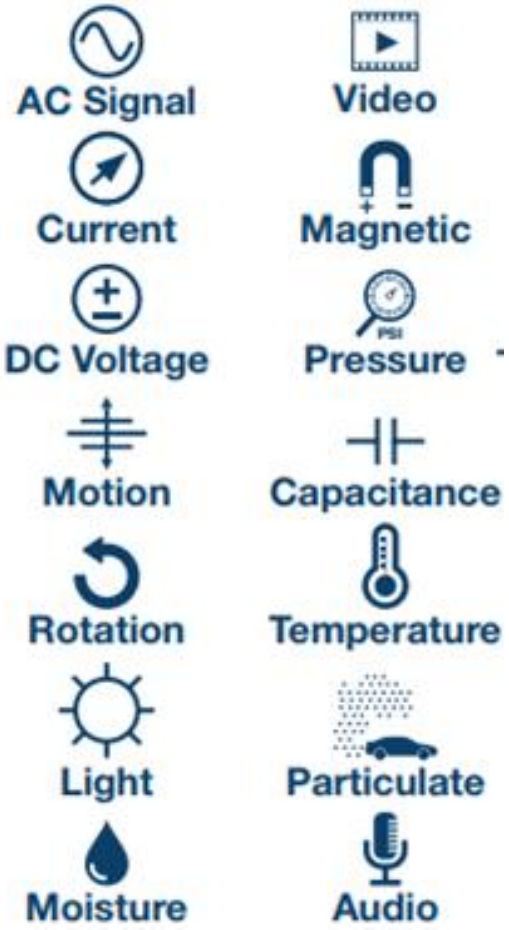
AHEAD OF WHAT'S POSSIBLE™

Signal Acquisition Challenges

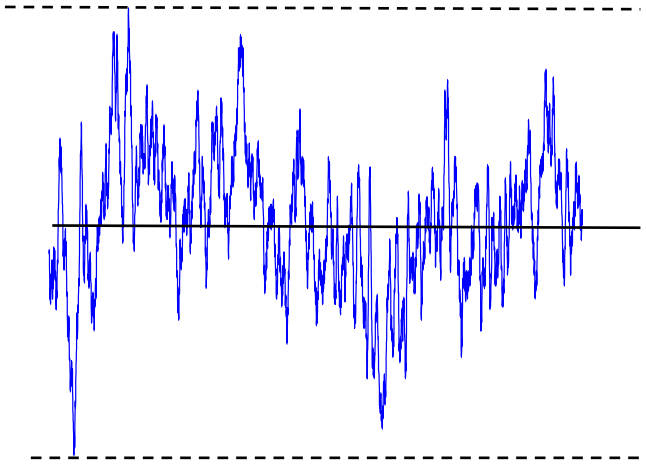


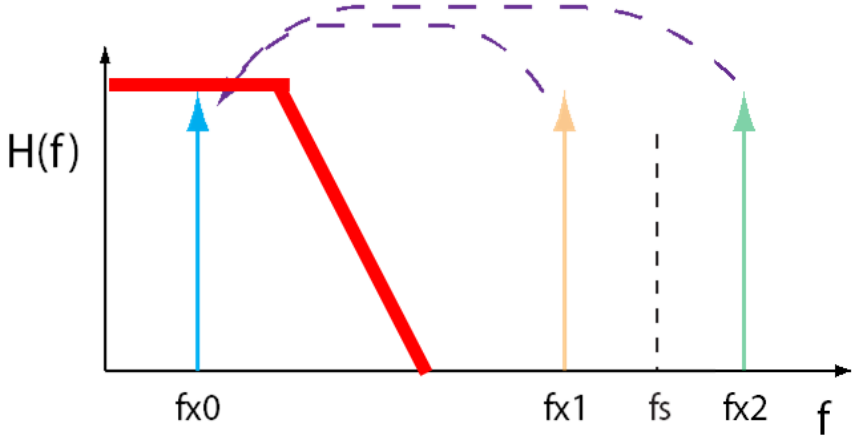
- Wide range of signals (µV to V)
- Various bandwidths (DC to MHz)
- Various impedances (Ω to MΩ)

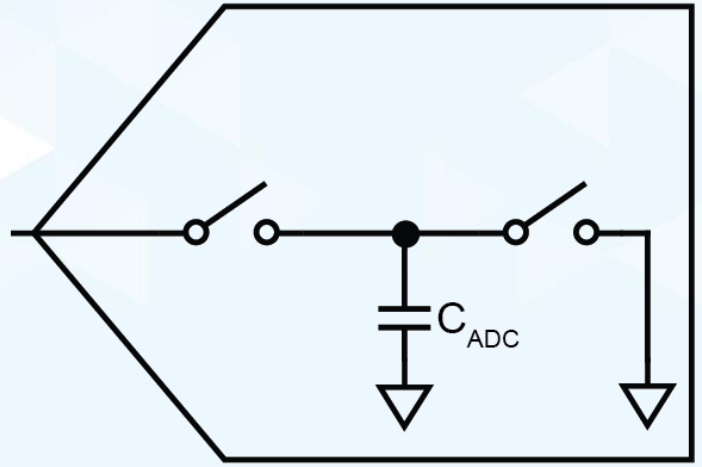
- Noise / Resolution
- Signal Chain Bandwidth
- System Settling Dynamics

Agenda

- Noise optimization
- Anti-aliasing filter design
- ADC driving







Noise / Resolution

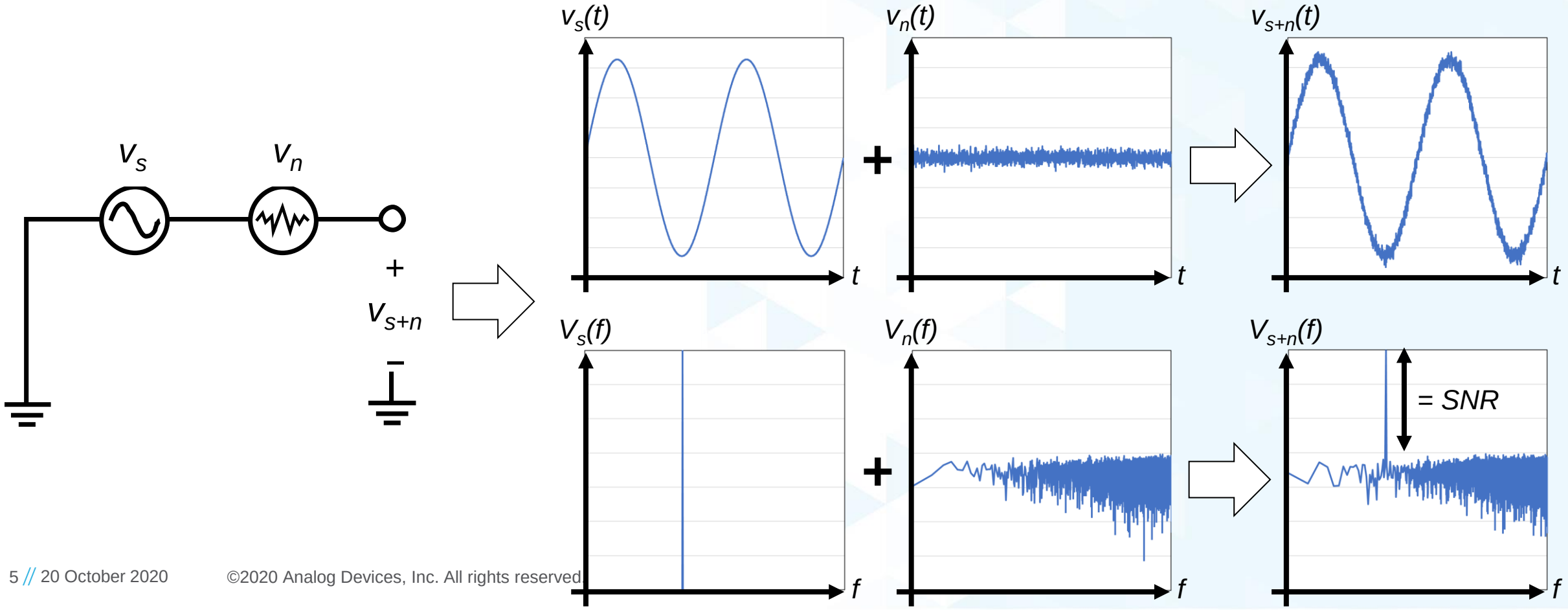
Signal Chain Bandwidth

System Settling Dynamics

Cutting Through the Noise

What is Noise and Why Do We Care?

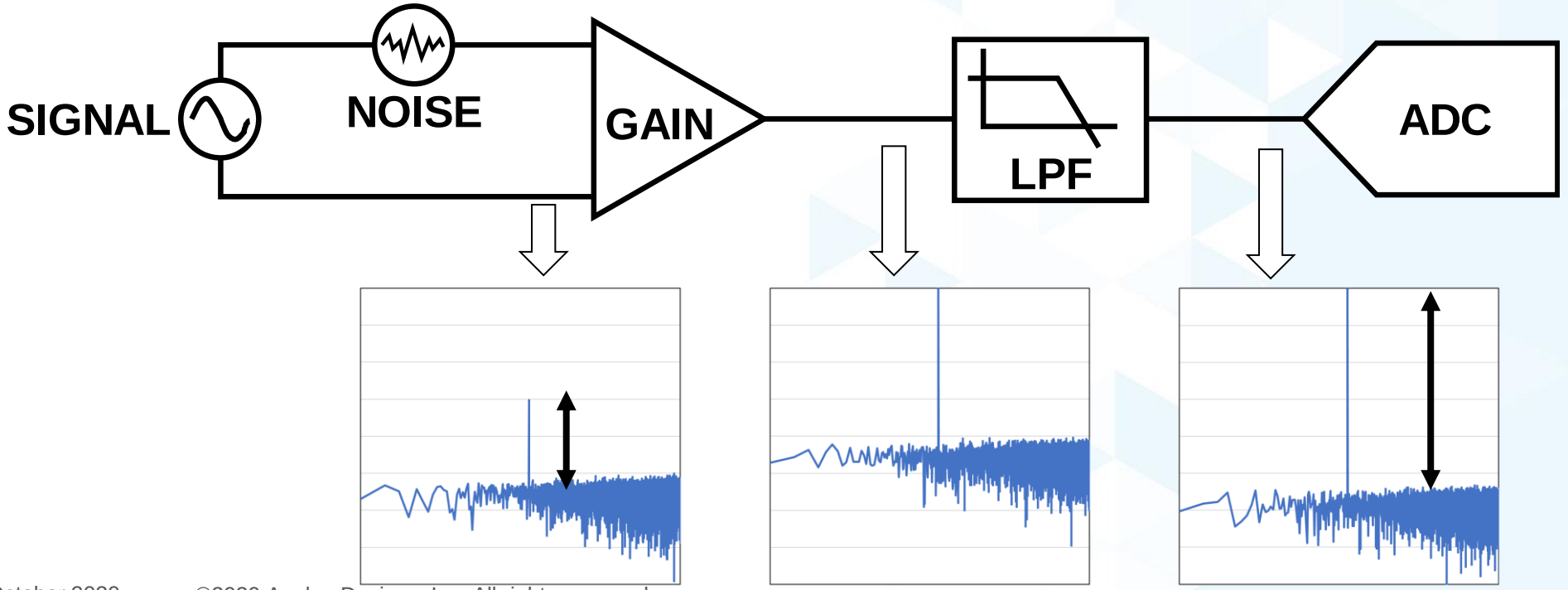
- Variations in a signal with inherently random and unpredictable amplitudes
- Noise fundamentally limits the certainty of precision measurements
- Signal-to-Noise Ratio (SNR): measure of desired signal versus noise signal



System Noise vs. SNR

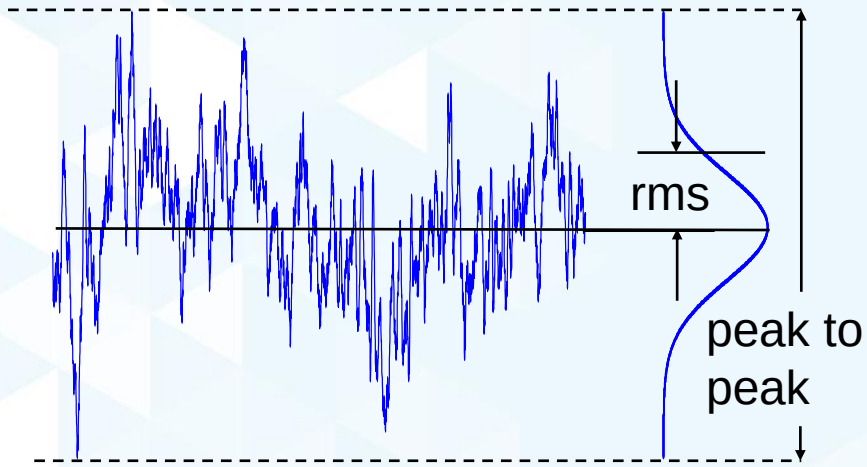
- To maximize system SNR:
  - Maximize *signal*
    - Add gain to increase the amplitude of the signal
    - This can amplify the noise, but there are ways around this
  - Minimize *noise*
    - Select low-noise components to build the signal chain
    - Add filtering to reject noise from out-of-band

$$SNR(dB) = 20\log\left(\frac{Signal\ (V_{RMS})}{Noise\ (V_{RMS})}\right)$$

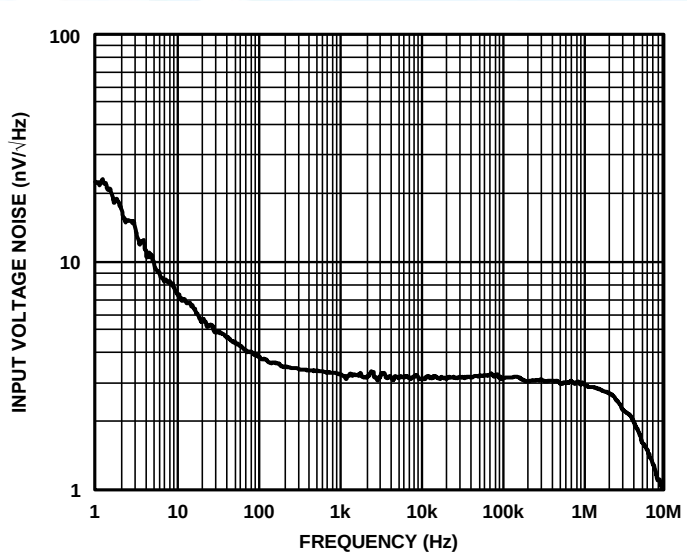


Quantifying Noise

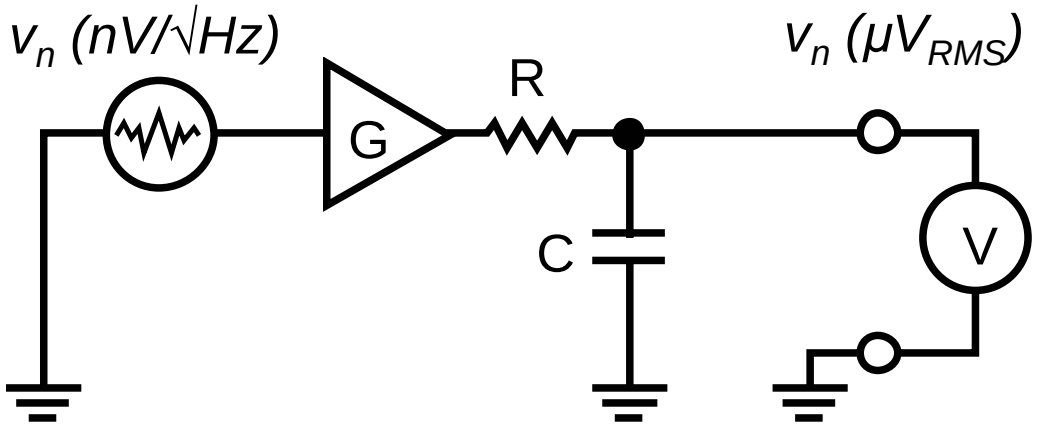
- **Peak-to-peak noise** (μV_{p-p})
  - Time dependent
  - Not repeatable, predictable
- **RMS Noise** (μV_{rms})
  - Normalized over any time interval
  - Related to noise power
    - Repeatable and predictable
- **Noise Spectral Density (NSD)** (nV/√Hz)
  - Relative noise power over specified frequency bands
    - Predicts RMS noise vs. filter bandwidths
  - Noise power is related to integration of NSD
    - Somewhat more complex maths



Example Noise Waveform

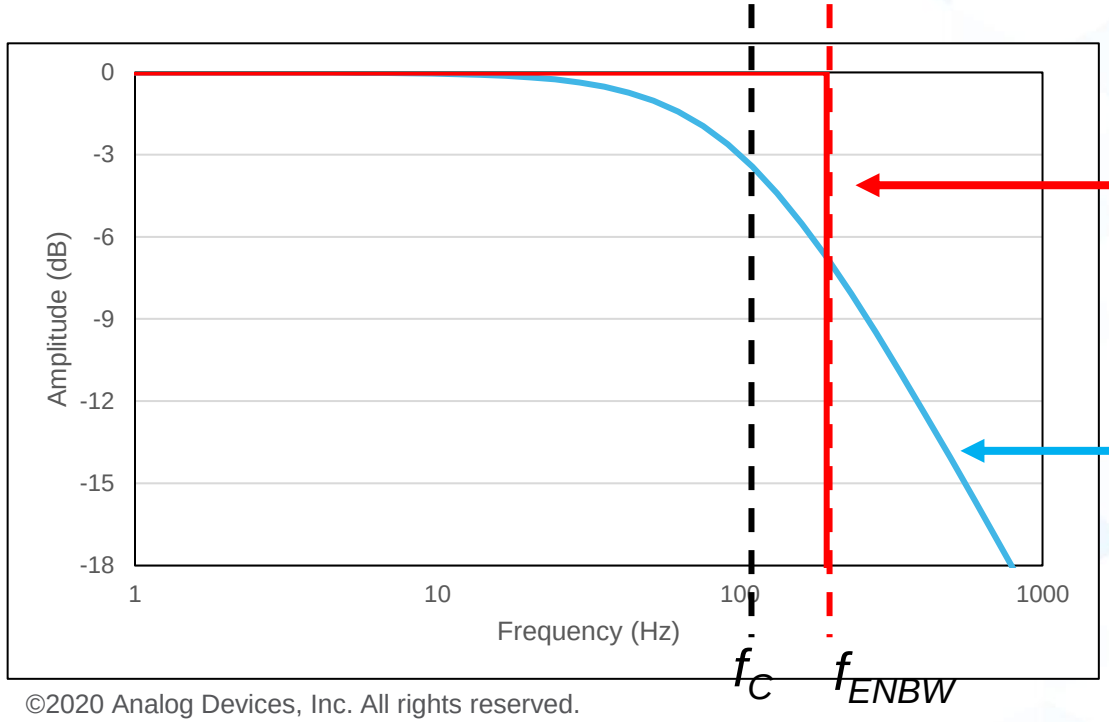


Converting NSD to RMS Noise



$$RMS\ Noise(V_{RMS}) = NSD\left(\frac{V}{\sqrt{Hz}}\right) \times G \times \sqrt{f_{ENBW}\ (Hz)}$$

$$(f_{ENBW} = K \times f_C) \Rightarrow (f_{ENBW} = \frac{\pi}{2} \times f_C)$$



Equivalent brickwall filter response

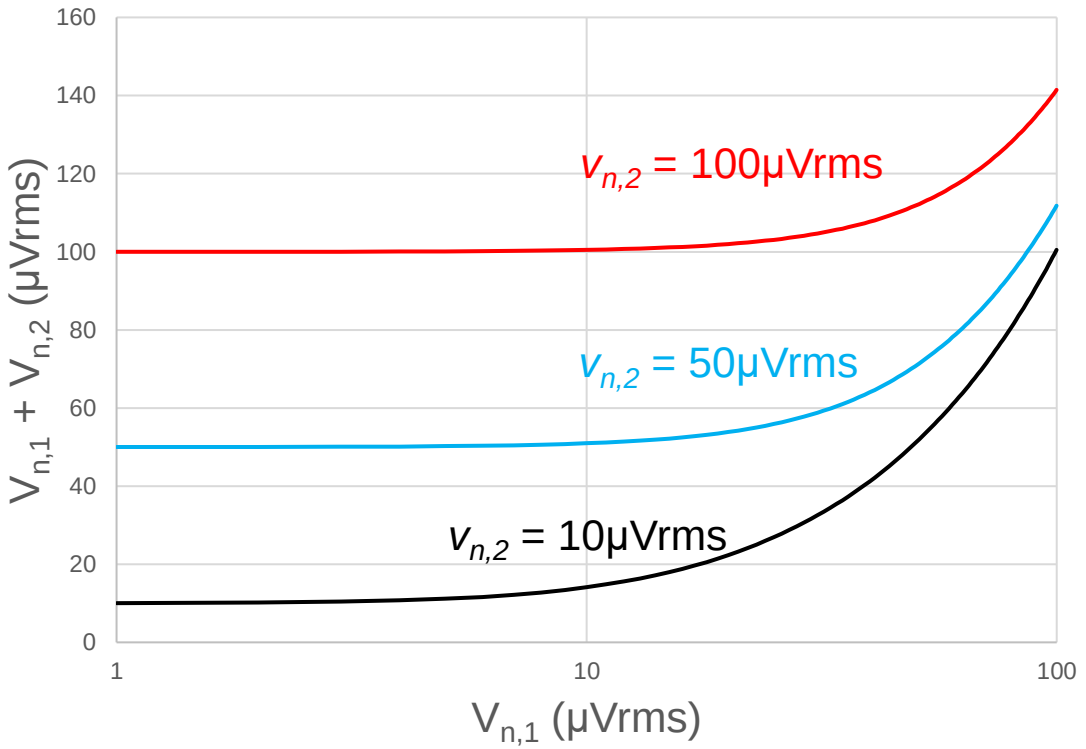
Real filter response (single-pole RC)

Combining Noise Sources

- Noise voltage *does not* sum linearly: 2 µVrms + 2 µVrms ≠ 4 µVrms
- Total RMS noise is the root sum of squares of the constituent noise sources:

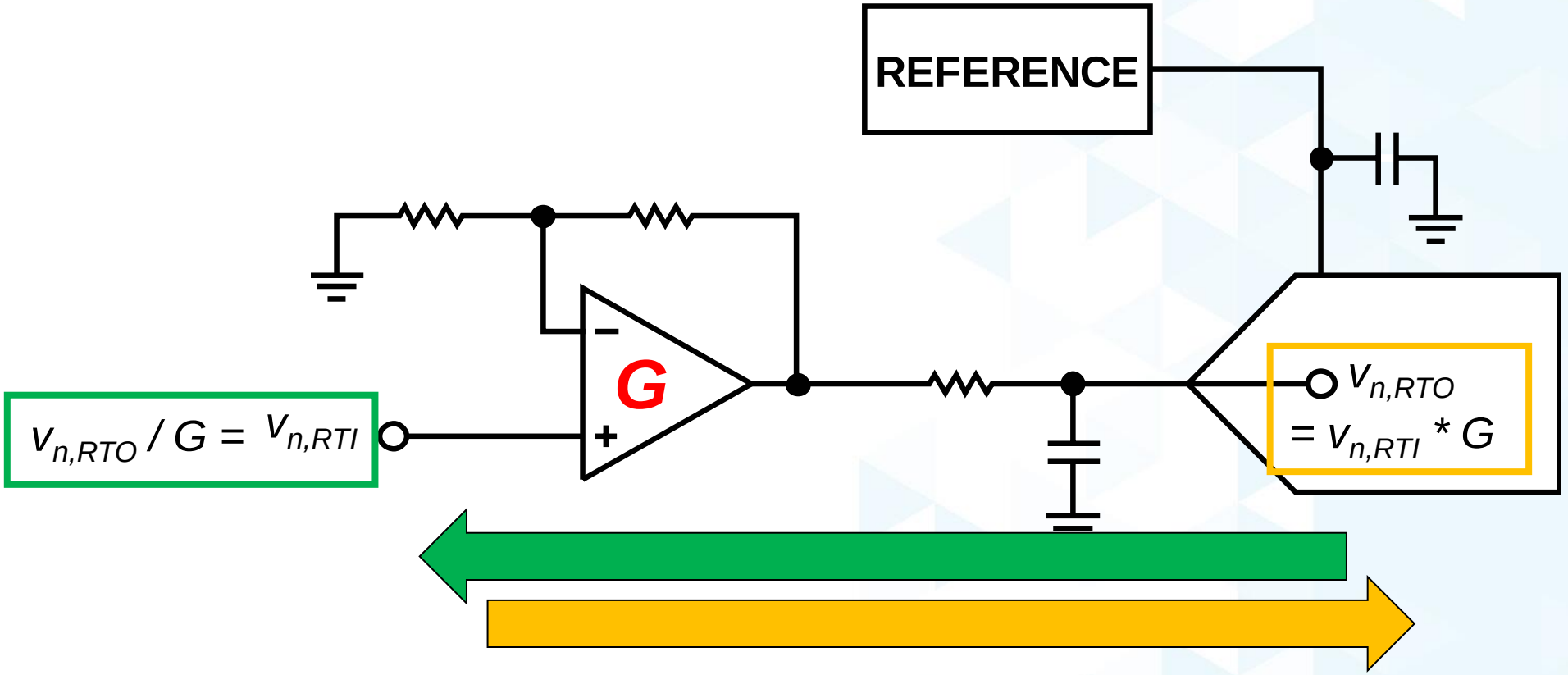
$$V_{n,total} = \sqrt{\left({V_{n,1}}^2 + {V_{n,2}}^2 + \cdots + {V_{n,N}}^2\right)}$$

- **System noise is dominated by the largest constituent noise source**
  - (50 µVrms)² + (5 µVrms)² = (50.25 µVrms)²
- **Goal is to make precision measurement system with fraction of transducer noise**



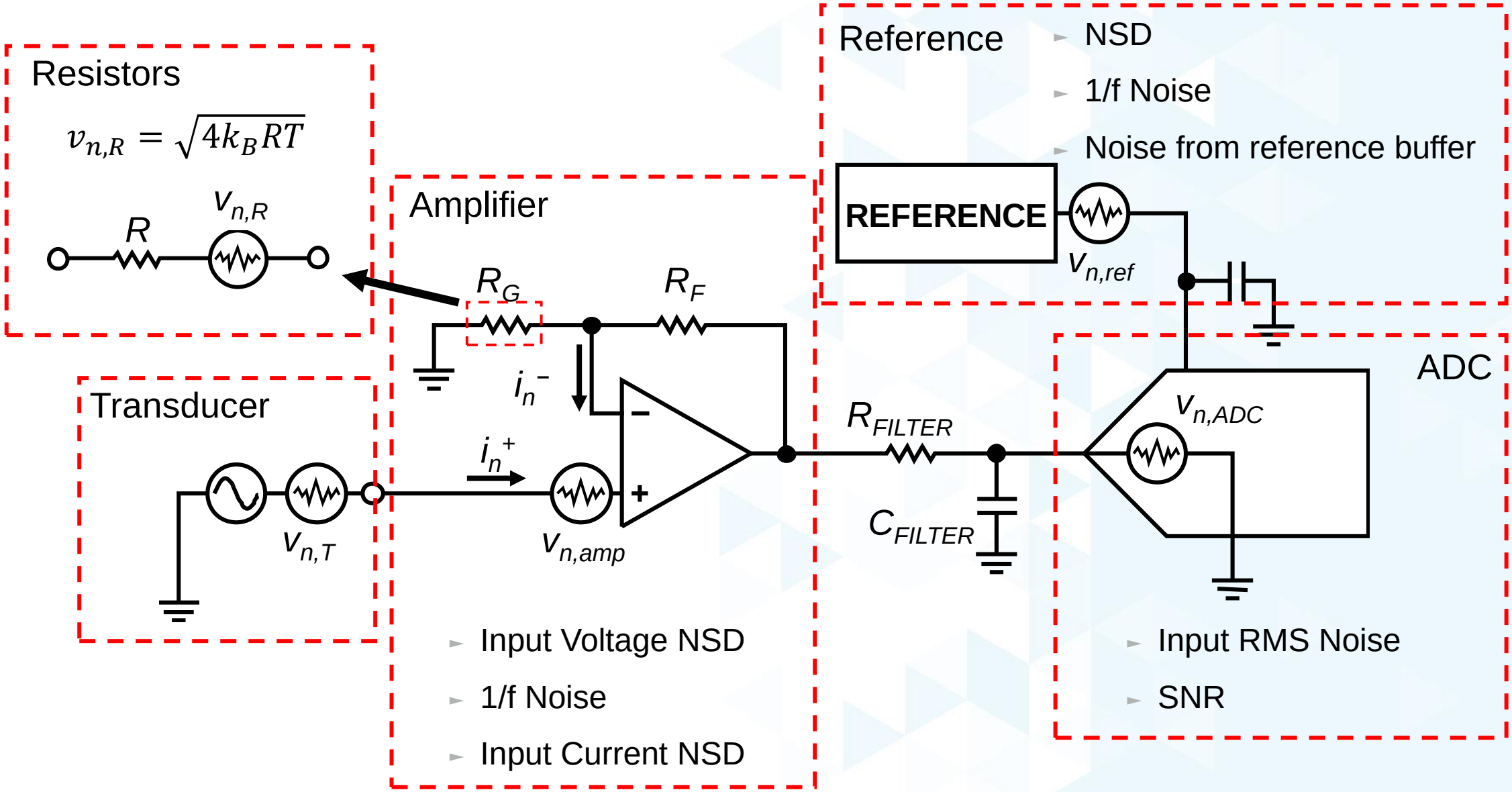
Determining System Noise – Tips

- **Quantify all constituent noise sources with the same units (NSD or RMS)**
- **Quantify all constituent noise sources all at the same point (RTI or RTO)**

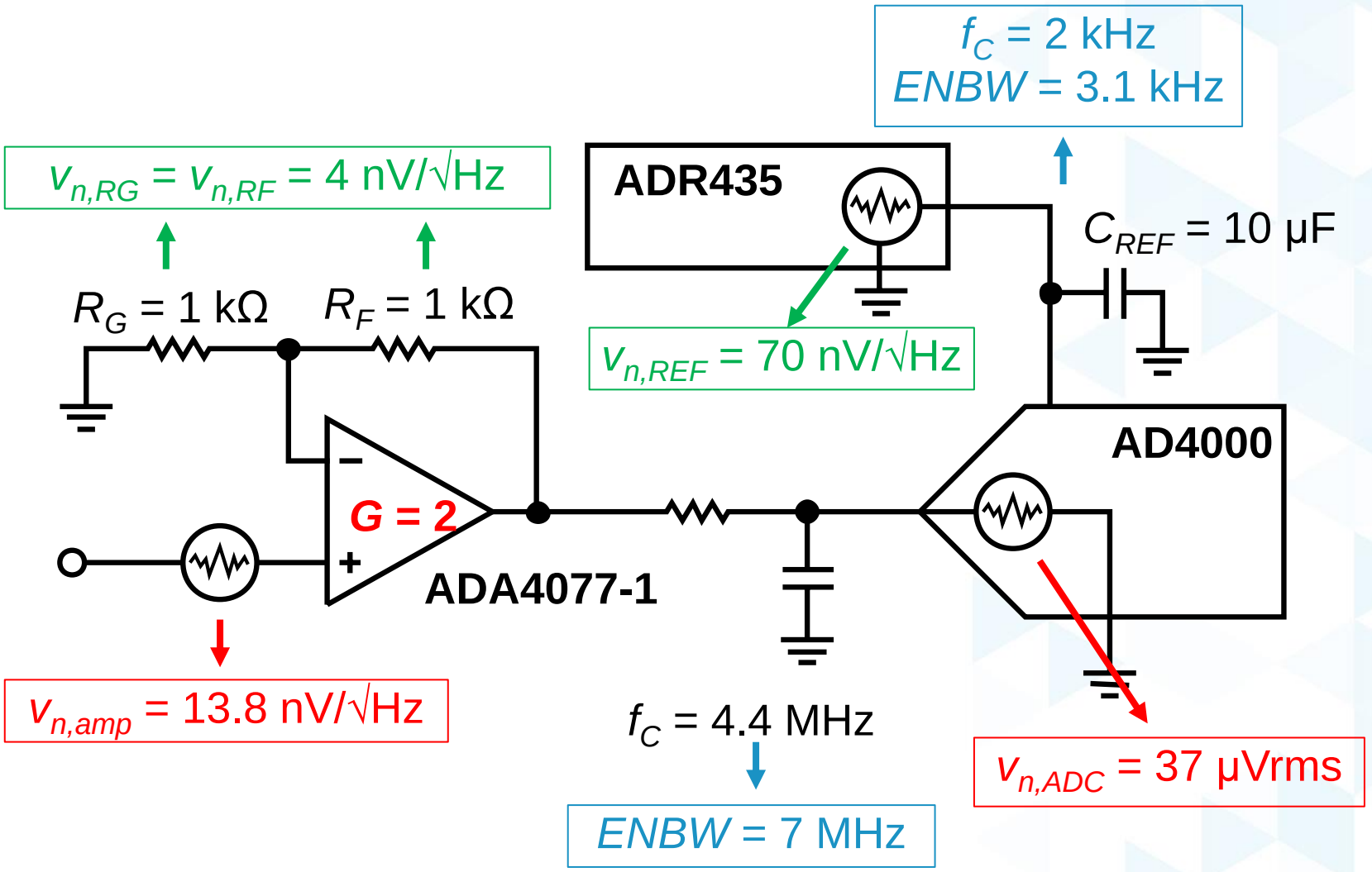


- Referred to Input (RTI):
  - Easy comparison with transducer noise
- Referred to Output (RTO):
  - Easy comparison of measurement systems

Signal Chain Noise Sources



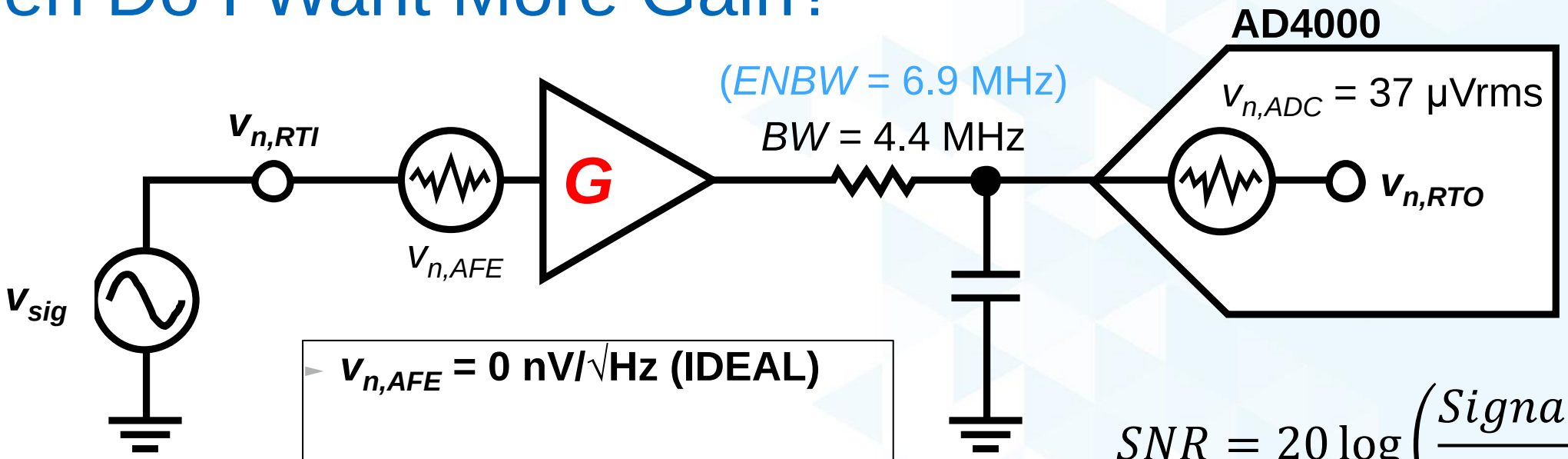
Example: Precision Signal Chain Noise Analysis



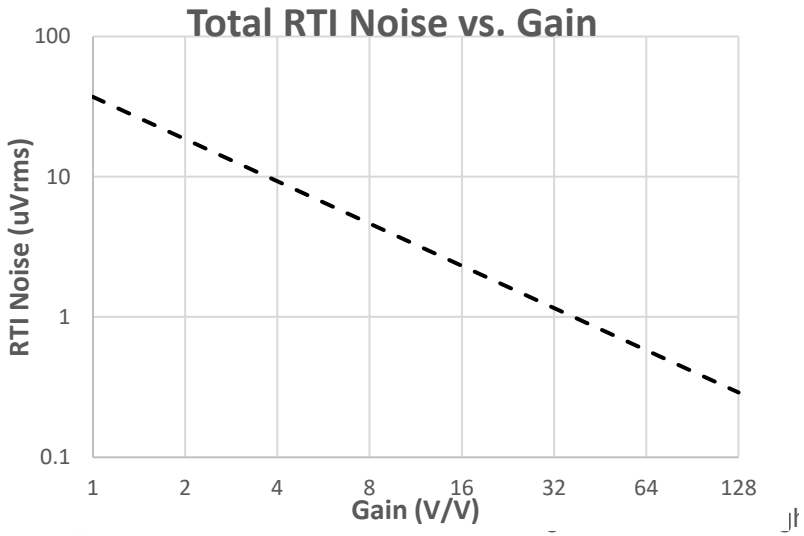
Component	RTO Noise (µVrms)
R_F	10.5
R_G	10.5
ADA4077-1	36.5
ADR435	3.9
AD4000	37
Total	**54.2**

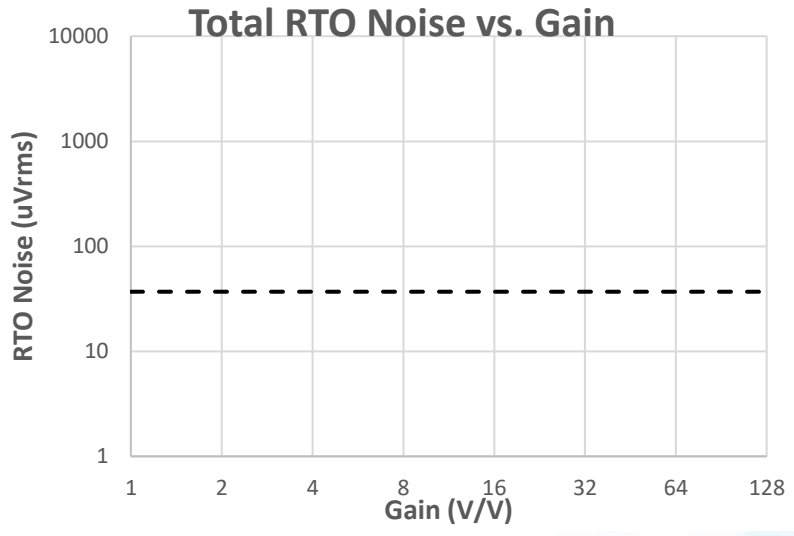
SNR = 90.3 dB

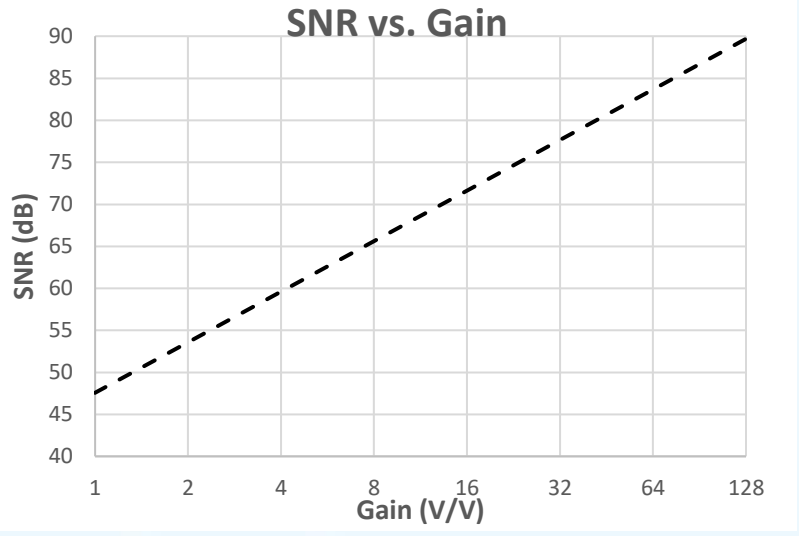
When Do I Want More Gain?



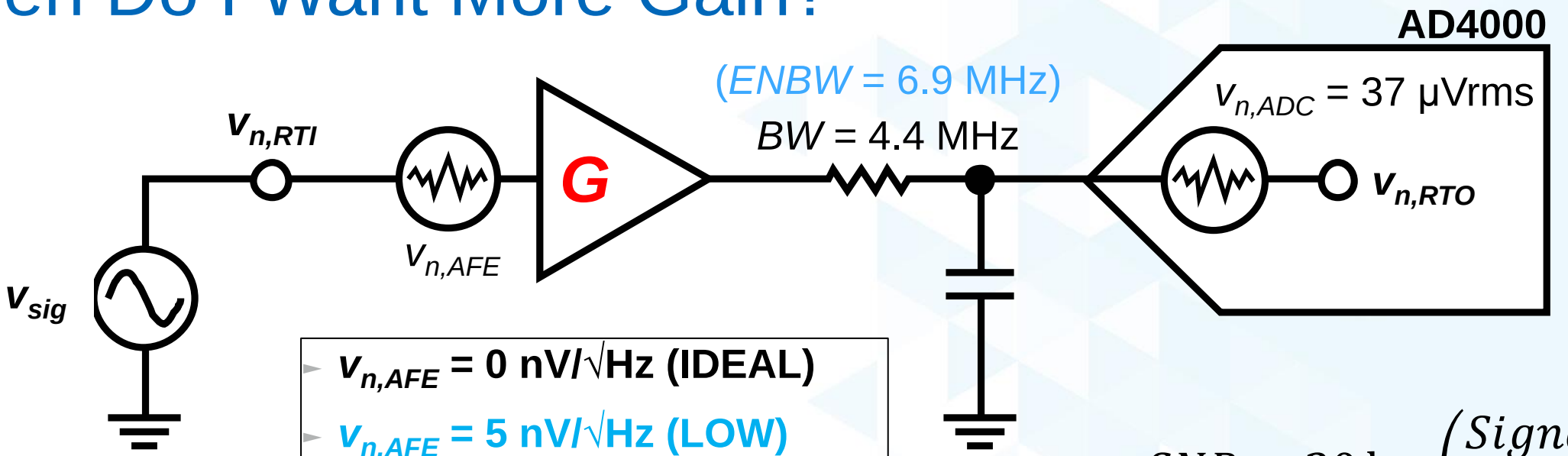
$$SNR = 20\log\left(\frac{Signal\ (rms)}{Noise\ (rms)}\right)$$





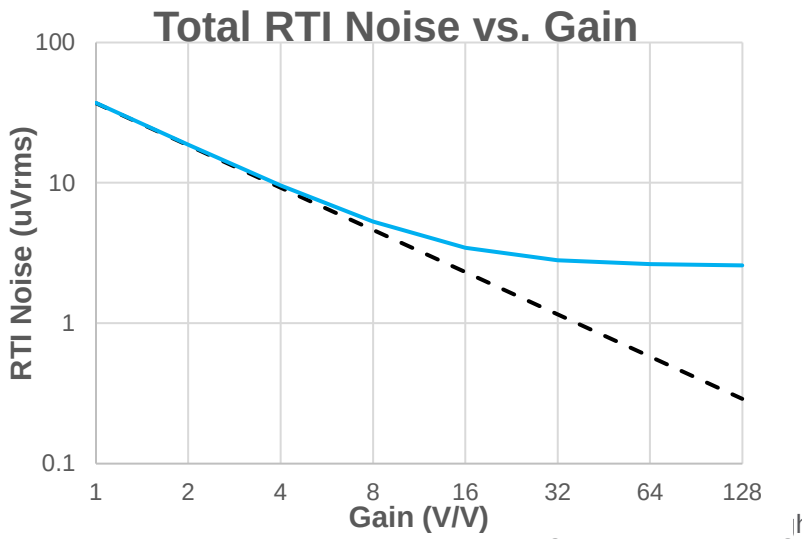


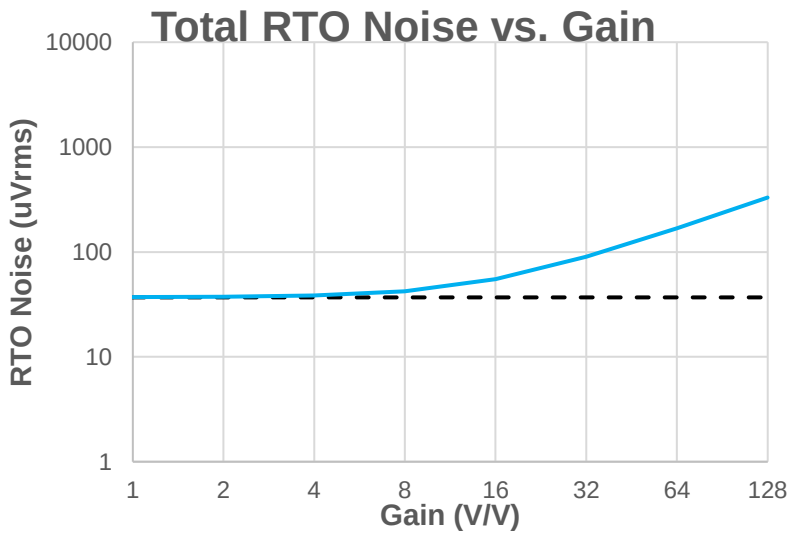
When Do I Want More Gain?

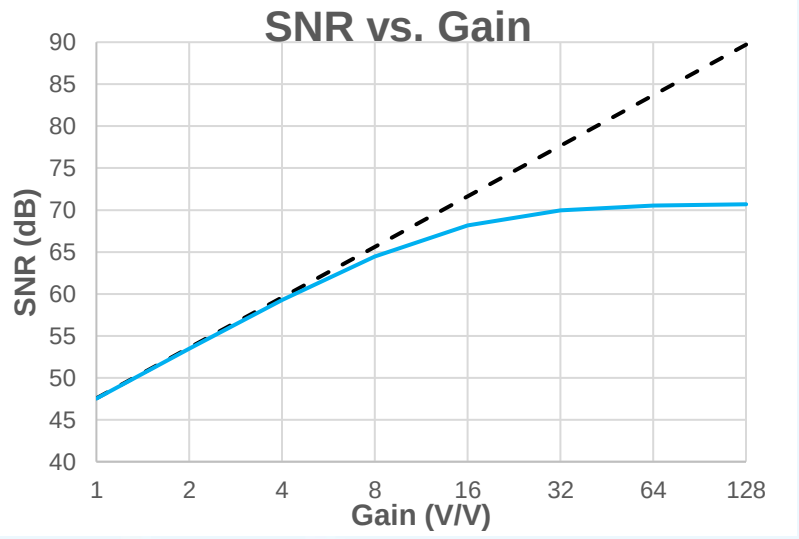


- $V_{n,AFE}$ = 0 nV/√Hz (IDEAL)
- $V_{n,AFE}$ = 5 nV/√Hz (LOW)

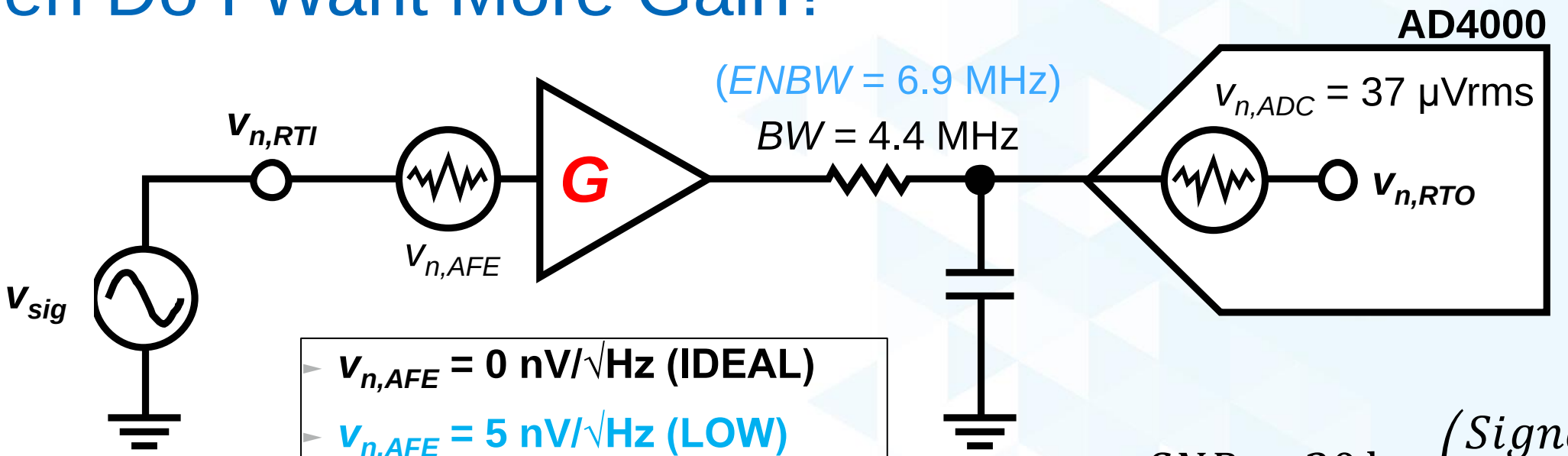
$$SNR = 20\log\left(\frac{Signal\ (rms)}{Noise\ (rms)}\right)$$





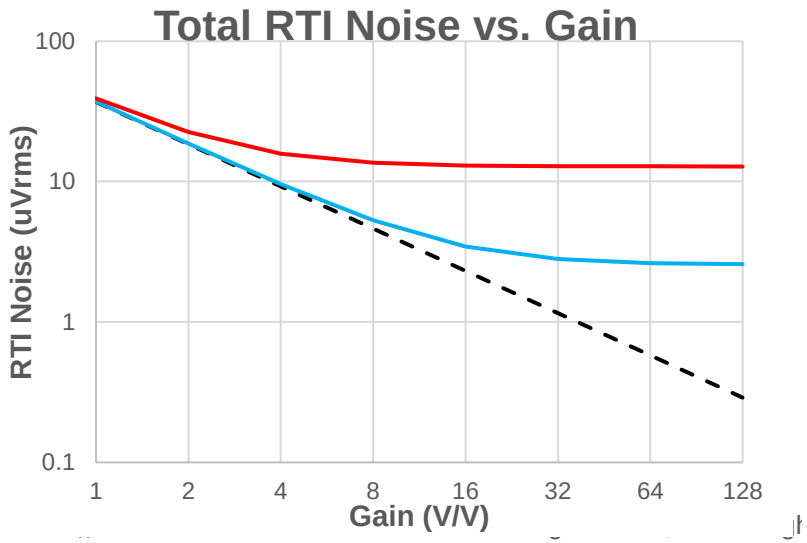


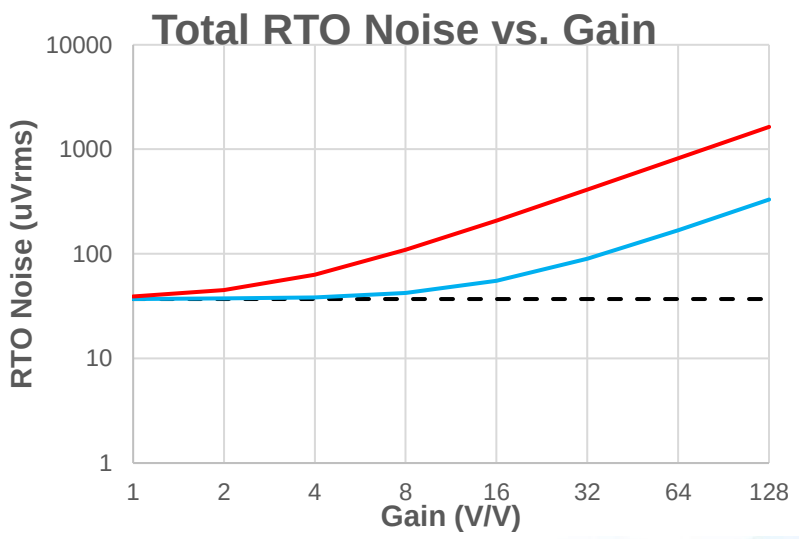
When Do I Want More Gain?

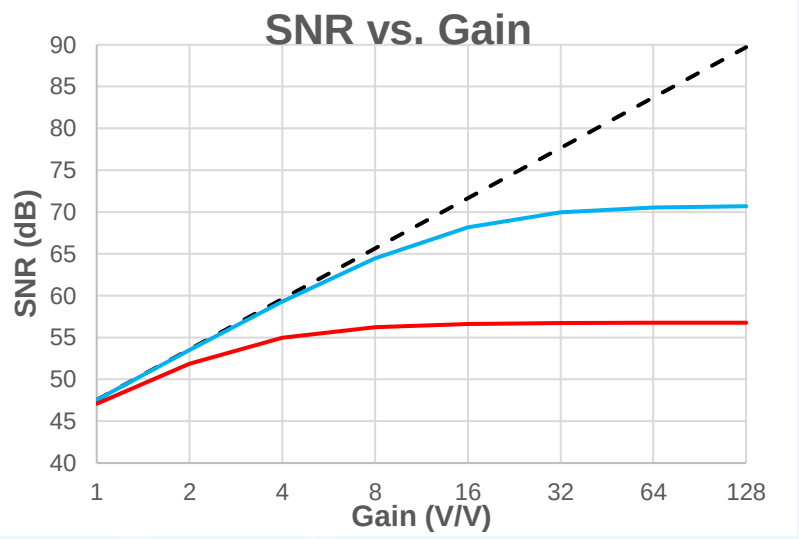


- $V_{n,AFE}$ = 0 nV/√Hz (IDEAL)
- $V_{n,AFE}$ = 5 nV/√Hz (LOW)
- $V_{n,AFE}$ = 25 nV/√Hz (HIGH)

$$SNR = 20\log\left(\frac{Signal\ (rms)}{Noise\ (rms)}\right)$$

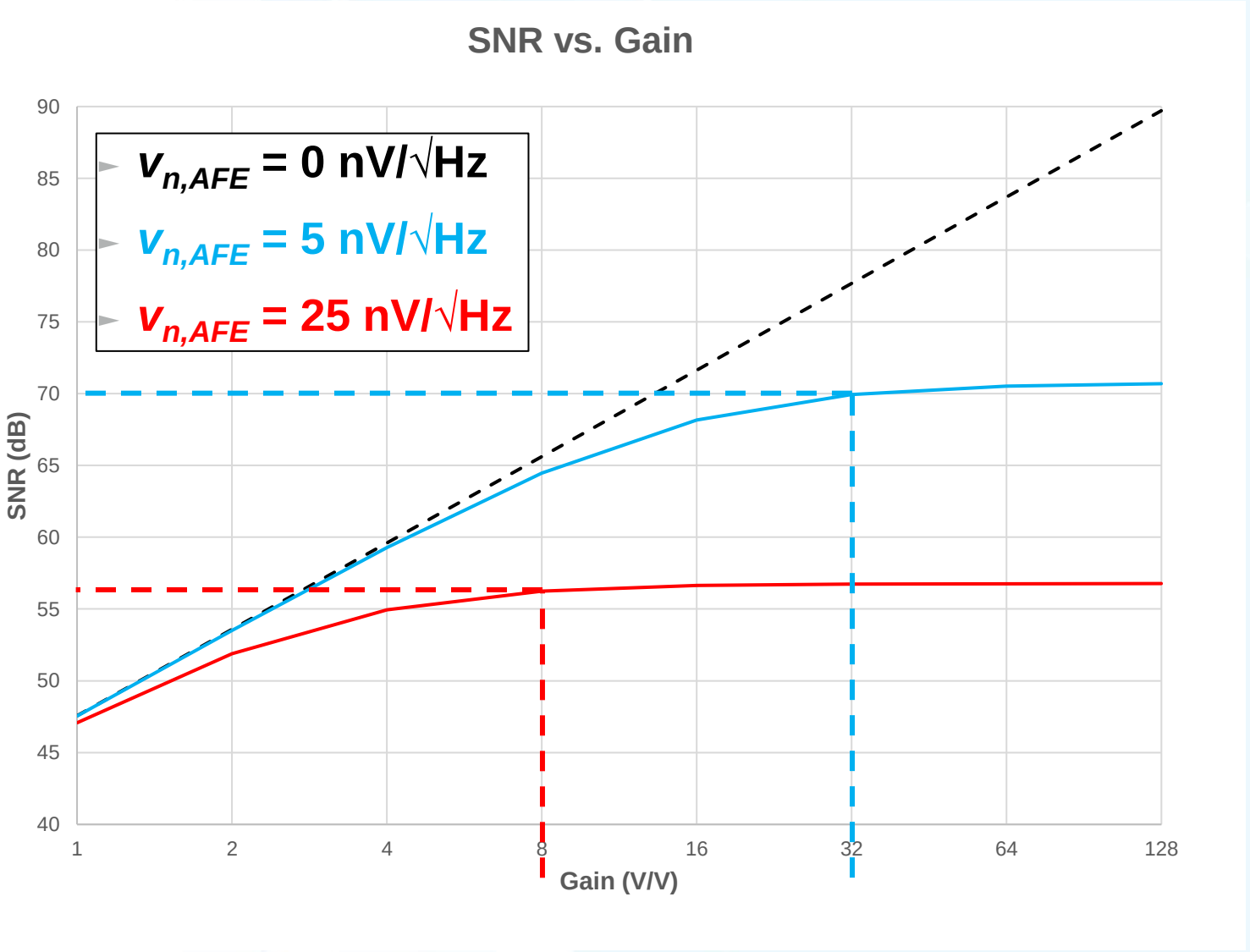






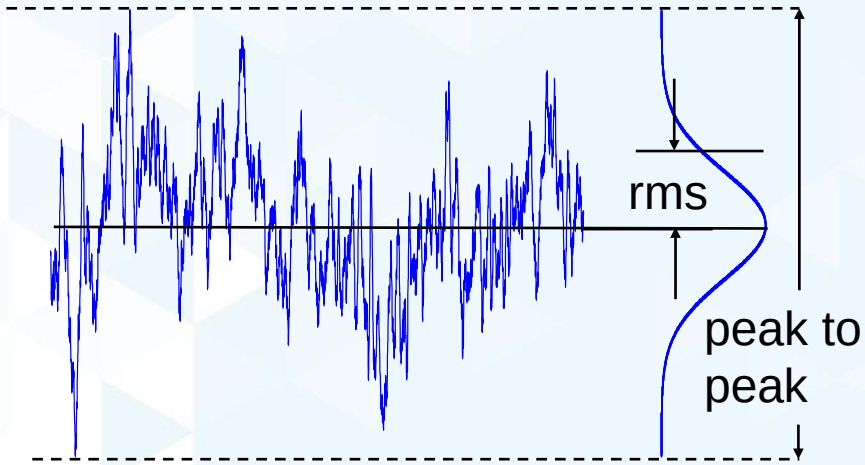
When Do I Want More Gain?

- Adding gain improves SNR until the RTO AFE noise dominates
- Lower noise front-end circuitry enables higher maximum SNR
  - But are often times higher power!
- Next step: filters to cut out-of-band noise
  - Reduce noise while maintaining signal amplitude



Cutting Through The Noise - Takeaways

- RMS voltage noise **is** predictable!
  - Can make informed design decisions to achieve target SNR
- Signal-chain noise optimization is a game of whack-a-mole!
  - Biggest bang for your buck → target the worst offenders
- Strategies to manage noise:
  - Low-noise front end with gain
  - Filtering to reduce remaining in-band noise

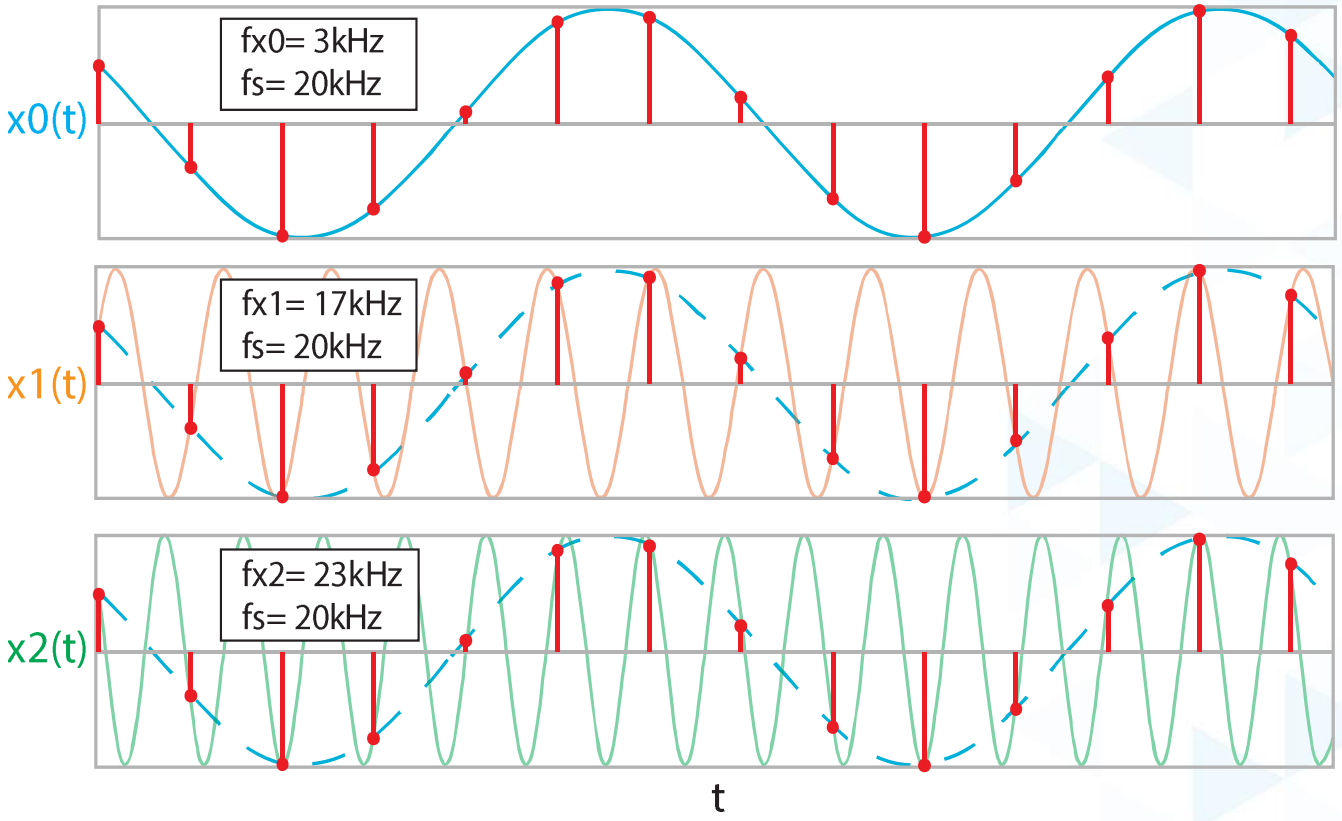


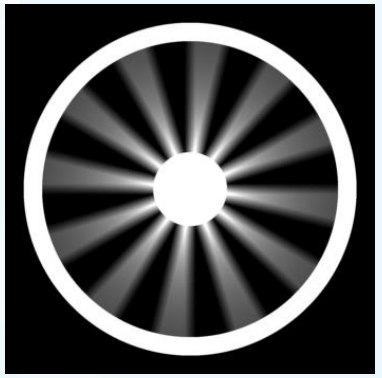
Example Noise Waveform

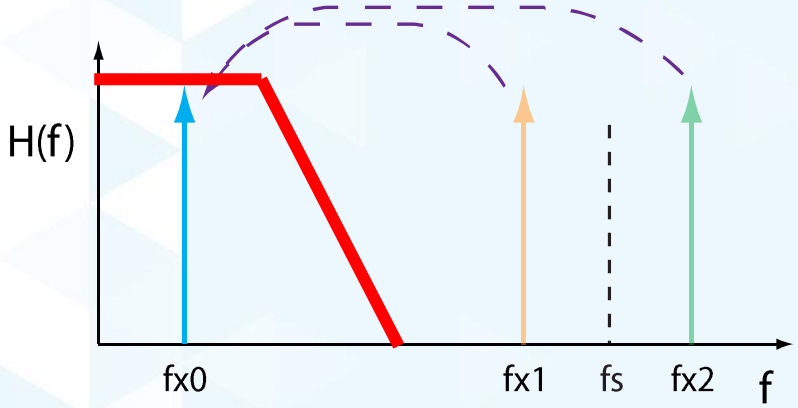
Filtering

Why do I need an anti-aliasing filter?

Nyquist–Shannon sampling theorem
For a sampling system, perfect reconstruction of the original signal requires the sampling frequency to be at least twice the max signal frequency







But I have a filter on the ADC input – why do I need another one?

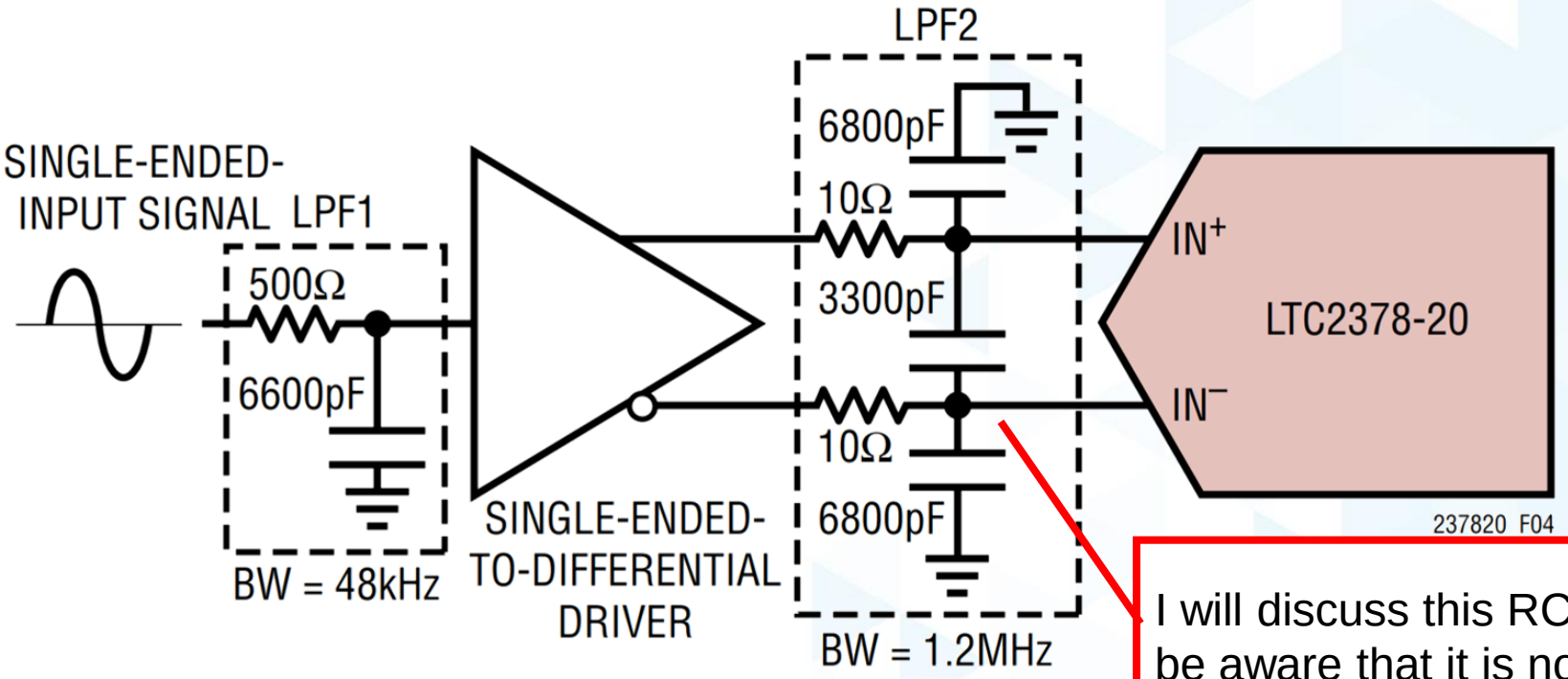
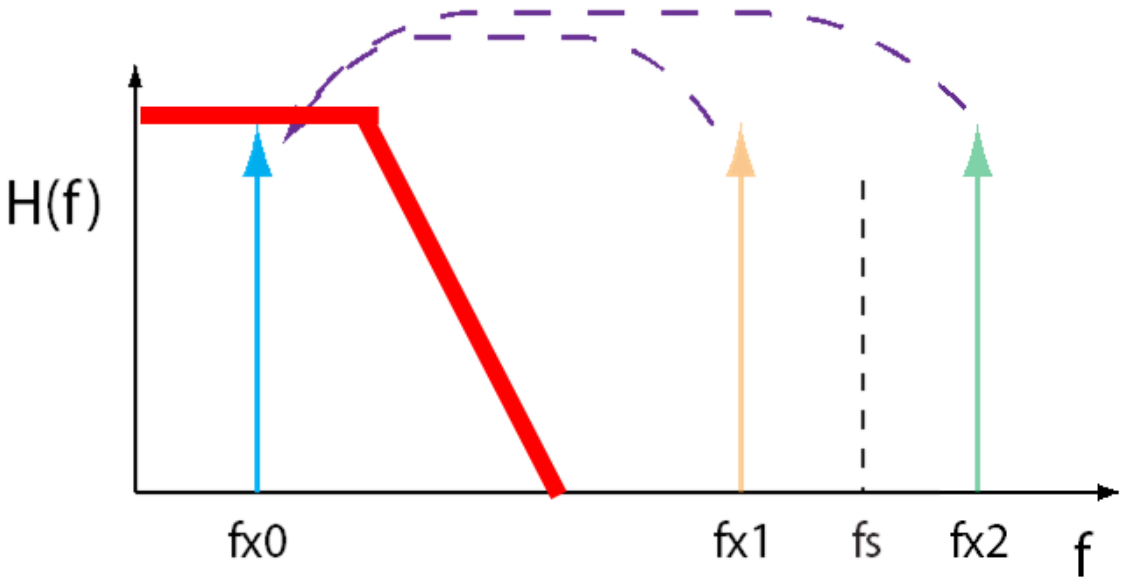


Figure 4. Input Signal Chain

I will discuss this RC filter later. Just be aware that it is not functioning as an anti-aliasing filter

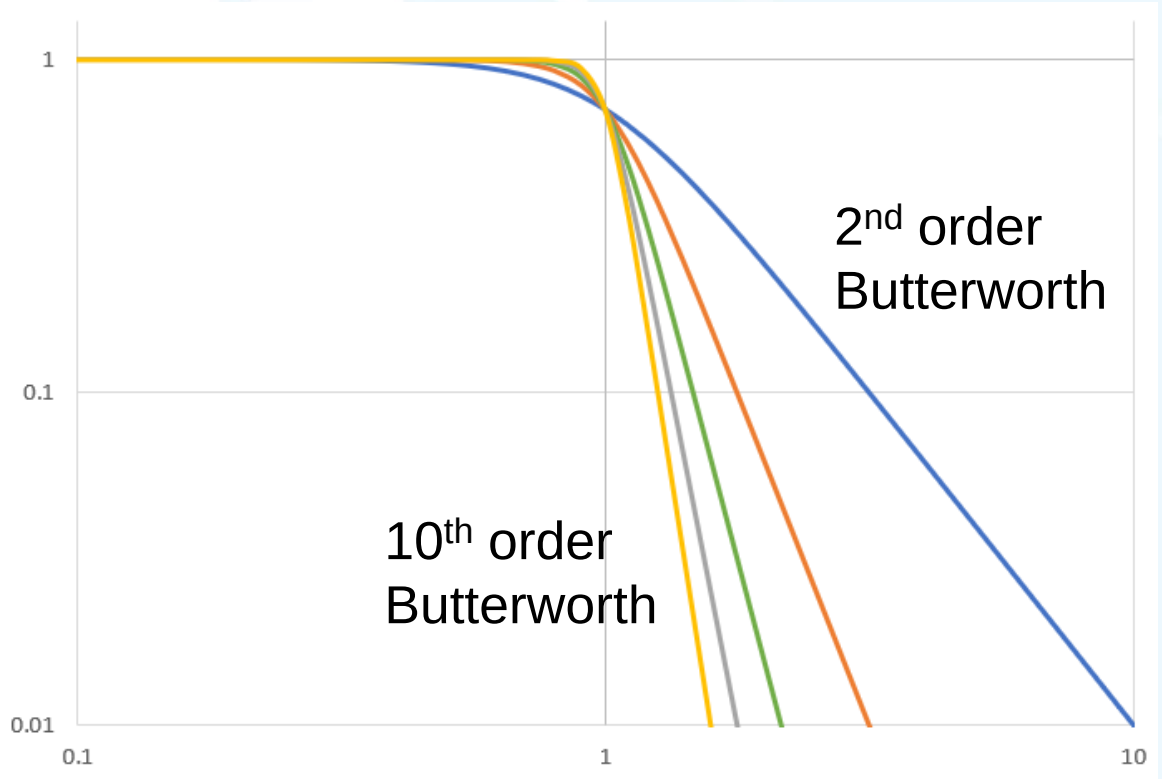
There is an RC filter required at the ADC input as part of the drive circuitry – but this filter does not provide adequate anti-aliasing. The fc for this RC is usually well above the Nyquist frequency.

Filtering – determine your criteria

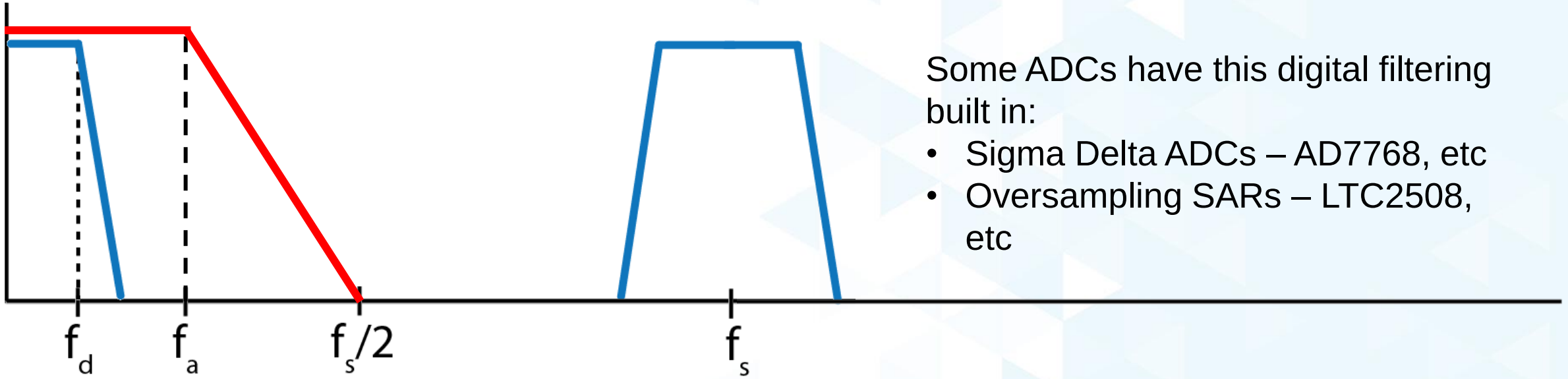


Determine the shape of the filtering you need to achieve anti-aliasing – the steeper the slope, the higher order filter you need

Higher order → Steeper slope



Easing the requirements on the anti-alias filter



Some ADCs have this digital filtering built in:

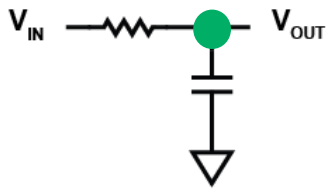
- Sigma Delta ADCs – AD7768, etc
- Oversampling SARs – LTC2508, etc

- Allow the digital filter (averaging, sinc, FIR, etc) determine the pass band response, and then the analog filter is in place for anti-aliasing
- Digital filtering eases the requirements of the analog filter
- Oversampling eases the analog filter requirements even more

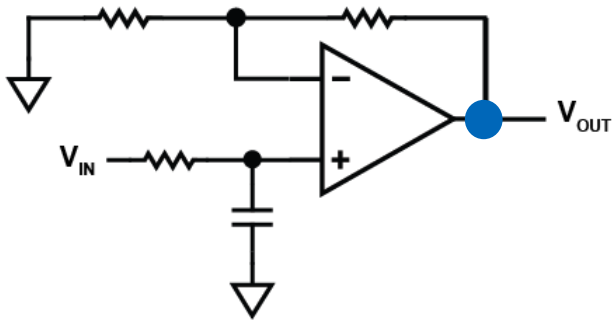
Added bonus – ADC noise is spread over the Nyquist zone, so noise floor is lower for higher fs

Topologies and Tradeoffs – 1st order

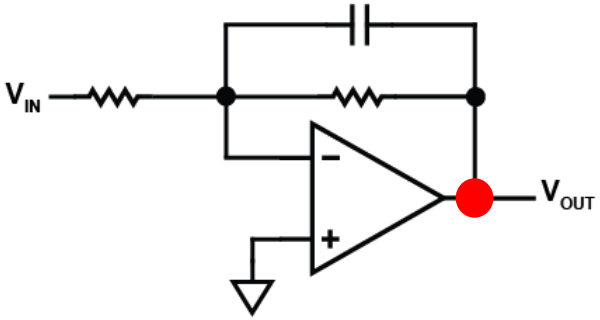
Passive RC

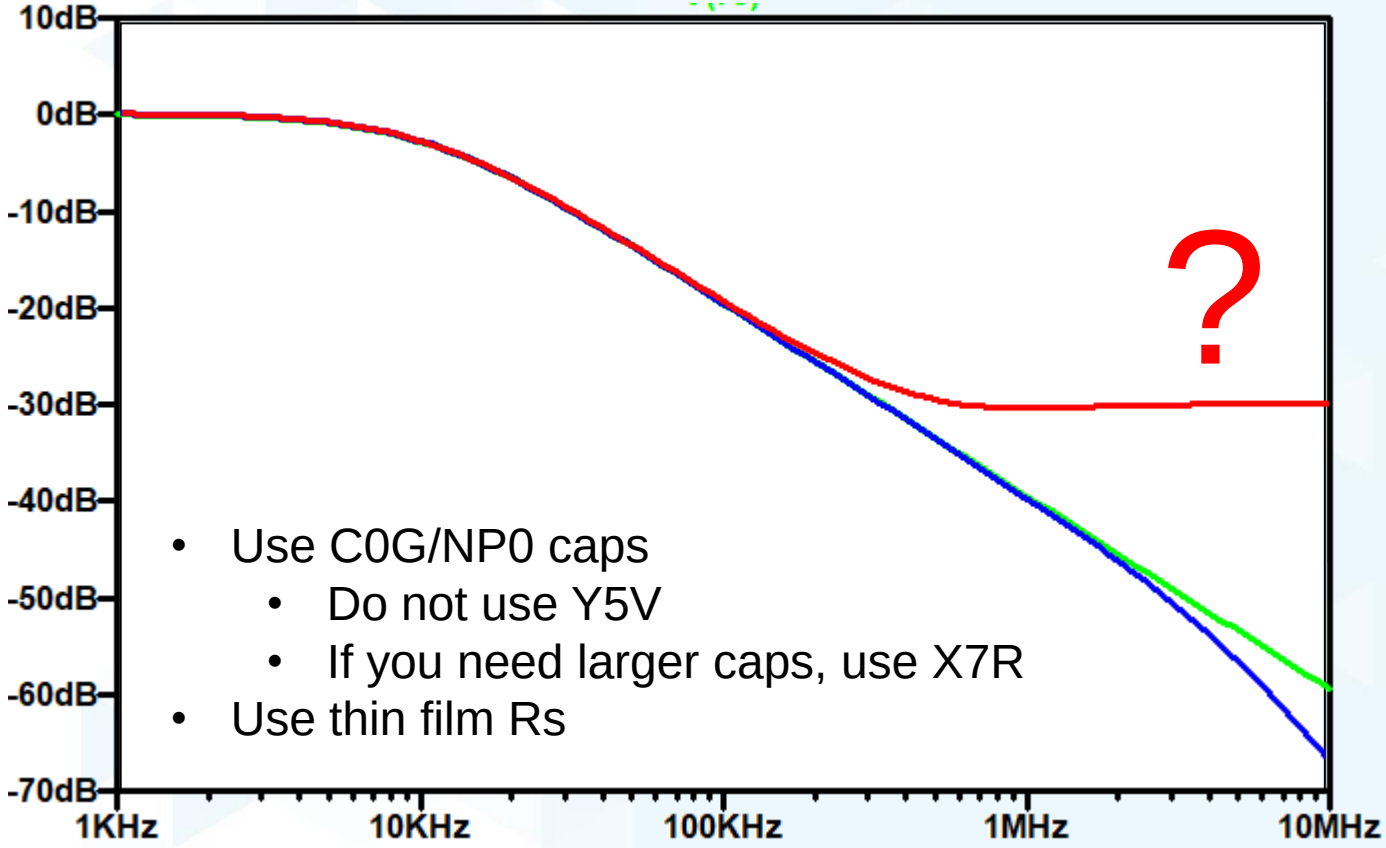


Non-inverting



Inverting

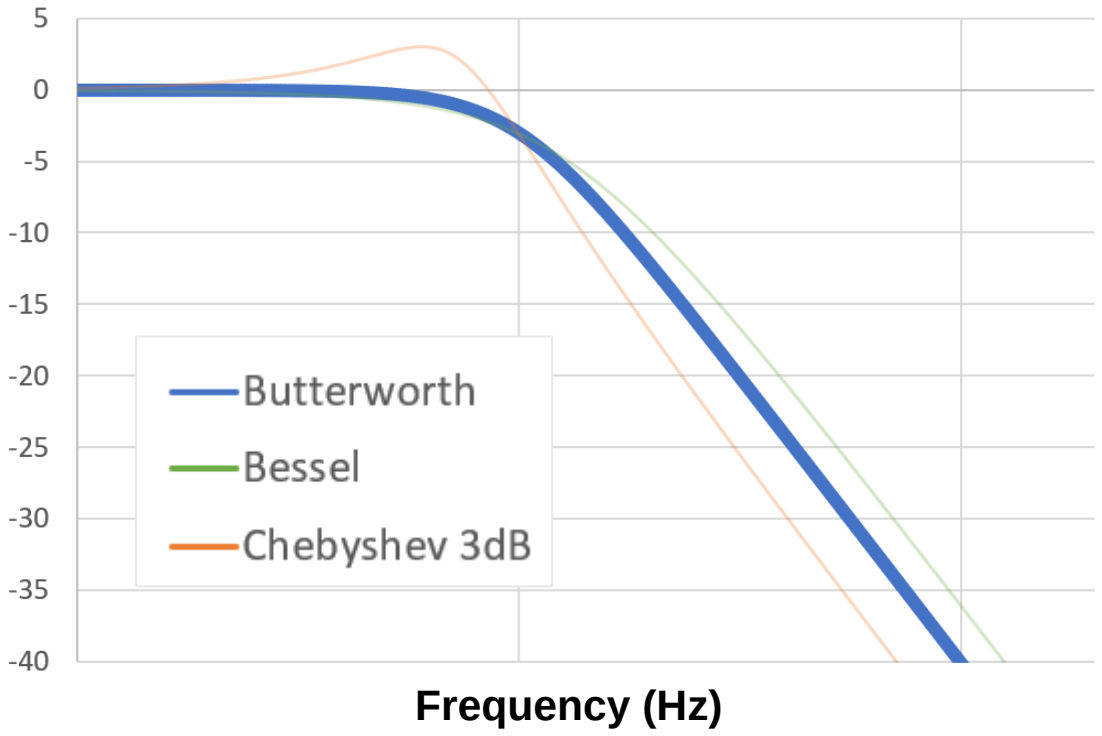




- Active filters can provide gain, and better tuning of poles in multi-pole filter designs
- Active filters are limited by the ability of the amplifier

Response types and Tradeoffs

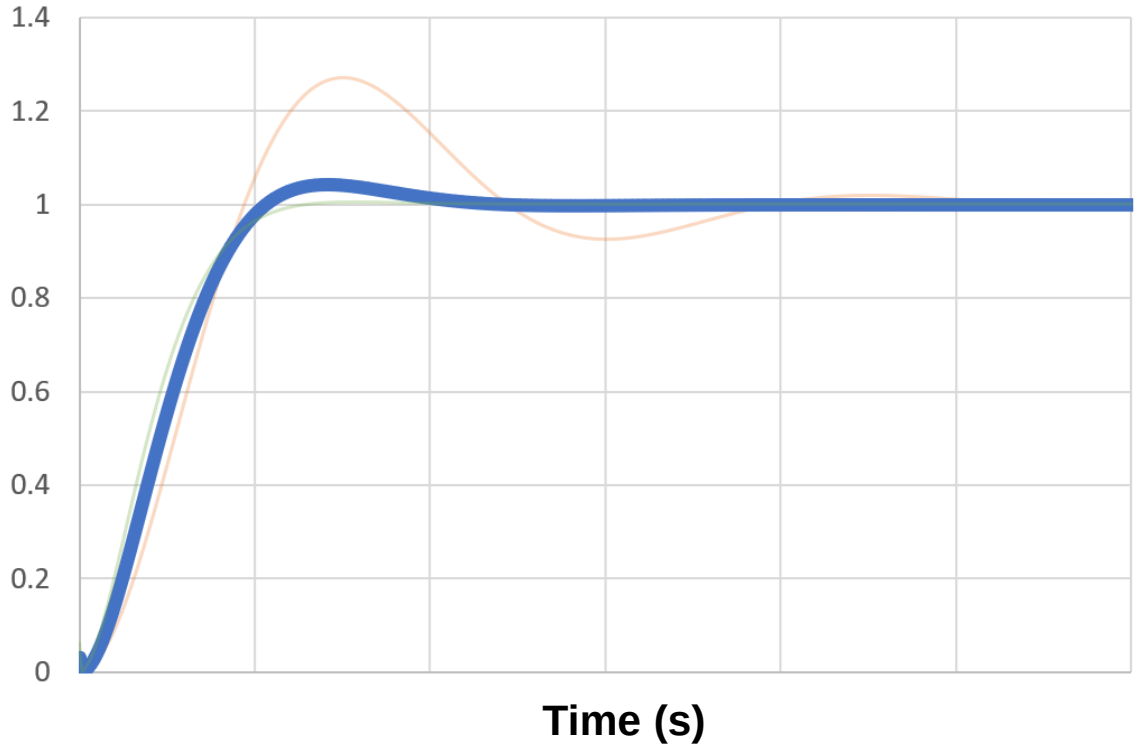
Magnitude Response (dB)



Comparing implementations with same number of stages (2nd order shown above):

- Chebyshev has steeper rolloff

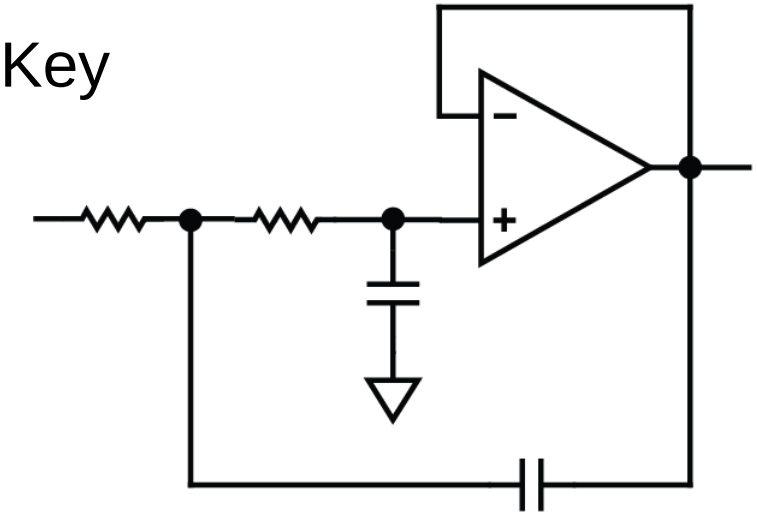
Step Response (V)

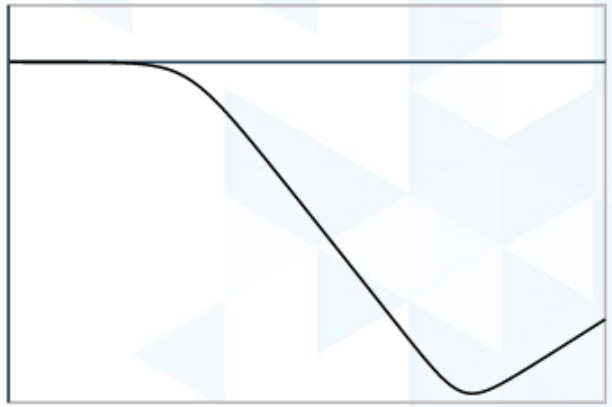


- Bessel has optimal step response
- Butterworth has flattest frequency response in pass band

Topologies and tradeoffs – 2nd order

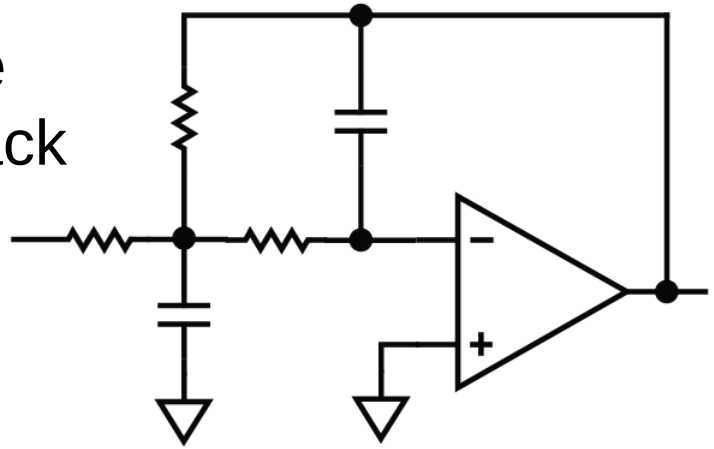
Sallen Key

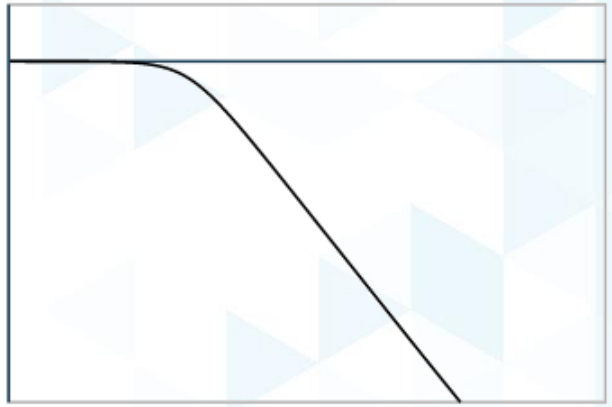




Magnitude response

Multiple Feedback





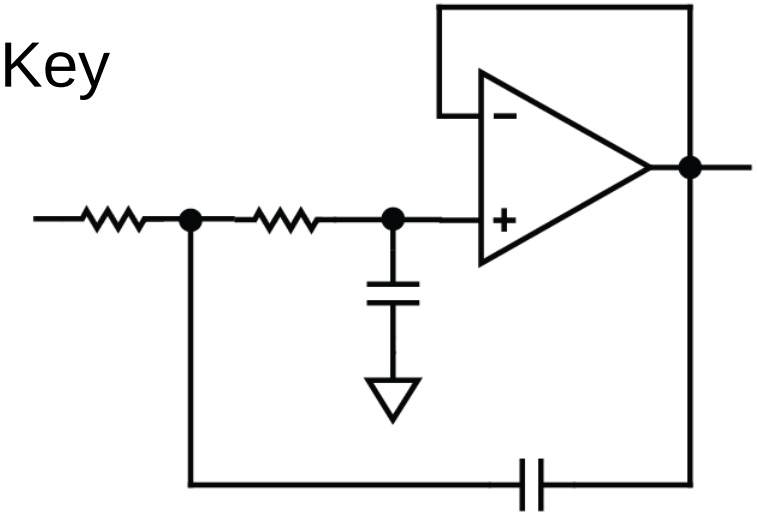
Sallen Key is more susceptible to the same issue as inverting 1st order at high frequencies

Learn more about impact of amplifier output impedance on Sallen Key topology by watching “Sallen-Key 101 Whiteboard Series”

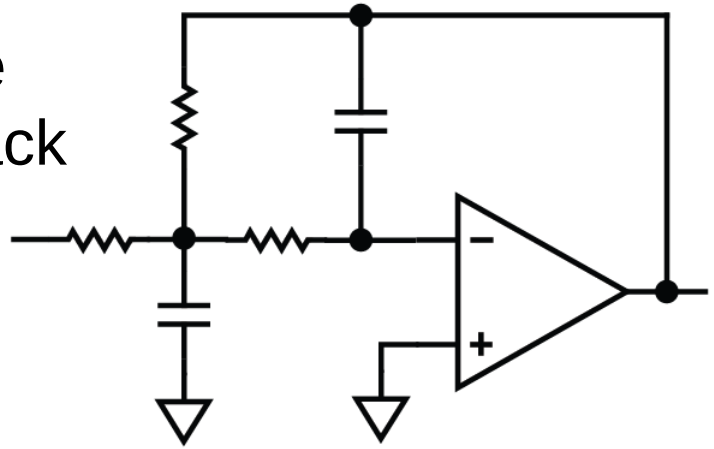
https://youtu.be/_BYZirwIEEI

Topologies and tradeoffs – 2nd order

Sallen Key



Multiple Feedback

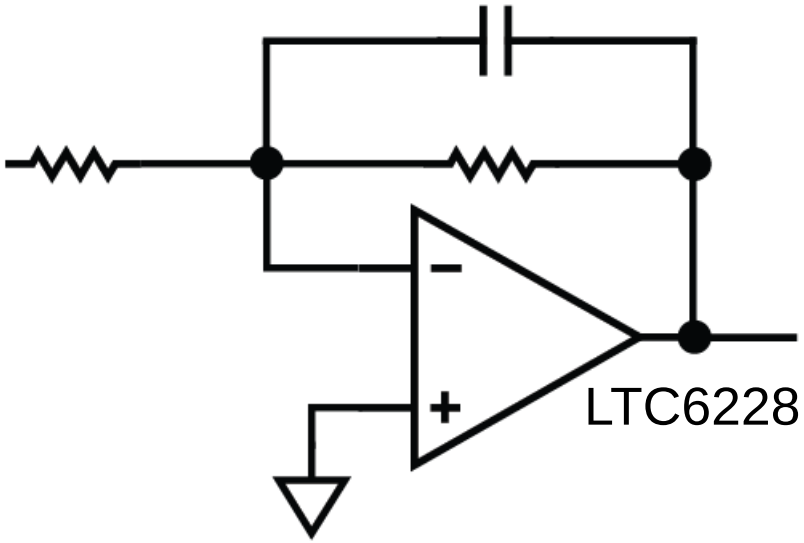


Tradeoffs between Sallen Key and MFB:

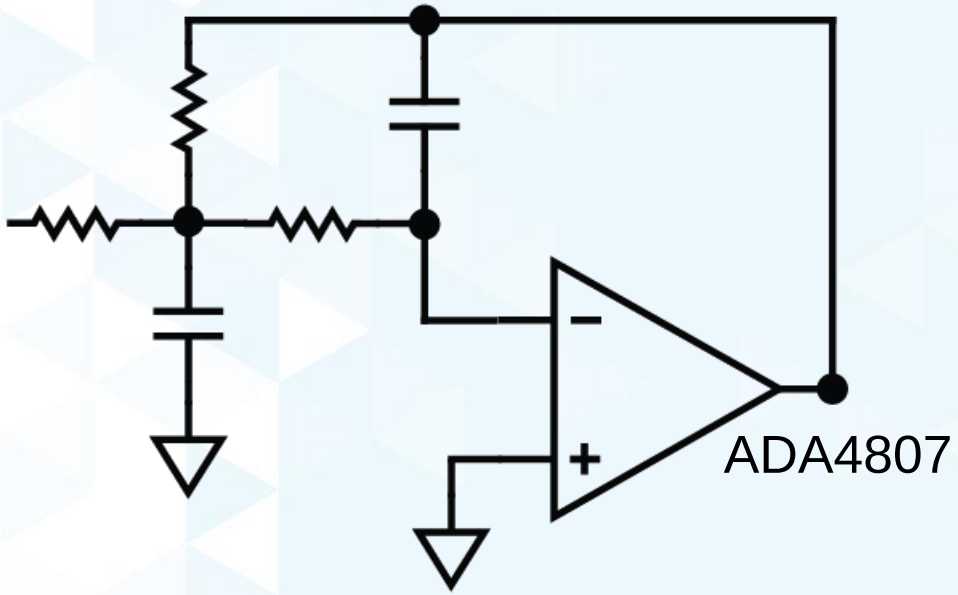
- When gain = 1, Sallen Key has fewer components and no gain error
  - These advantages disappear when gain is not 1
- Sallen Key has better passband and fc fidelity when op amp GBW is marginal
- MFB is better behaved at higher Qs

Filtering topologies for fully differential amps

1st Order Inverting

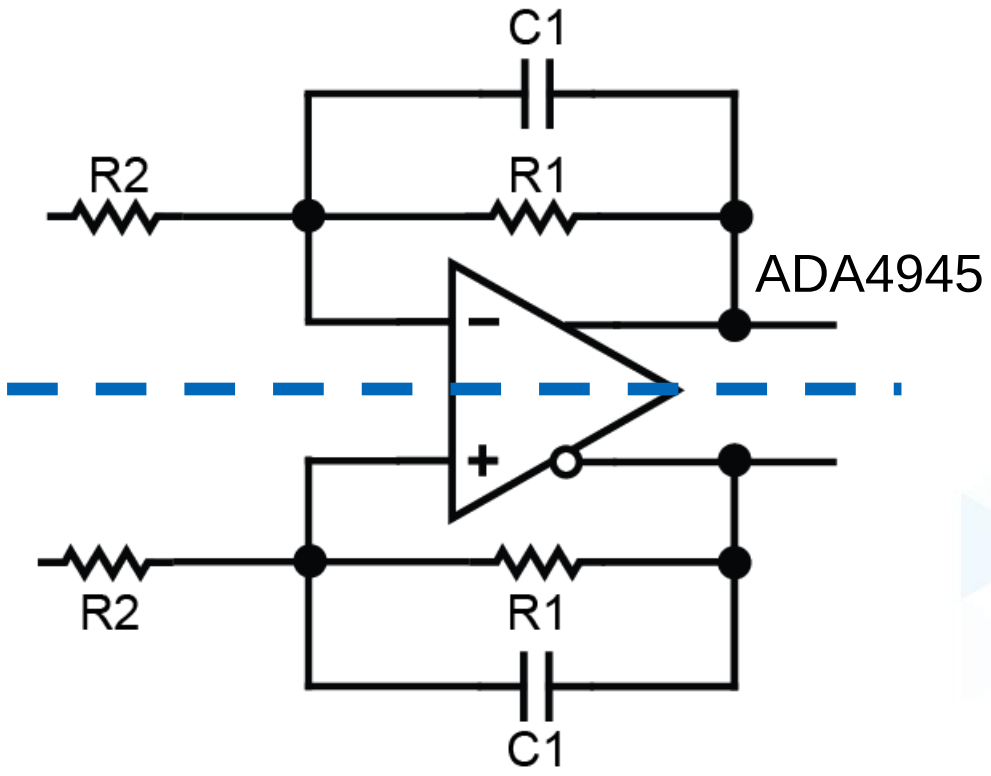


2nd Order Multiple Feedback

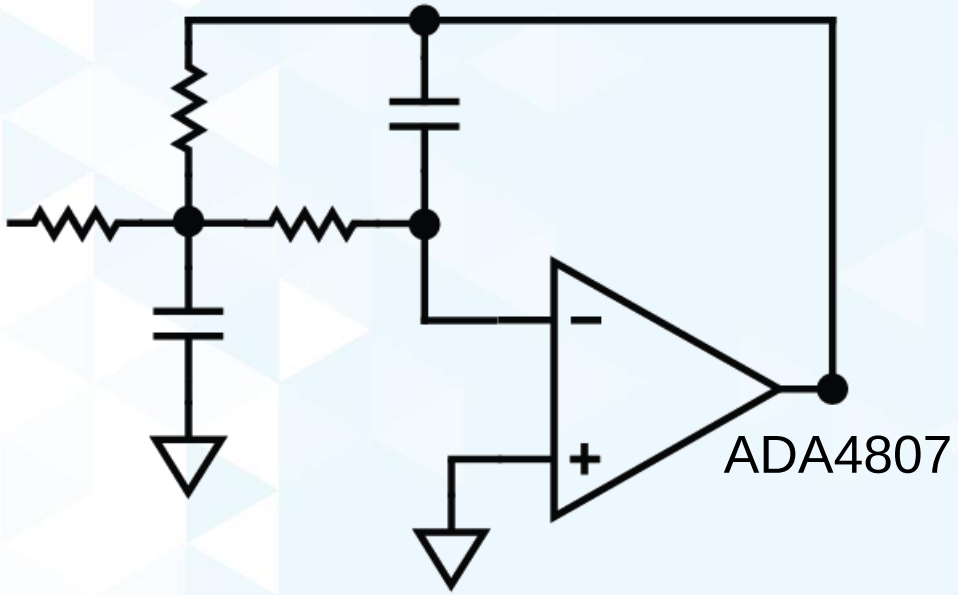


Filtering topologies for fully differential amps

1st Order Inverting

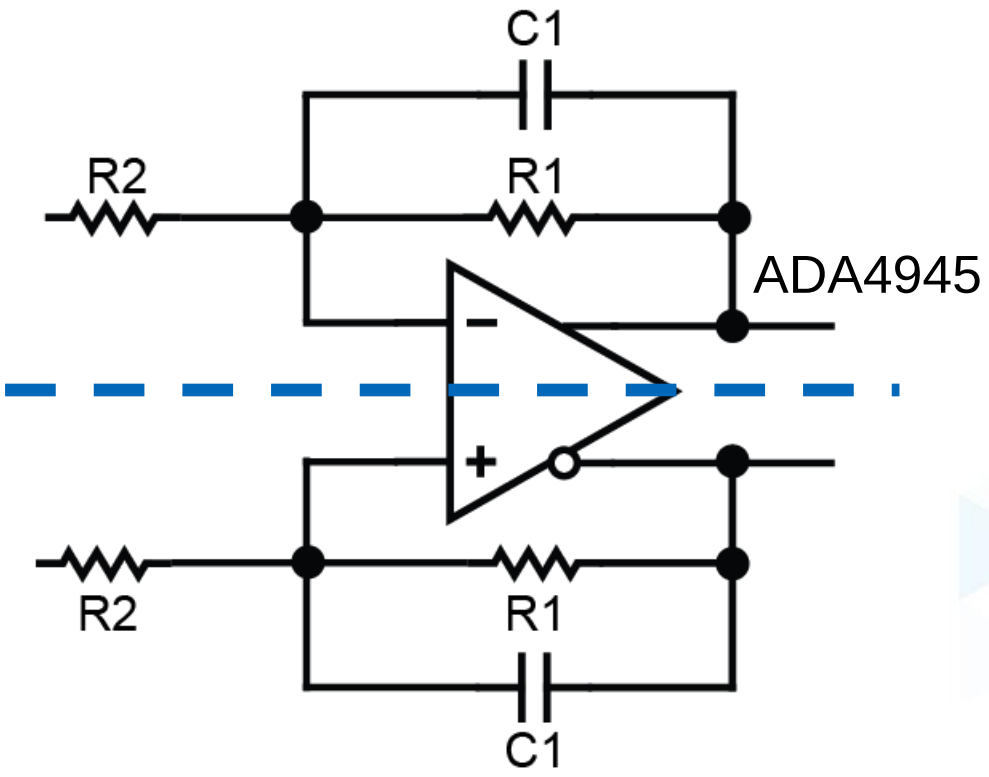


2nd Order Multiple Feedback

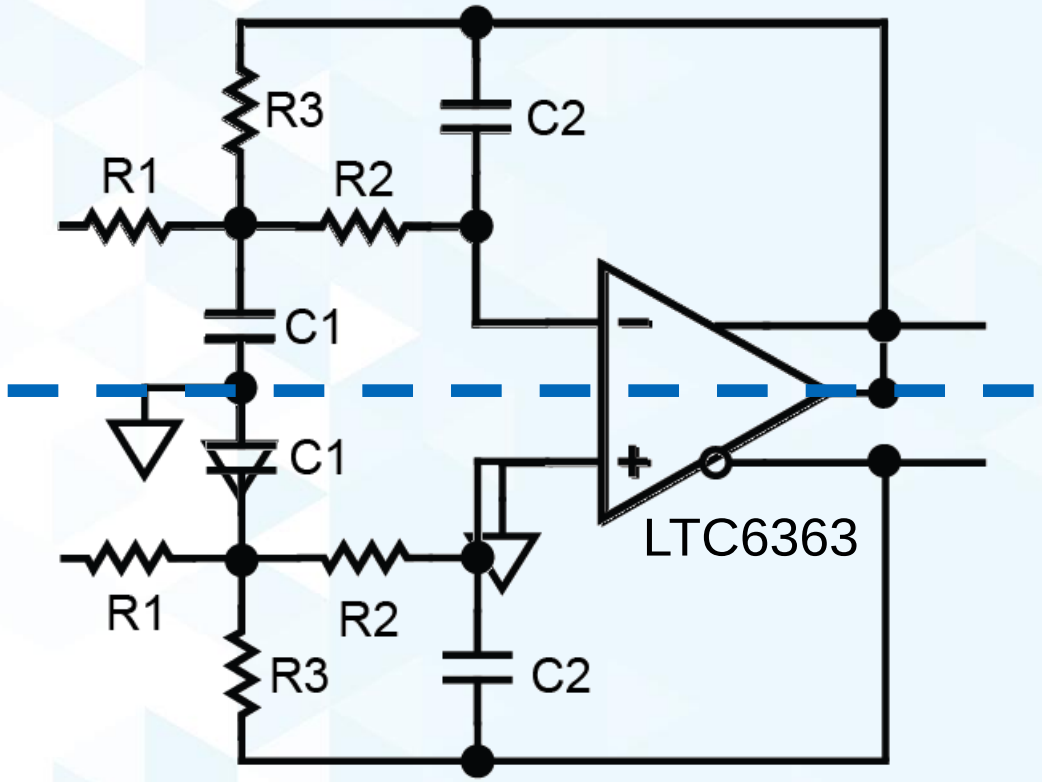


Filtering topologies for fully differential amps

1st Order Inverting



2nd Order Multiple Feedback



Learning more about Filtering

- Oversampling and digital filtering to ease requirements of analog filters - https://www.analog.com/en/analog-dialogue/articles/antialiasing-filtering-considerations-for-high-precision-ad-converters.html
- Filtering 101 whiteboard video series - https://www.youtube.com/watch?v=ftk9C45F_bo&list=PL64A193CF0B94C5D3
- Sallen-Key 101 whiteboard video series - https://www.youtube.com/watch?v=DEV7l66D6Ys&list=PLiwaj4qabLWxp1kilM2Pa6H-db8zygpNo
- Filter Wizard online design tool – http://www.analog.com/filterwizard

Driving the ADC input

Introduction – What is “Precision ADC Driving?”

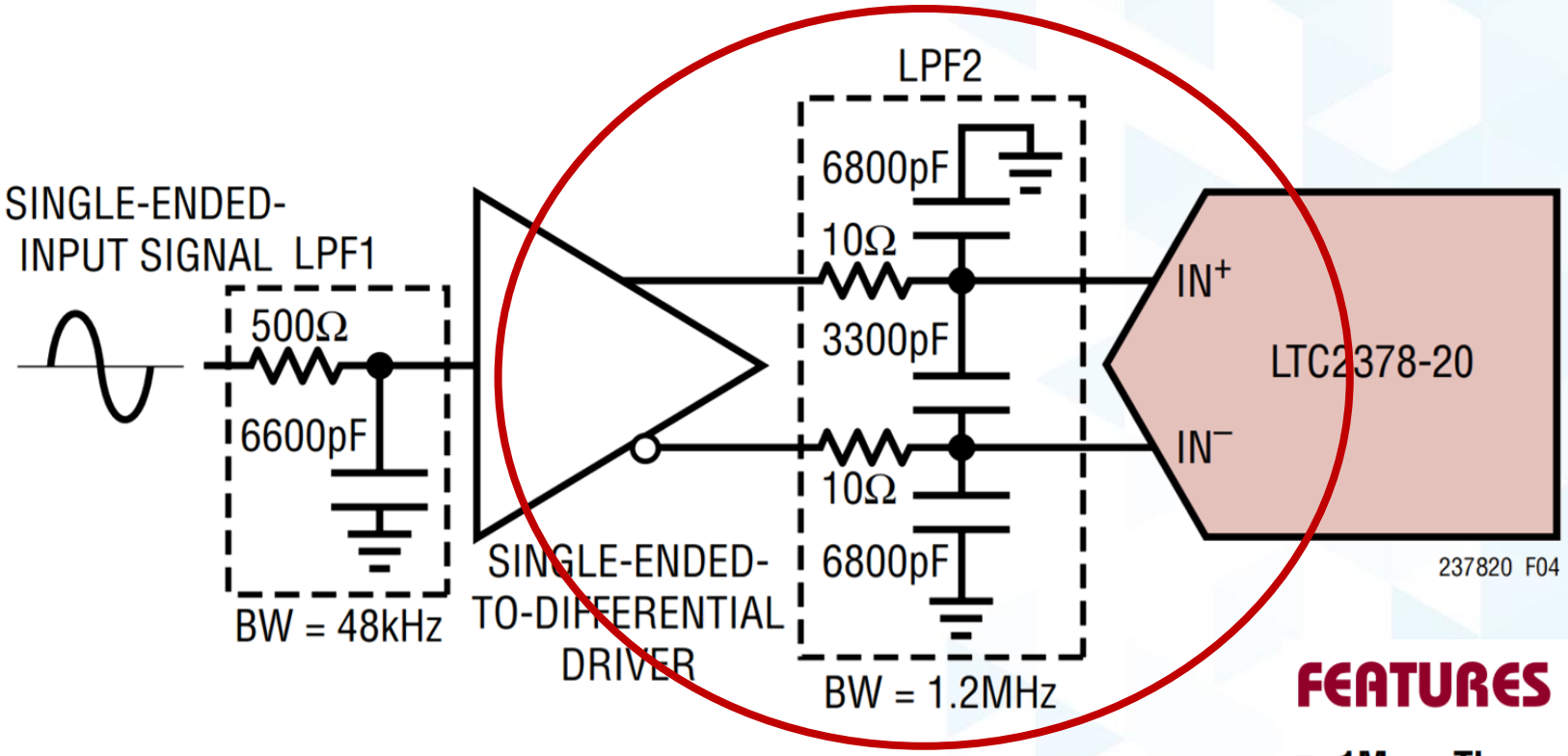
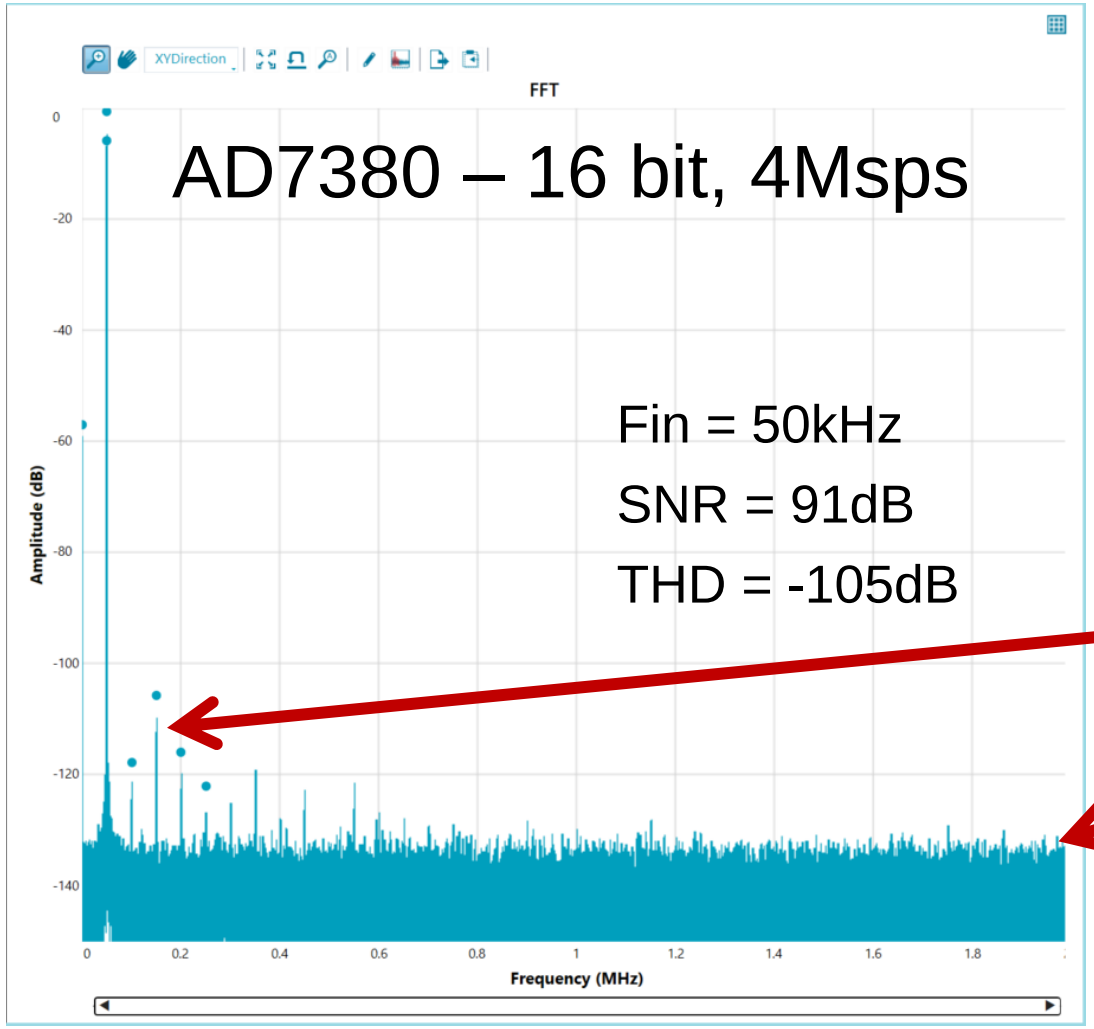


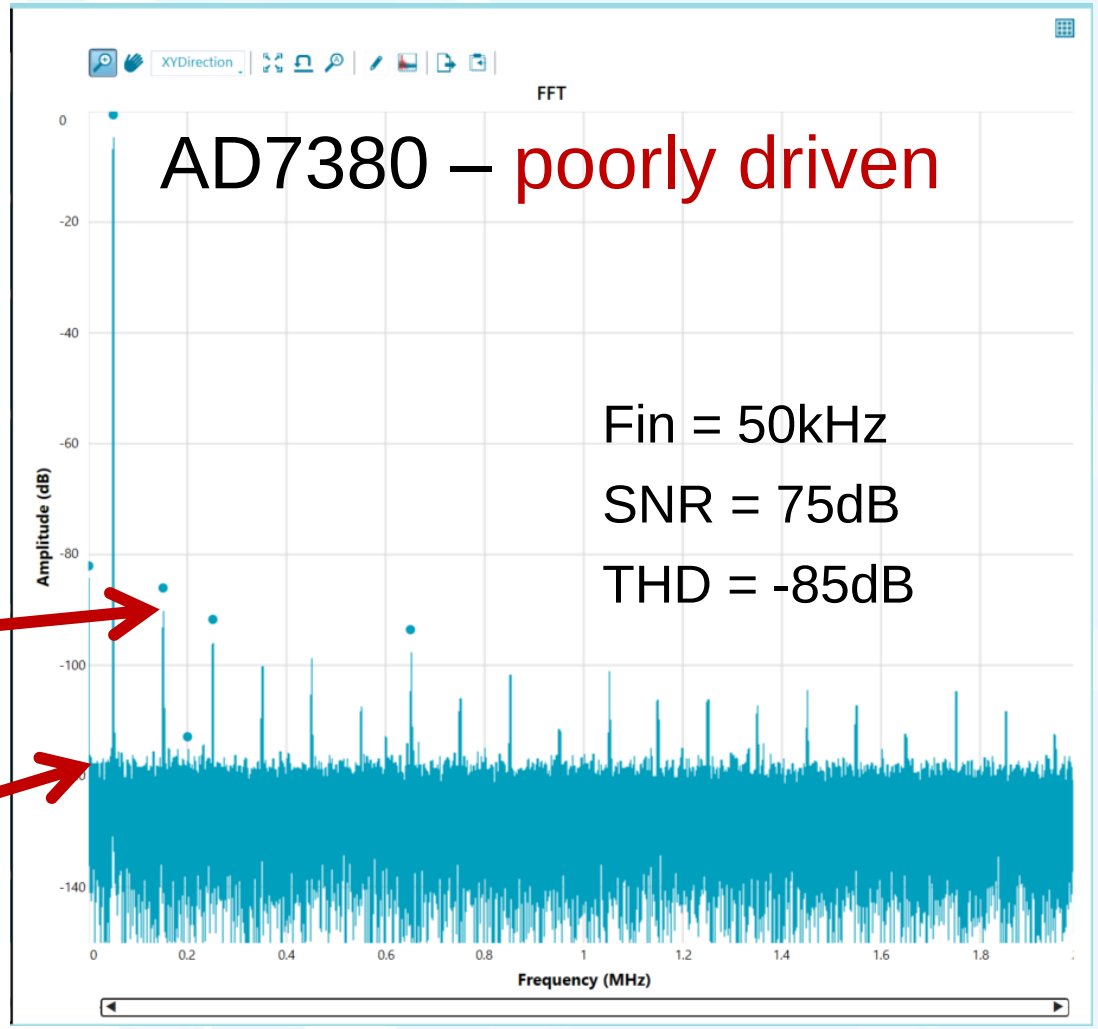
Figure 4. Input Signal Chain

FEATURES

- 1Msps Throughput Rate
- ±0.5ppm INL (Typ)
- Guaranteed 20-Bit No Missing Codes
- Low Power: 21mW at 1Msps, 21µW at 1ksps
- 104dB SNR (Typ) at f_{IN} = 2kHz
- –125dB THD (Typ) at f_{IN} = 2kHz

ADC Driving – Why do I care?

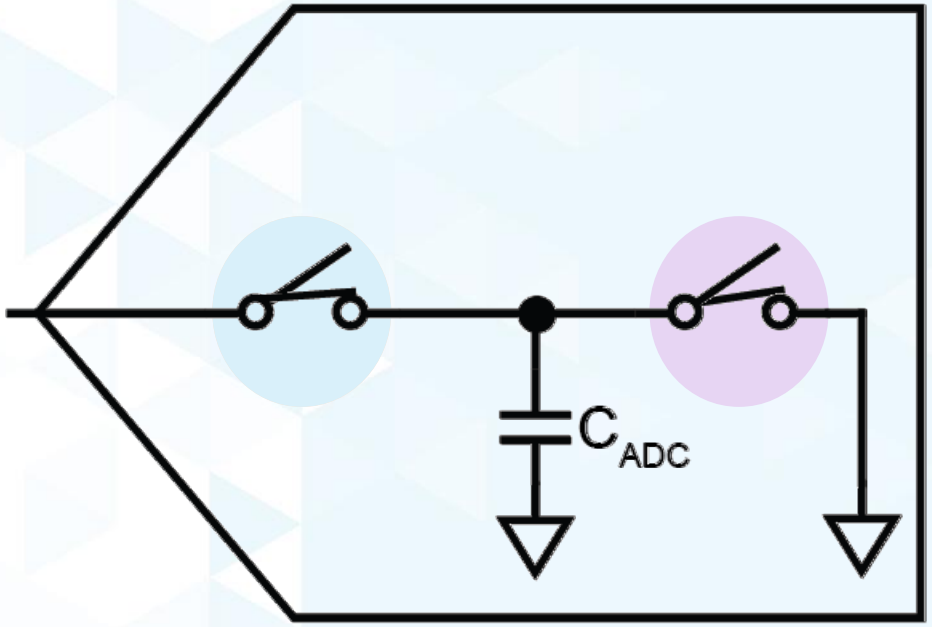


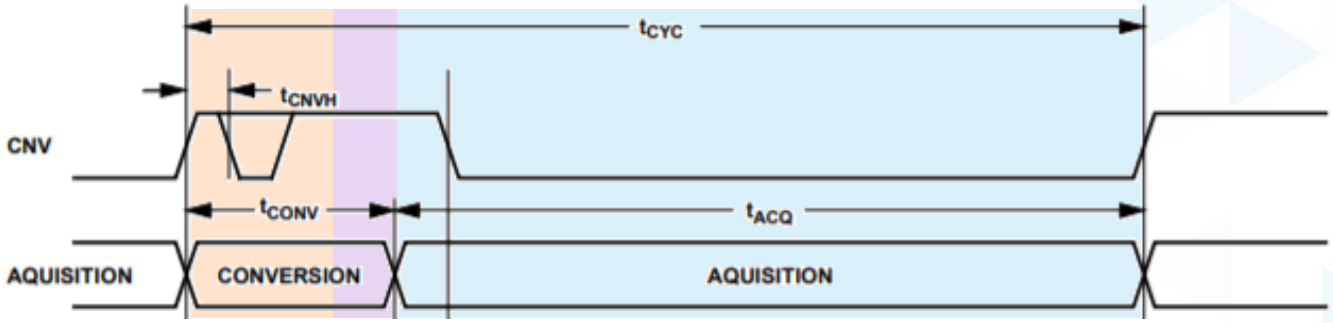


A Simple Model for the ADC Input

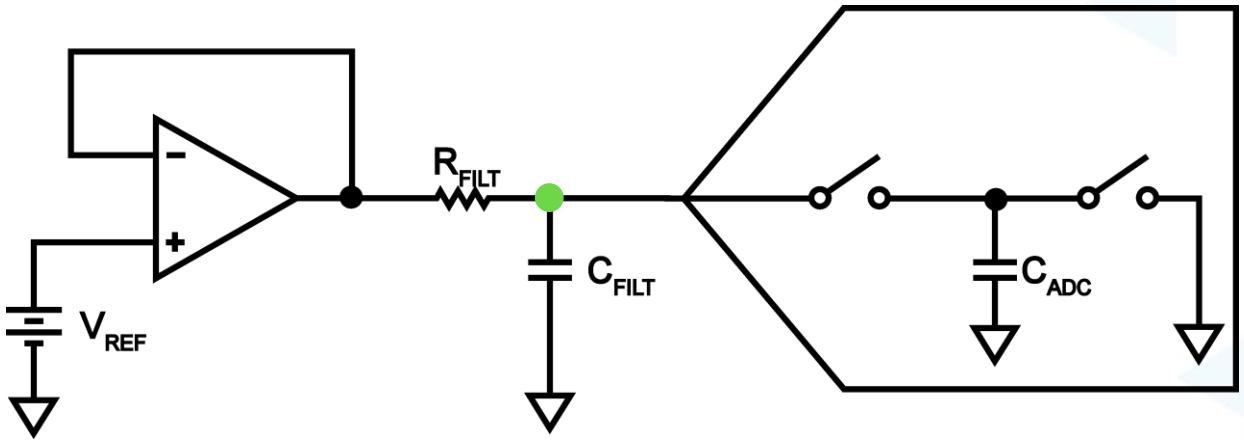
A simplified model of SAR ADC front end

- Switch at input is open for conversion
- C_{ADC} is discharged to ground prior to acquisition
- Switch at input is closed for acquisition
- Don’t overthink it – this is a simple model of the ADC input to understand why a driver is needed. This model does not describe the internal workings of the ADC.

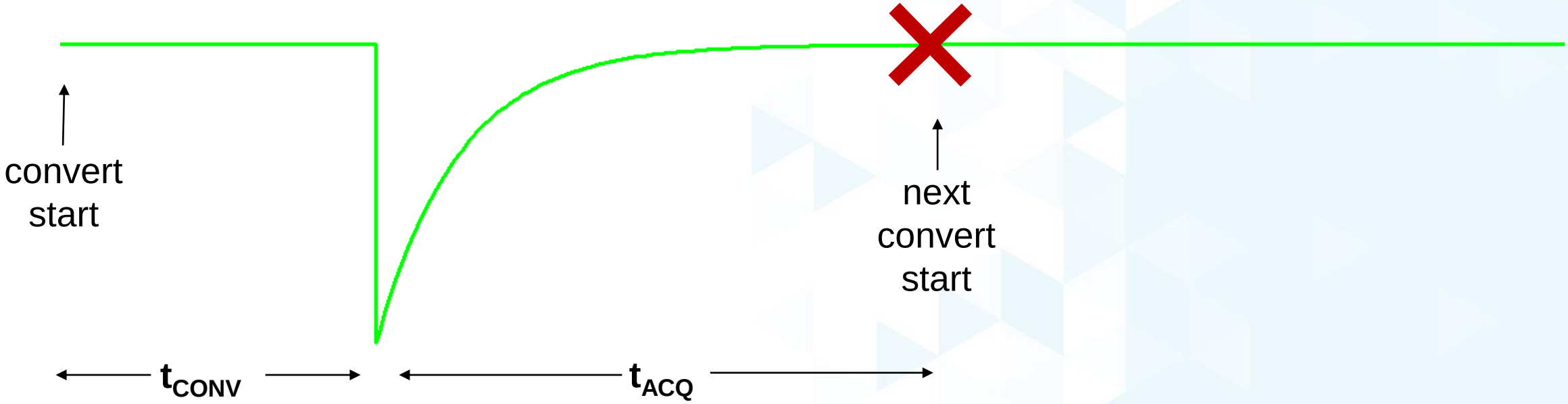




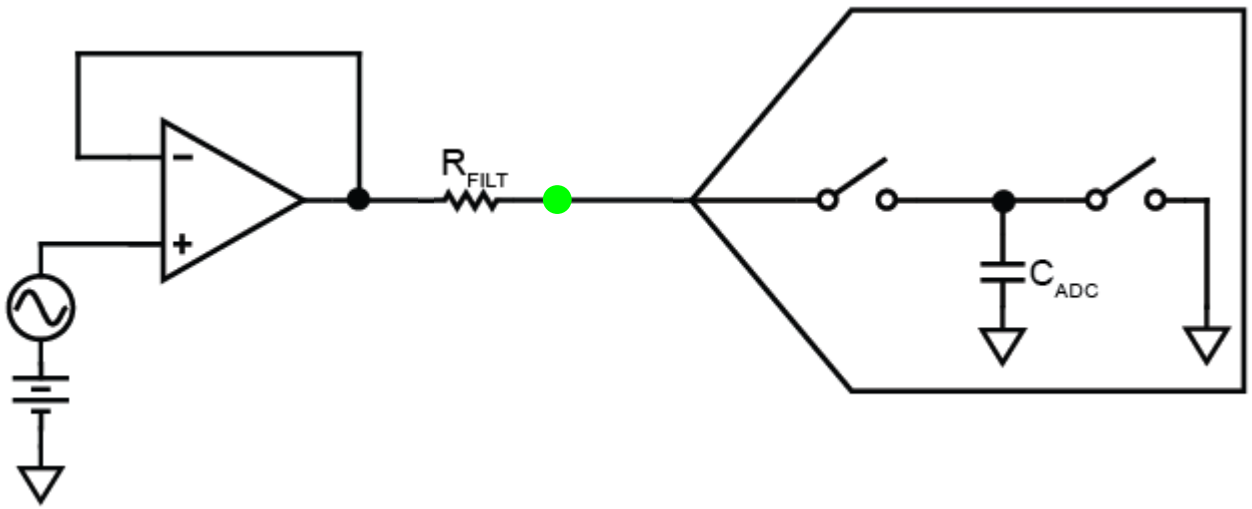
What happens at the ADC input?



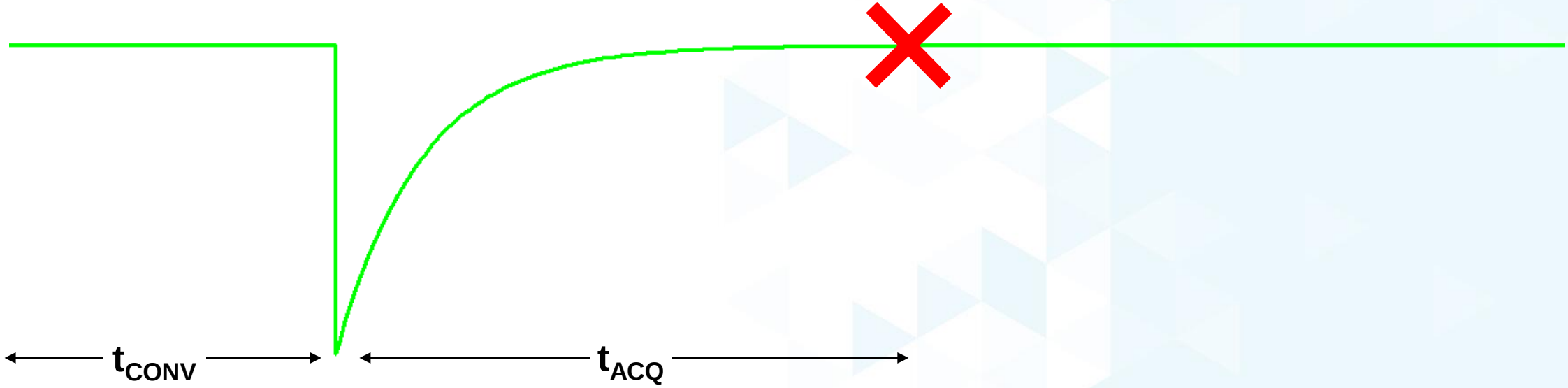
- Voltage difference between input and sample cap causes disturbance on ADC input
- Specifics of timing and kickback size varies with ADC architecture and driver circuitry
- If kickback is not fully settled by the end of the sample period, the resulting measurement can have error



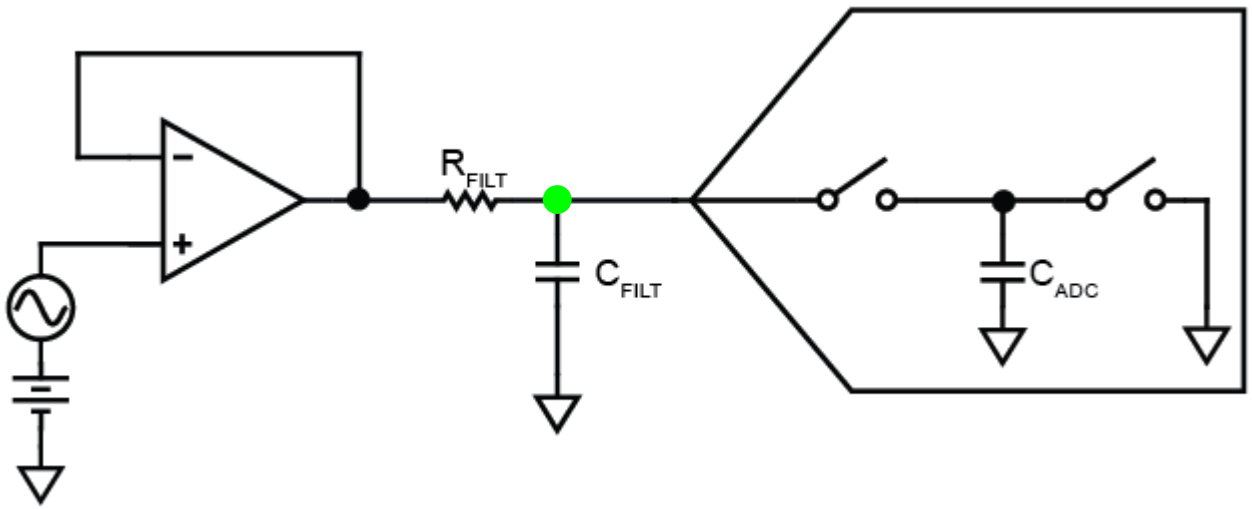
RC Filter – Why it's needed



- Rfilt needed to isolate amp output from capacitive load
- Cfilt dampens the kickback, and combined with Rfilt, and provides filtering of noise from the driver
- Remember – **this is not an anti-aliasing filter** – the BW of this RC is usually much higher than Nyquist



RC Filter – Why it's needed



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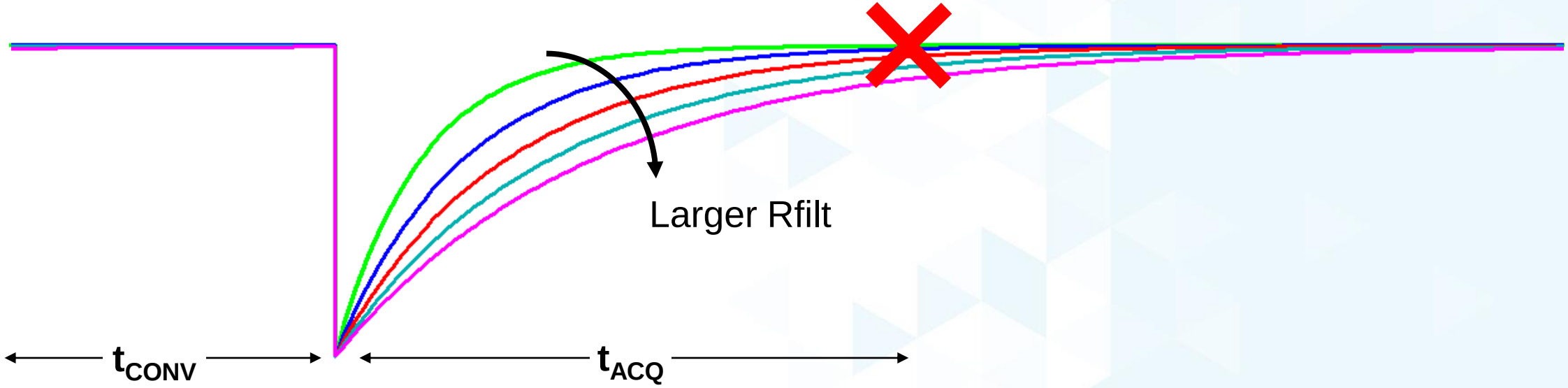
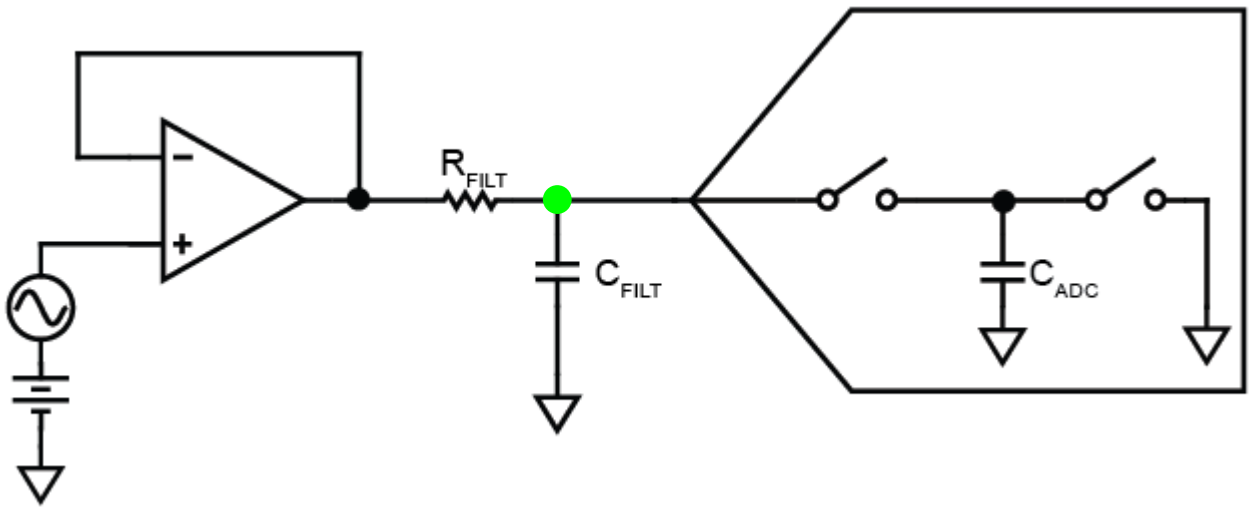
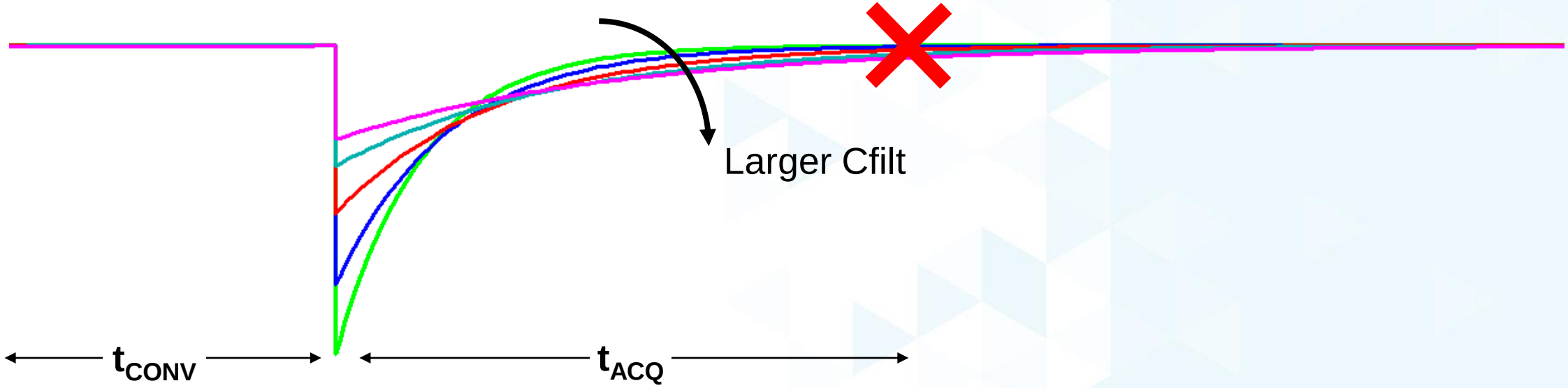


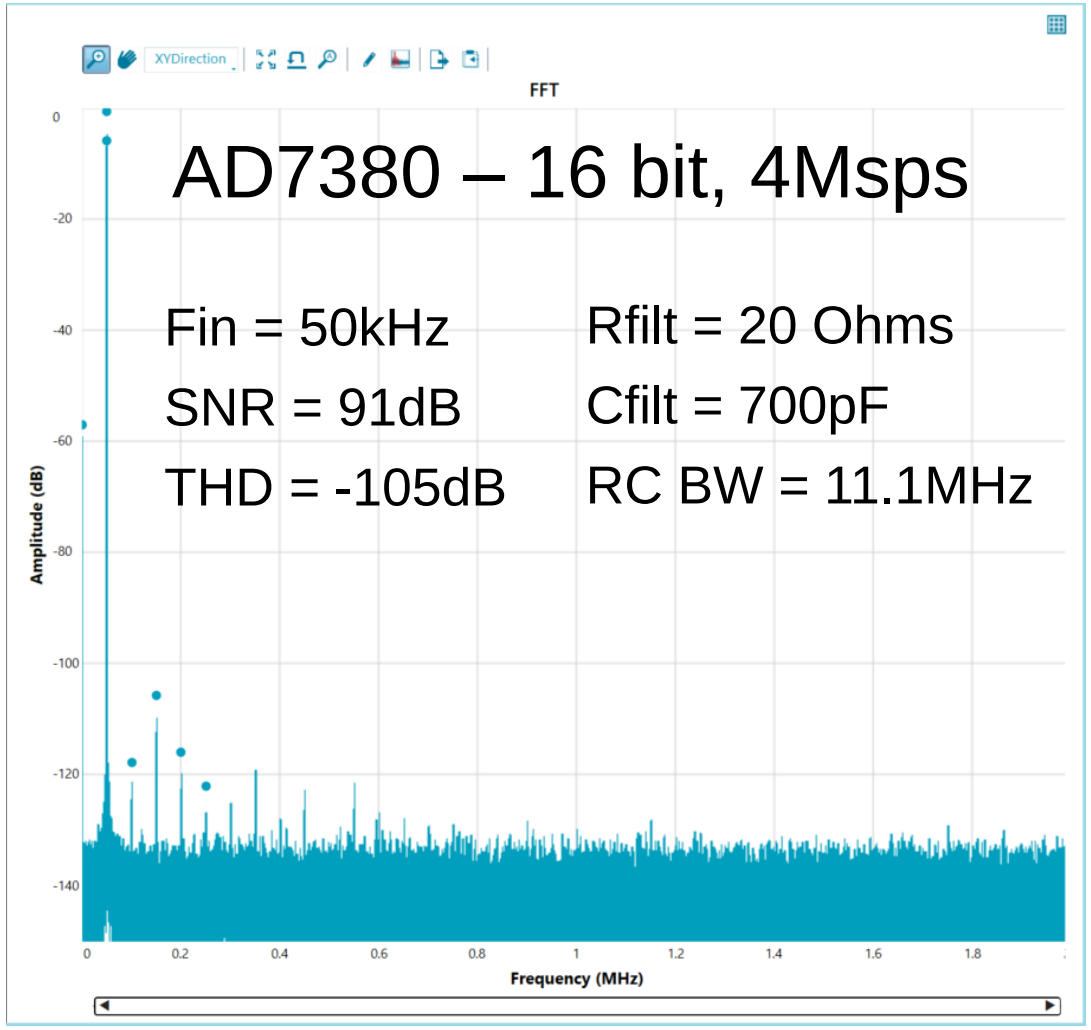
RC Filter – Why it's needed

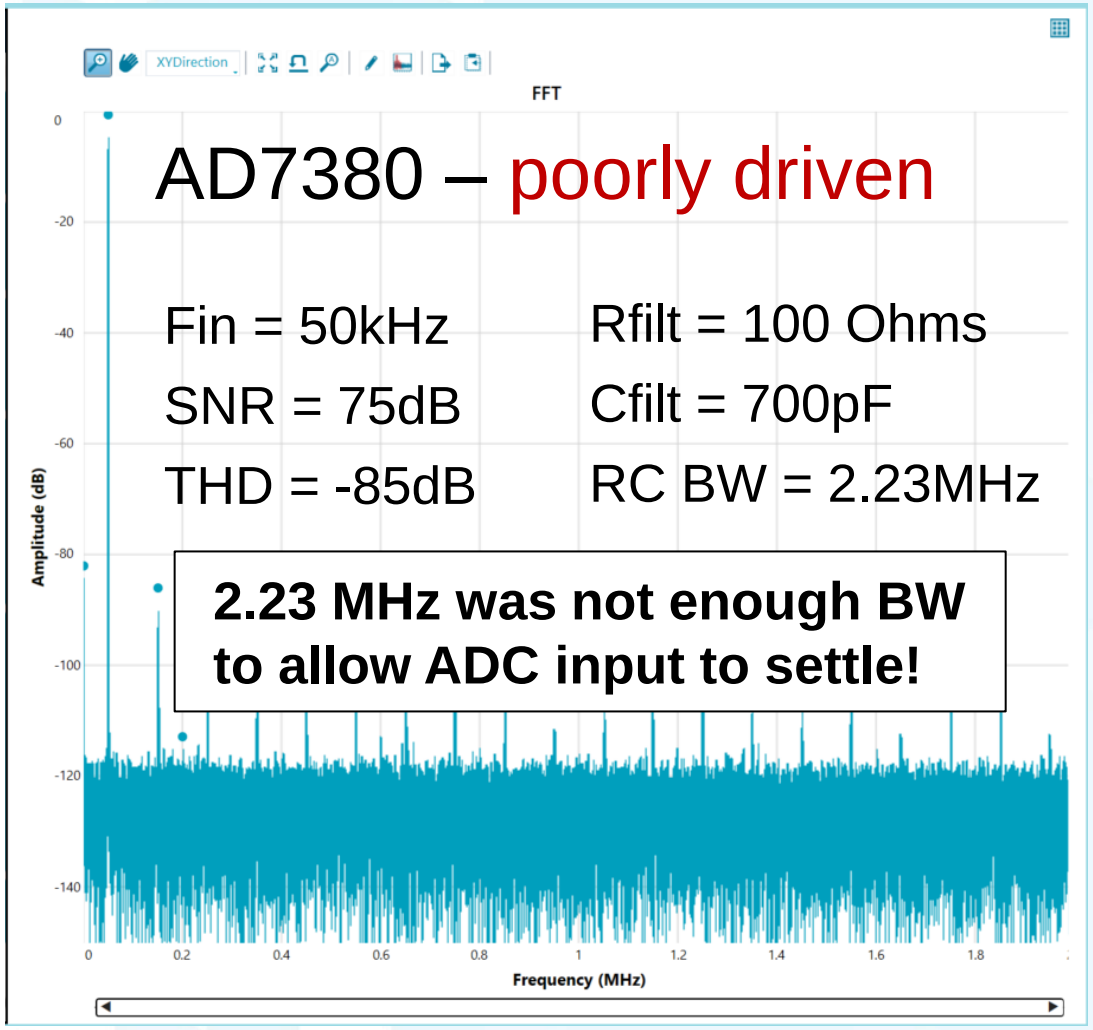


- Rfilt needed to isolate amp output from capacitive load
- Cfilt dampens the kickback, and combined with Rfilt, and provides filtering of noise from the driver
- Remember – **this is not an anti-aliasing filter** – the BW of this RC is usually much higher than Nyquist



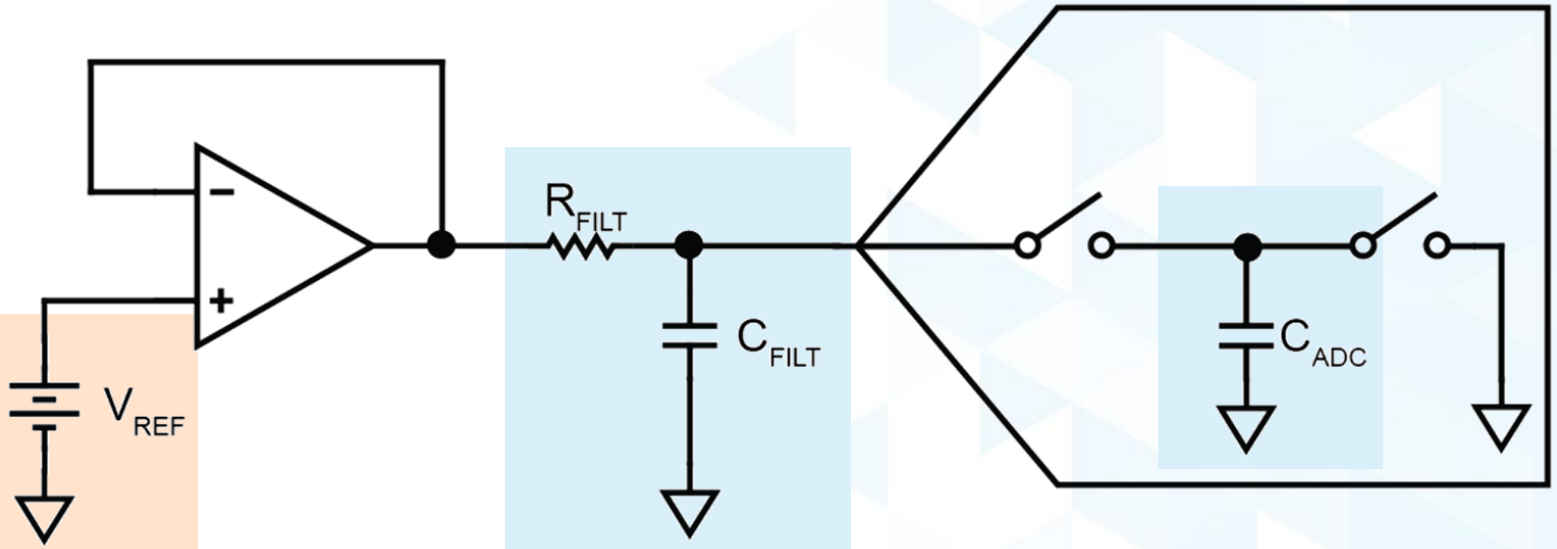
Consequences of not settling





Quantifying the kickback and settling time

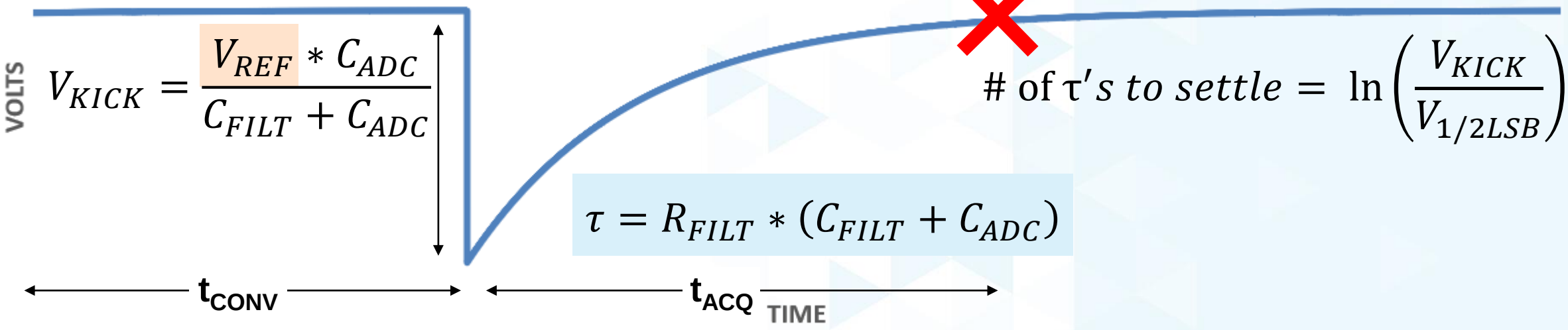
Driving full scale is the worst case scenario



$$V_{KICK} = \frac{V_{REF} * C_{ADC}}{C_{FILT} + C_{ADC}}$$

$$\tau = R_{FILT} * (C_{FILT} + C_{ADC})$$

$$\#\ \text{of}\ \tau's\ to\ settle = \ln\left(\frac{V_{KICK}}{V_{1/2LSB}}\right)$$



Links to learn more about the theory

- Driving SAR ADCs Whiteboard Series: https://www.youtube.com/playlist?list=PLiwaj4qabLWwQX_6dzznaH8Sgr7q1_pAS
- Front-End Amplifier and RC Filter Design for a Precision SAR ADC: https://www.analog.com/en/analog-dialogue/articles/front-end-amp-and-rc-filter-design.html
- LTspice: Simulating SAR ADC Analog Inputs: https://www.analog.com/en/technical-articles/ltspice-simulating-sar-adc-analog-inputs.html
- LTspice: SAR ADC Driver Interface: https://www.analog.com/en/technical-articles/10-ltspice-simulating-a-sar-adc-driver-interface.html

Quicker experimentation with online tool

ADC LTC2378-20

Sample Rate:	1M	SPS
Vref:	5	V

For LTC2378-20, maximum sample rate is 1MSPS and maximum voltage for Vref is 5.1V

Driver LT6200

Follower

Gain	1	V/V
Rf:	0	Ω
+Vs	6	V
-Vs	-900m	V

Input

Differential

Frequency	2k	Hz

☐ Input will be multiplexed

Filter

Rext:	10	Ω
Cext:	3.3n	F

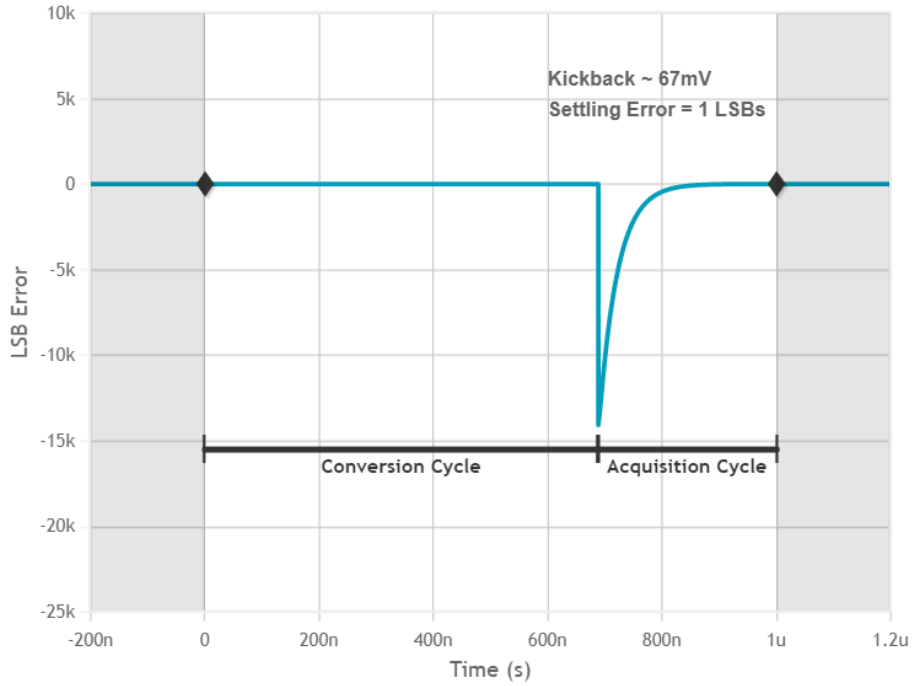
ADC Input Setting Summary

ADC Sample Period:	1 us
ADC Conversion Time:	688 ns
ADC Acquisition Time:	312 ns
RC Filter Bandwidth:	4.76 MHz
1 LSB:	9.54 uV

DC Input Signal

Time Domain Simulation - DC Input Signal

LSB Error | PPM Error | Volts



tools.analog.com/en/adcdriver

What it can look like when RC BW too low

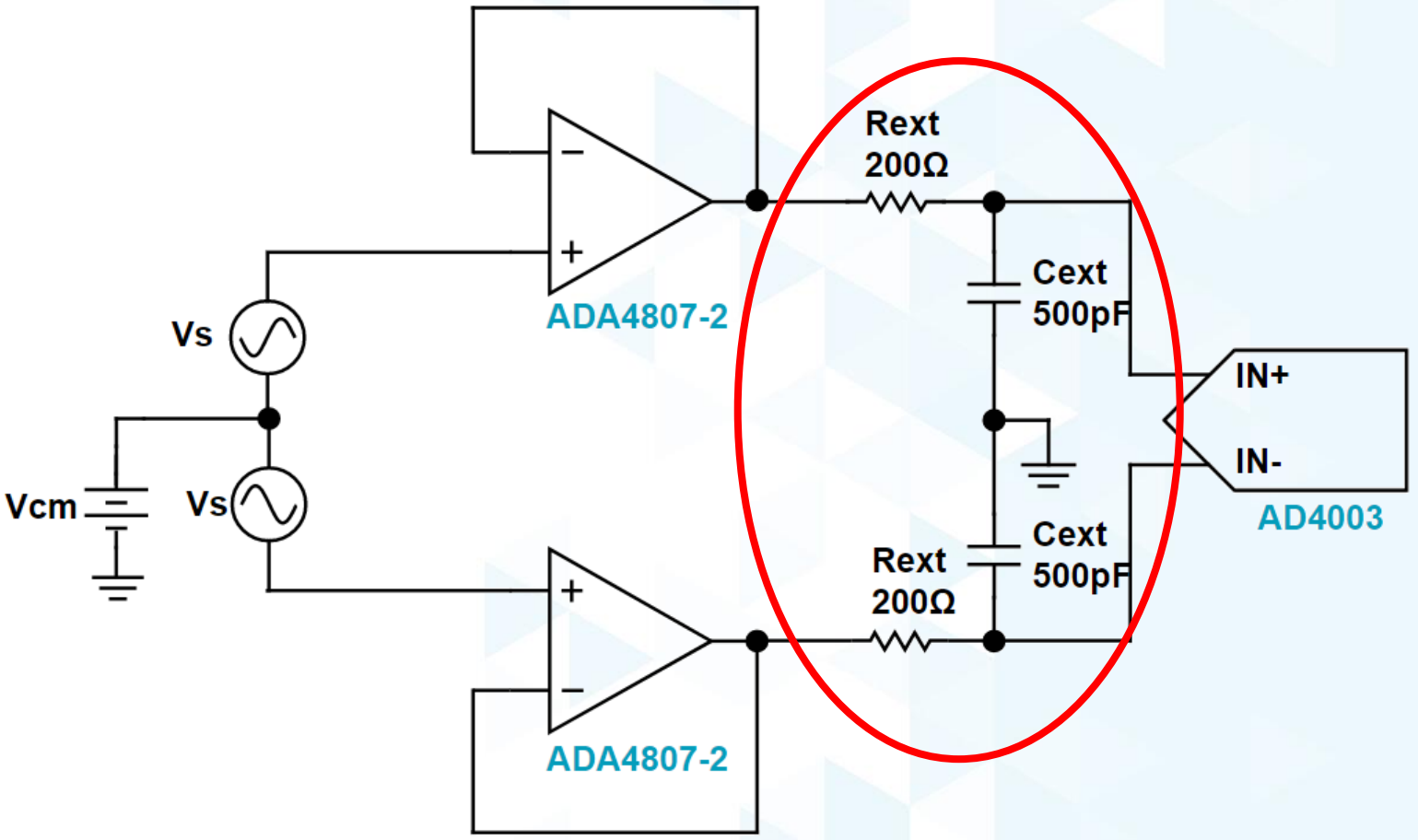
ADC	AD4003
Sample Rate:	2M SPS
Vref:	5 V
Enable high-Z mode	

For AD4003, maximum sample rate is 2MSPS and maximum voltage for Vref is 5.1V

Driver	ADA4807-2
Follower	
Gain	1 V/V
Rf:	0 Ω
+Vs	5.6 V
-Vs	-600m V

Input	
Differential	
Frequency	1k Hz
Input will be multiplexed	

Filter	
Rext:	200 Ω
Cext:	500p F



bit.ly/ADCDriver-lowRC-AD4003

What it can look like when RC BW too low

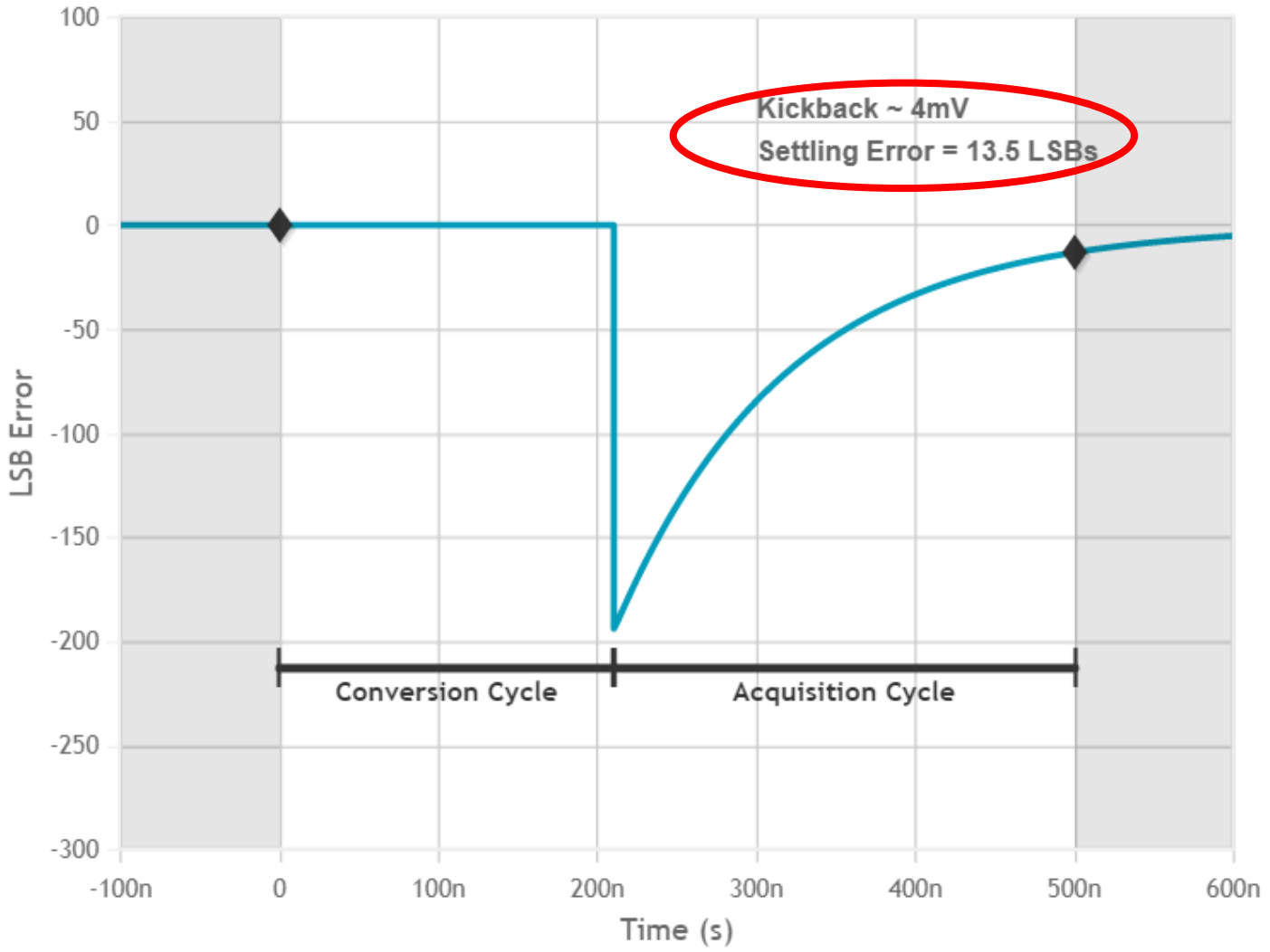
ADC	AD4003
Sample Rate:	2M SPS
Vref:	5 V
Enable high-Z mode	

For AD4003, maximum sample rate is 2MSPS and maximum voltage for Vref is 5.1V

Driver	ADA4807-2
Follower	
Gain	1 V/V
Rf:	0 Ω
+Vs	5.6 V
-Vs	-600m V

Input	
Differential	
Frequency	1k Hz
Input will be multiplexed	

Filter	
Rext:	200 Ω
Cext:	500p F



ADC Input Setting Summary	
ADC Sample Period:	500 ns
ADC Conversion Time:	210 ns
ADC Acquisition Time:	290 ns
RC Filter Bandwidth:	1.47 MHz

DC input settling: The bandwidth of the RC filter is too low, the ADC input will not be able to settle from the charge kickback before the ADC switches to conversion mode. View the settling error in the DC Input Signal plot, and increase the BW of the RC filter or lower the sample rate to resolve this error. See help topics in DC Input Signal tab and Filter settings for more information.

1 LSB:	38.1 uV

Noise and Distortion Summary	
THD @ 1 kHz:	-105 dB
ENOB @ 1 kHz:	16.2 bits
SINAD @ 1 kHz:	99.1 dB
SNR:	100.3 dB
System Noise:	34.3 uVrms

Driver Noise Contribution = 6.67 uVrms

THD estimate includes distortion caused by insufficient settling of the ADC kickback prior to acquisition. See the Input Settling tab for tips to resolve this issue.

What it can look like when RC BW too low

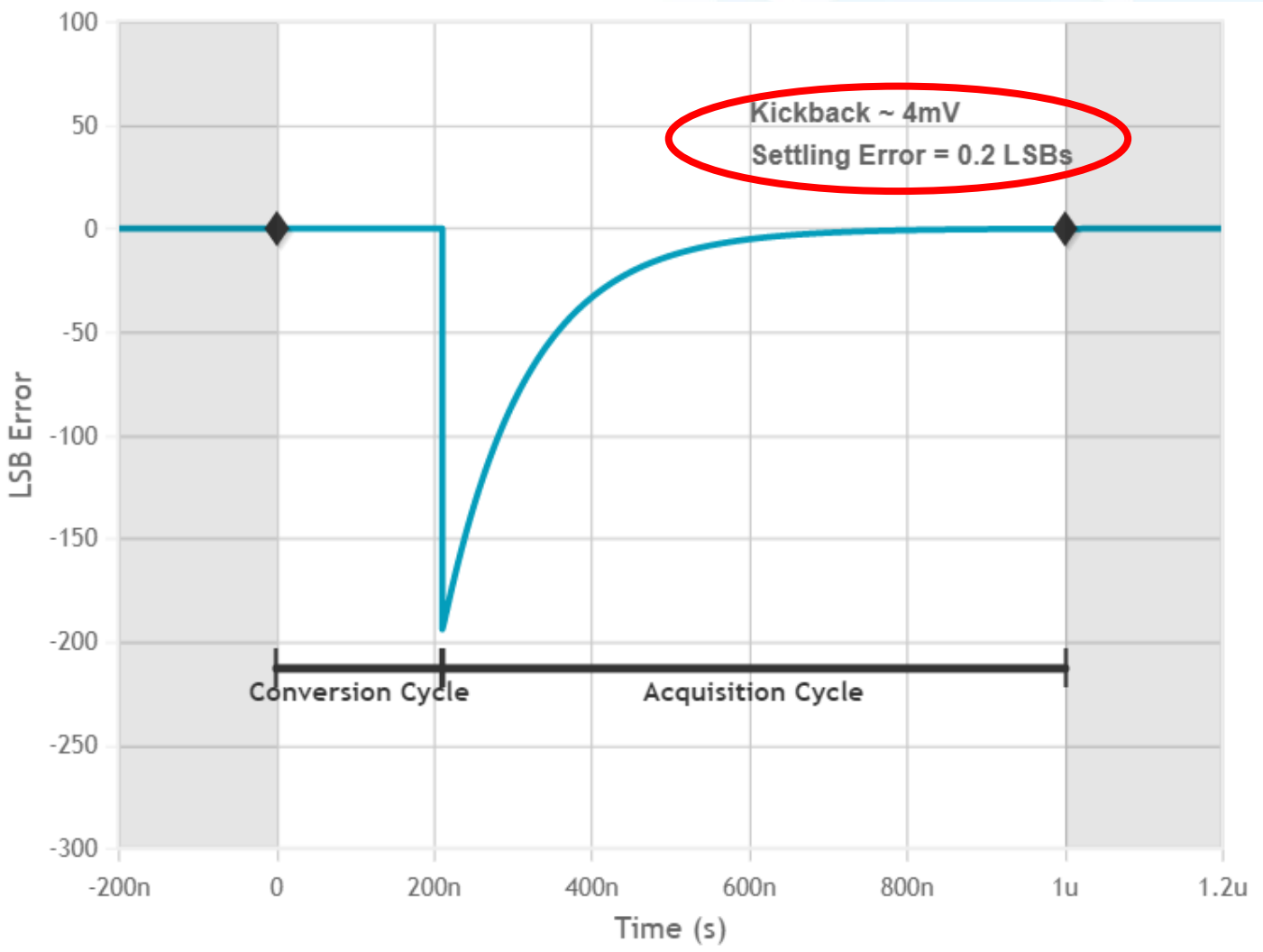
ADC	AD4003
Sample Rate:	1M SPS
Vref:	5 V
Enable high-Z mode	

For AD4003, maximum sample rate is 2MSPS and maximum voltage for Vref is 5.1V

Driver	ADA4807-2
Follower	
Gain	1 V/V
Rf:	0 Ω
+Vs	5.6 V
-Vs	-600m V

Input	
Differential	
Frequency	1k Hz
Input will be multiplexed	

Filter	
Rext:	200 Ω
Cext:	500p F

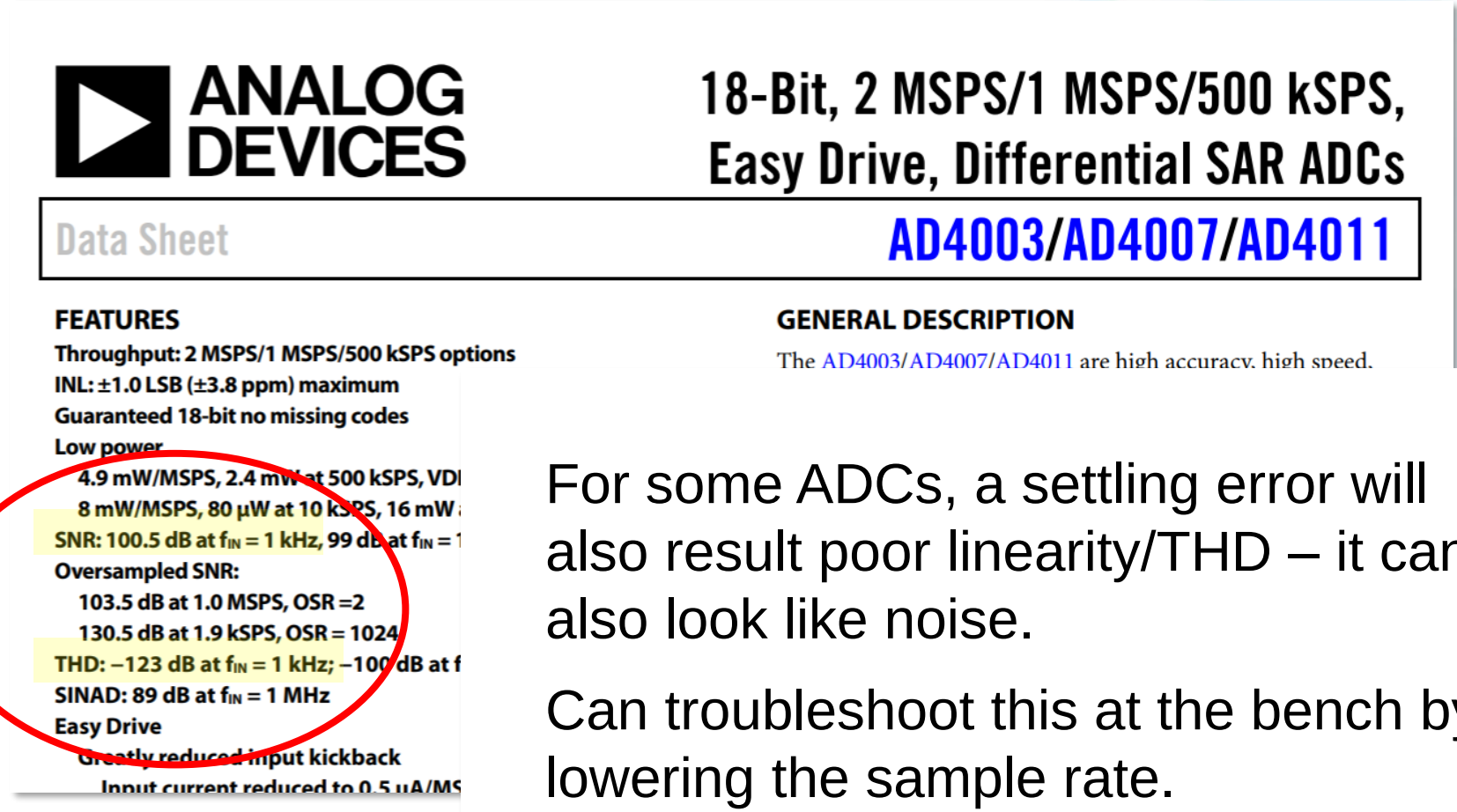


ADC Input Setting Summary	
ADC Sample Period:	1 us
ADC Conversion Time:	210 ns
ADC Acquisition Time:	790 ns
RC Filter Bandwidth:	1.47 MHz
1 LSB:	38.1 uV

Noise and Distortion Summary	
THD @ 1 kHz:	-123 dB
ENOB @ 1 kHz:	16.4 bits
SINAD @ 1 kHz:	100 dB
SNR:	100.3 dB
System Noise:	34.3 uVrms

Driver Noise Contribution = 6.67 uVrms

What it can look like when RC BW too low



ANALOG DEVICES

18-Bit, 2 MSPS/1 MSPS/500 kSPS, Easy Drive, Differential SAR ADCs

Data Sheet AD4003/AD4007/AD4011

FEATURES

Throughput: 2 MSPS/1 MSPS/500 kSPS options
INL: ±1.0 LSB (±3.8 ppm) maximum
Guaranteed 18-bit no missing codes
Low power
4.9 mW/MSPS, 2.4 mW at 500 kSPS, VDI
8 mW/MSPS, 80 µW at 10 kSPS, 16 mW
SNR: 100.5 dB at f_{IN} = 1 kHz, 99 dB at f_{IN} = 1
Oversampled SNR:
103.5 dB at 1.0 MSPS, OSR =2
130.5 dB at 1.9 kSPS, OSR = 1024
THD: −123 dB at f_{IN} = 1 kHz; −100 dB at f
SINAD: 89 dB at f_{IN} = 1 MHz
Easy Drive
Greatly reduced input kickback
Input current reduced to 0.5 µA/MS

GENERAL DESCRIPTION

The AD4003/AD4007/AD4011 are high accuracy, high speed,

For some ADCs, a settling error will also result poor linearity/THD – it can also look like noise.

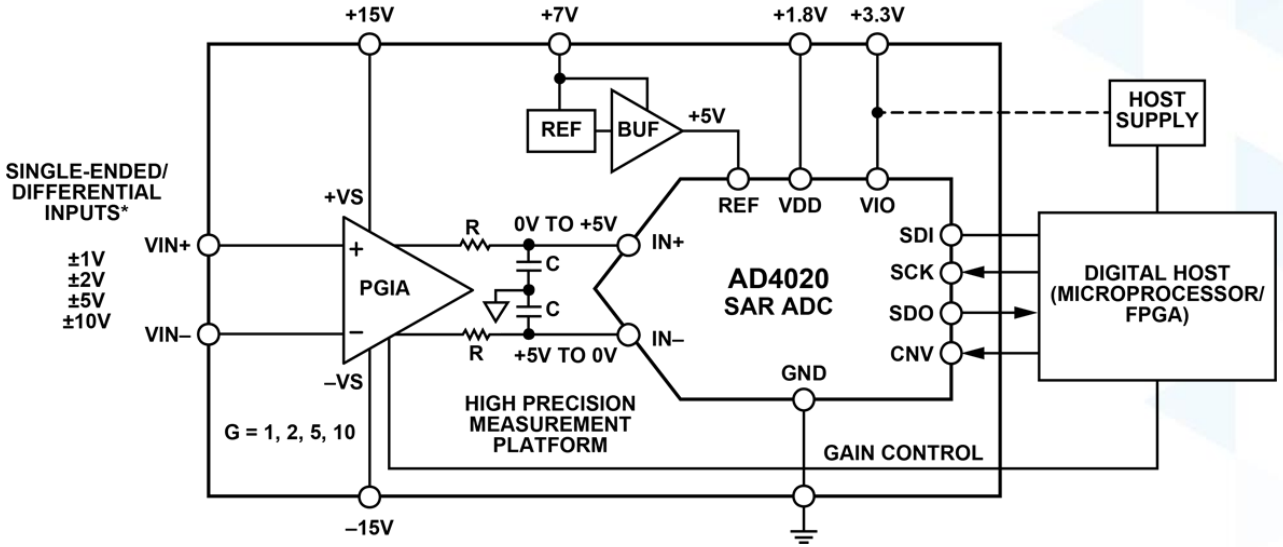
Can troubleshoot this at the bench by lowering the sample rate.

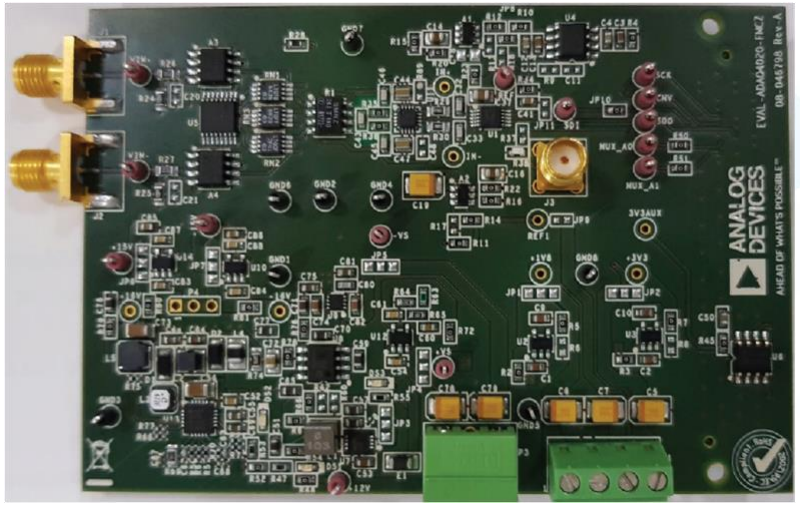
ADC Input Setting Summary	
ADC Sample Period:	1 us
ADC Conversion Time:	210 ns
ADC Acquisition Time:	790 ns
RC Filter Bandwidth:	1.47 MHz
1 LSB:	38.1 uV

Noise and Distortion Summary	
THD @ 1 kHz:	-123 dB
ENOB @ 1 kHz:	16.4 bits
SINAD @ 1 kHz:	100 dB
SNR:	100.3 dB
System Noise:	34.3 uVrms
Driver Noise Contribution = 6.67 uVrms	

Signal Chain Solutions

CN0513: High Accuracy 20-Bit Data Acquisition Solution





ANALOG DEVICES

Reference Design
CN-0513

Circuits from the Lab™ Reference Circuits

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0513.

Devices Connected/Referenced	
AD4020	20-Bit, 1.8 MSPS, Successive Approximation Register (SAR) ADC

20-Bit, 1.8 MSPS, ±2.5 ppm INL, Low Drift, High Accuracy Data Acquisition Solution

FEATURES

Data acquisition solution fully characterized over 0°C to 70°C
Guaranteed 20-bit no missing codes
INL: ±2 ppm, DNL: ±0.25 ppm
Throughput: 1.8 MSPS
Offset error drift: ±3.5 ppm/°C; gain error drift: ±6 ppm/°C
SNR: 98 dB at G = 1, 92 dB at G = 10, f_{IN} = 1 kHz
THD: −120 dB at G = 1, −116 dB at G = 10, f_{IN} = 1 kHz
Oversampled dynamic range: 102 dB at 900 kSPS, OSR = 2
Software programmable bipolar input ranges (±1 V to ±10 V)
Allows single-ended and differential signals
CMRR: 92 dB typical
GΩ input impedance allows direct interface with sensors
Ease of use features reduce system power and complexity
ADC input overvoltage clamp protection sinks up to 50 mA
On-board 5 V reference and buffer
First conversion accurate, no latency/pipeline delay
Fast conversion time allows low SPI clock rates
SPI-/QSPI-/MICROWIRE-/DSP-compatible serial interface

APPLICATIONS

Data acquisition and system monitoring
Automated test equipment
Instrumentation
Medical equipment

REFERENCE DESIGN SOLUTION

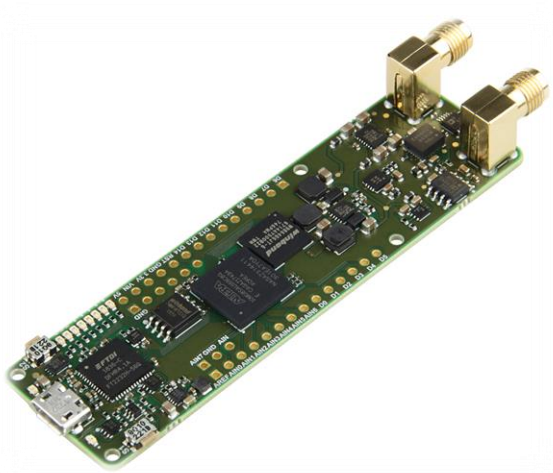
System designers developing data acquisition signal chains typically require high input impedance to allow direct interface with a variety of sensors, which could have varying common-mode voltages and unipolar or bipolar single-ended or differential input signals present. The majority of the instrumentation and programmable gain instrumentation amplifiers (PGIAs) are traditionally single-ended output that cannot directly drive a fully differential, high resolution, successive approximation register (SAR) analog-to-digital converter (ADC), and require at least one signal conditioning/driver stage. However, this approach may not always facilitate stringent high accuracy performance, namely, linearity, drift, and speed at desired input levels.

This reference design incorporates the unique discrete PGIA architecture of the Analog Devices, Inc., 20-bit, 1.8 MSPS SAR ADC AD4020, a 5 V reference, and a reference buffer with on-board power supply circuitry. This solution provides a fully characterized, validated design optimized for high precision, offering unprecedented linearity (±2 ppm typical INL), low offset/gain error drift, and trackable noise and distortion (beyond −115 dB) performance at full speed for all gain options over the 0°C to 70°C temperature range. The differential output PGIA uses off-the-shelf discrete components for digitally programmable gains that have GΩ input impedance, over 92 dB common-mode rejection ratio, low output noise, and low distortion, making it suitable for directly interfacing with various sensor types and driving a high throughput, high resolution SAR ADC without compromising performance.

For more information on how to test the AD4020-based high accuracy data acquisition solution, refer to UG-1280, and to obtain all design files contact Referencedesign@analog.com.

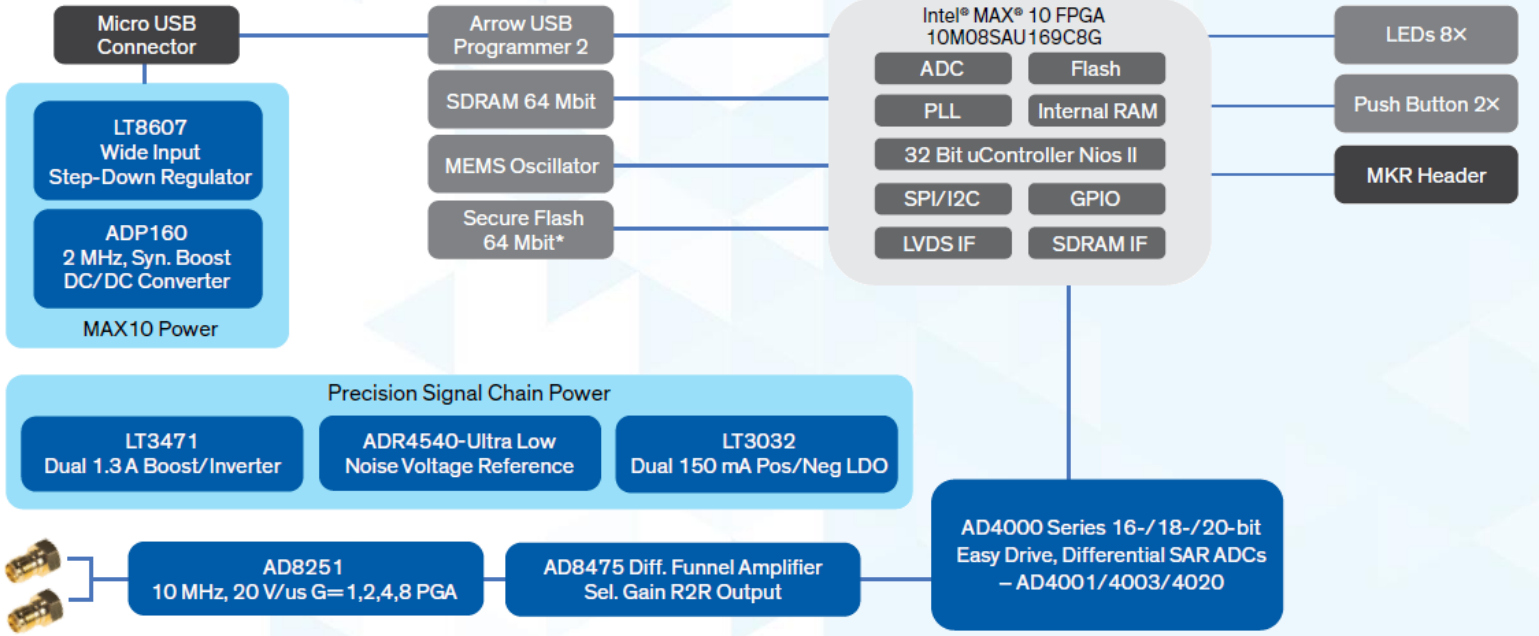
analog.com/CN0513

ANALOGMAX-DAQ1: High-Accuracy Programmable Data Acquisition Platform



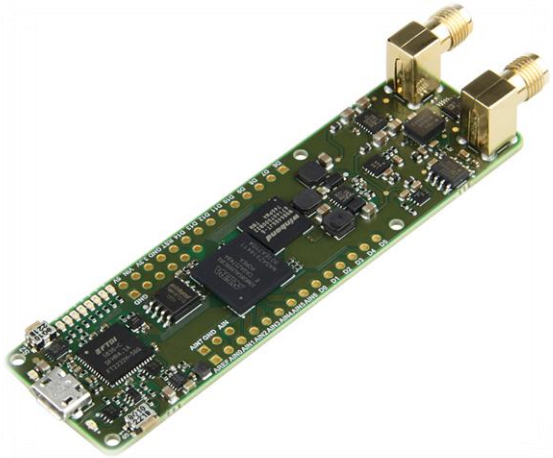
Five Years Out

trenz electronic



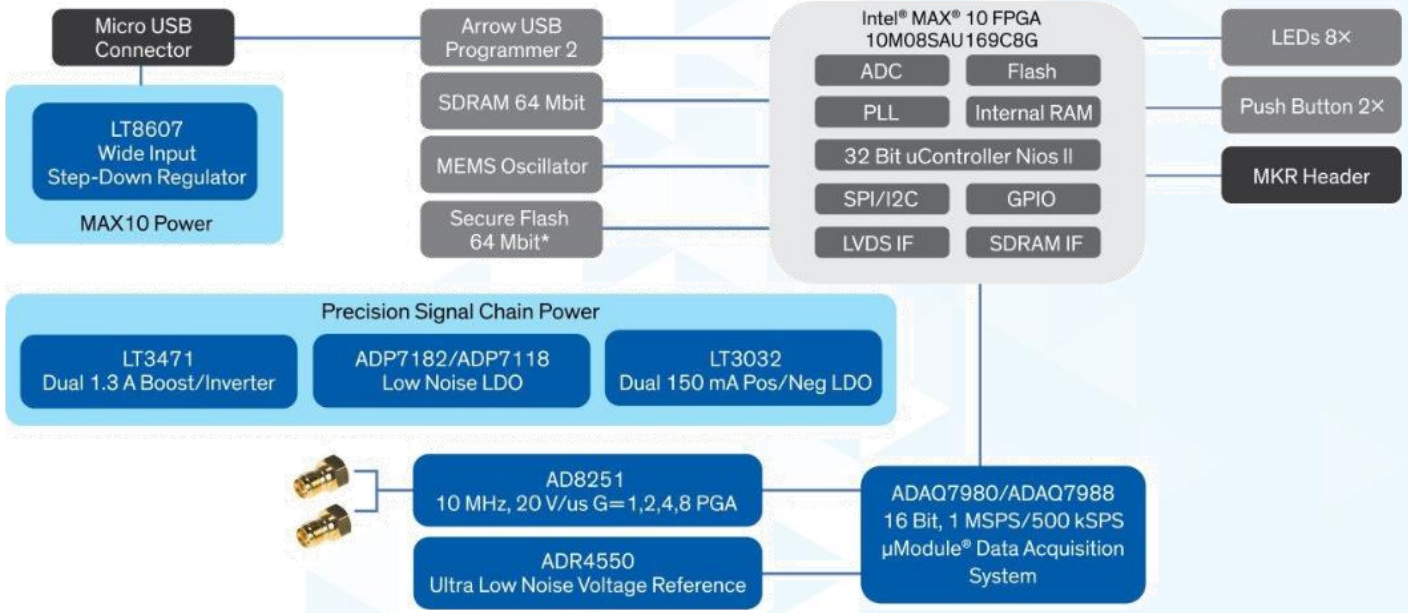
- High-accuracy analog front-end: Ideal for applications requiring accurate data capture at high throughputs
- Flexible platform: Based on the programmable Intel® MAX® 10 FPGA, easily adjusts to a wide range of use cases and production needs
- Rapid development and testing with an out-of-the-box experience that includes a Jupyter notebook demo with Python code
- Quick customization services: Add new functionality, lower BOM cost, or have the complete product designed

ANALOGMAX-DAQ2: Programmable 16-bit Data Acquisition Platform



Five Years Out

trenz electronic

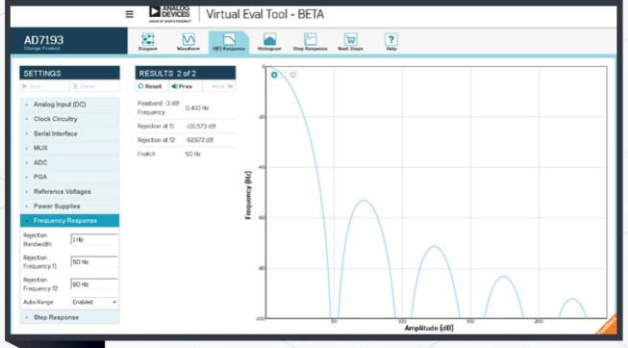


- Simplifies analog signal chain design: The level of integration in ADAQ7980/ADAQ7988 simplifies the development of high-accuracy data acquisition systems
- Flexible platform: Based on the programmable Intel® MAX® 10 FPGA, easily adjusts to a wide range of use cases and production needs
- Rapid development and testing with an out-of-the-box experience that includes a Jupyter notebook demo with Python code
- Quick customization services: Add new functionality, lower BOM cost, or have the complete product designed

Design Tools

Virtual Eval

Accelerate precision ADC product selection and evaluation with Virtual Eval—from configuring operating conditions to simulating crucial part performance characteristics within seconds.

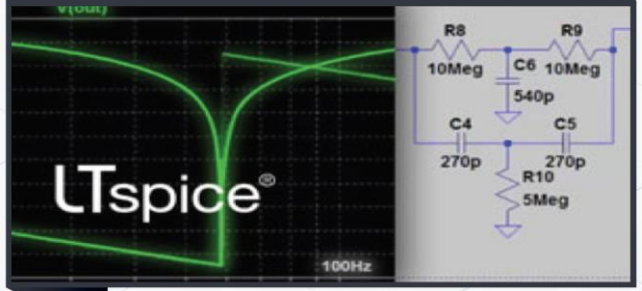


Visit beta-tools.analog.com/virtualeval

LTspice

Generate LTspice® schematics from Filter Wizard, Photodiode Wizard, or the Precision ADC Driver Tool. The LTspice library now includes:

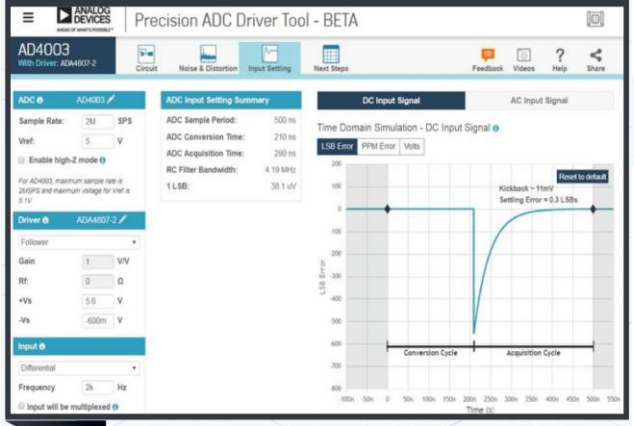
- SAR ADC models AD4002, AD4003, LTC2311, LTC2323, LTC2325
- ADG switch and multiplexer models
- DAC model AD5766



Visit analog.com/ltspice

Precision ADC Driver Tool

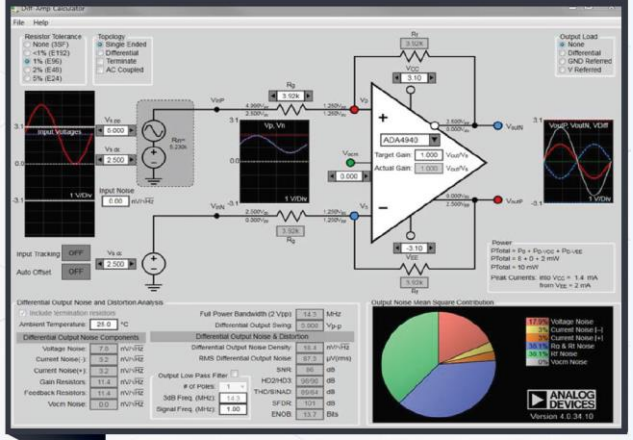
Quickly determine the impact of the driver and RC filter on performance of an ADC signal chain in a specialized simulation environment. Potential issues with driver selection, kickback settling, and distortion are flagged, and design trade-offs can be quickly evaluated.



Visit beta-tools.analog.com/adcdriver

DiffAmpCalc™

Reduce design time for differential amplifier circuits from hours to minutes by automating time-consuming calculations to determine gain, termination resistors, power dissipation, noise output, and input common-mode voltage range.



Visit analog.com/diffampcalc

Thank You For Watching!

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