전력무결성(Power Integrity) 테스트

With EXR 오실로스코프

2021. 01

(주)제이스 솔루션사업부

오정호 부장

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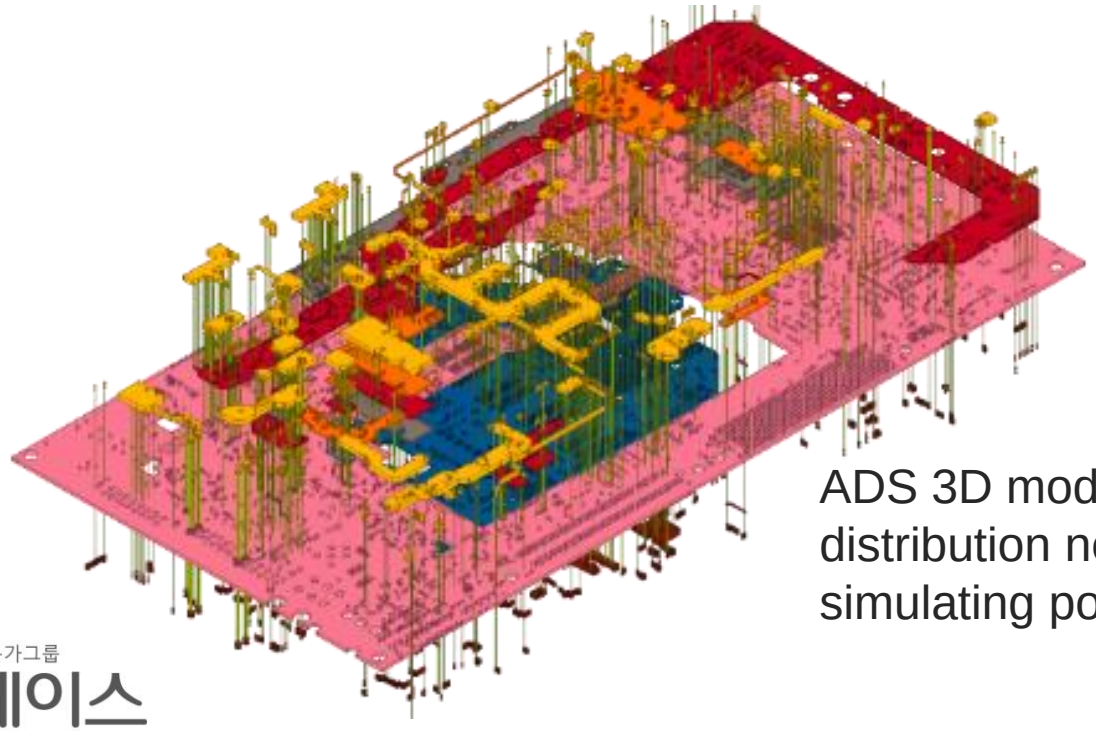
Power Integrity (PI)

What are we talking about

Power Integrity: The study of the conversion, delivery and consumption of DC power in an electronic system. *Kenny Johnson, Keysight*

Product Functional Reliability α Quality of the system power



ADS 3D model of power distribution network (PDN) for simulating power integrity

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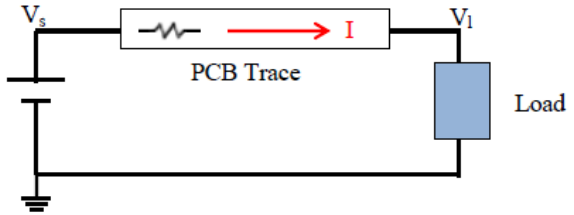
Power Delivery

균일한 파워 전달

- 모든 회로는 **동작을** 위해 파워를 공급받아야 한다. 모든 조건에서 안정적인 파워를 노이즈 없이 공급하는 것은 쉽지 않은 문제가 될 수 있다.

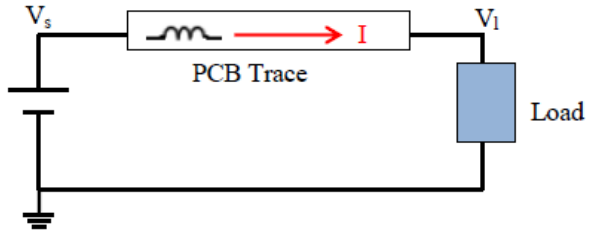
- 1. DC 관점의 파워 공급 : PCB 트레이스에DC 전류가 흐르면 트레이스 양단 사이의 저항 R 에 의해 V=IR 만큼의 전압 강하가 발생.

$$V_l = V_s - IR$$



- 2. AC 관점의 파워 공급 : Load에 빠르게 변화하는 전류 흐름이 있게 되면, PCB 트레이스의 L에 의해 L*dI/dt 만큼의 전압 강하가 발생하게 된다.

$$V_l = V_s - L\frac{dI}{dt}$$



- Summary: power supply source와 load사이의 inductance는 supply voltage의 fluctuation을 만든다.

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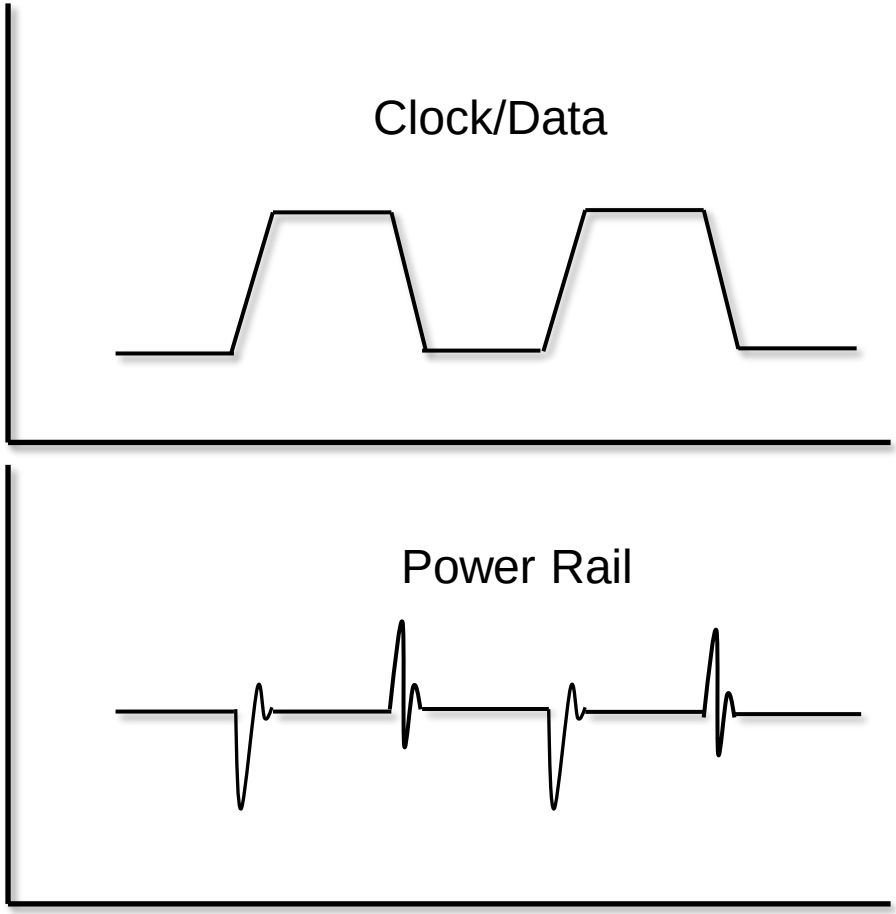
Power Integrity

DC전원: Switching loads 때문에 DC문제만 아니다



Switching loads can cause high frequency supply noise with content easily exceeding 1GHz

Power rails must be stable from DC to the BW of the switching current

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Power/Ground Plane Noise

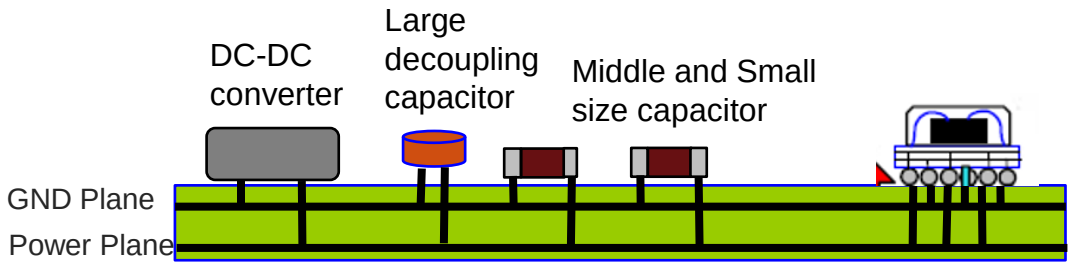
파워와 그라운드 사이의 임피던스

– Power ground plane에서 rail collapse 노이즈는 전류 변화에 대해 power ground의 임피던스가 곱해져서 생긴다. 전류 변화는 칩의 동작에 의해 결정되는 것으로 바꿀 수 없으므로, PCB 상에서 power ground 임피던스를 줄여서 노이즈를 줄이는 것이 필요하다.

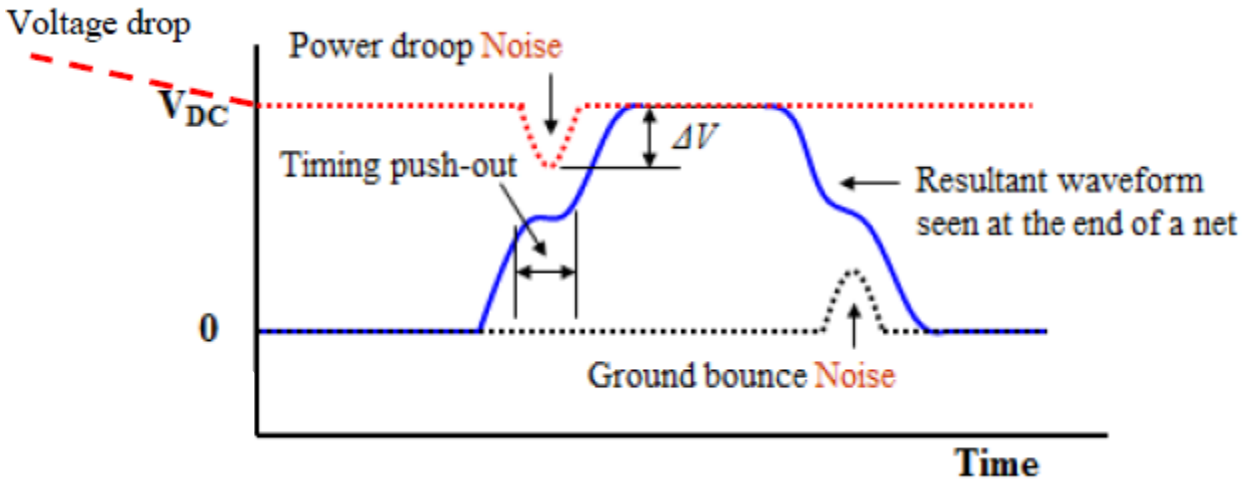
– 1. Power and Ground Bounce

$$\Delta V = Z \bullet \Delta I$$

Target to Reduce by
- Stack-up
- De-cap Mount Pad
- Plane Design



2. Target Impedance
전압 리플 허용 값이 정해지면 전류와의 관계에 의해 임피던스 최대 허용치가 결정되는데 이를 target impedance 라고 한다.



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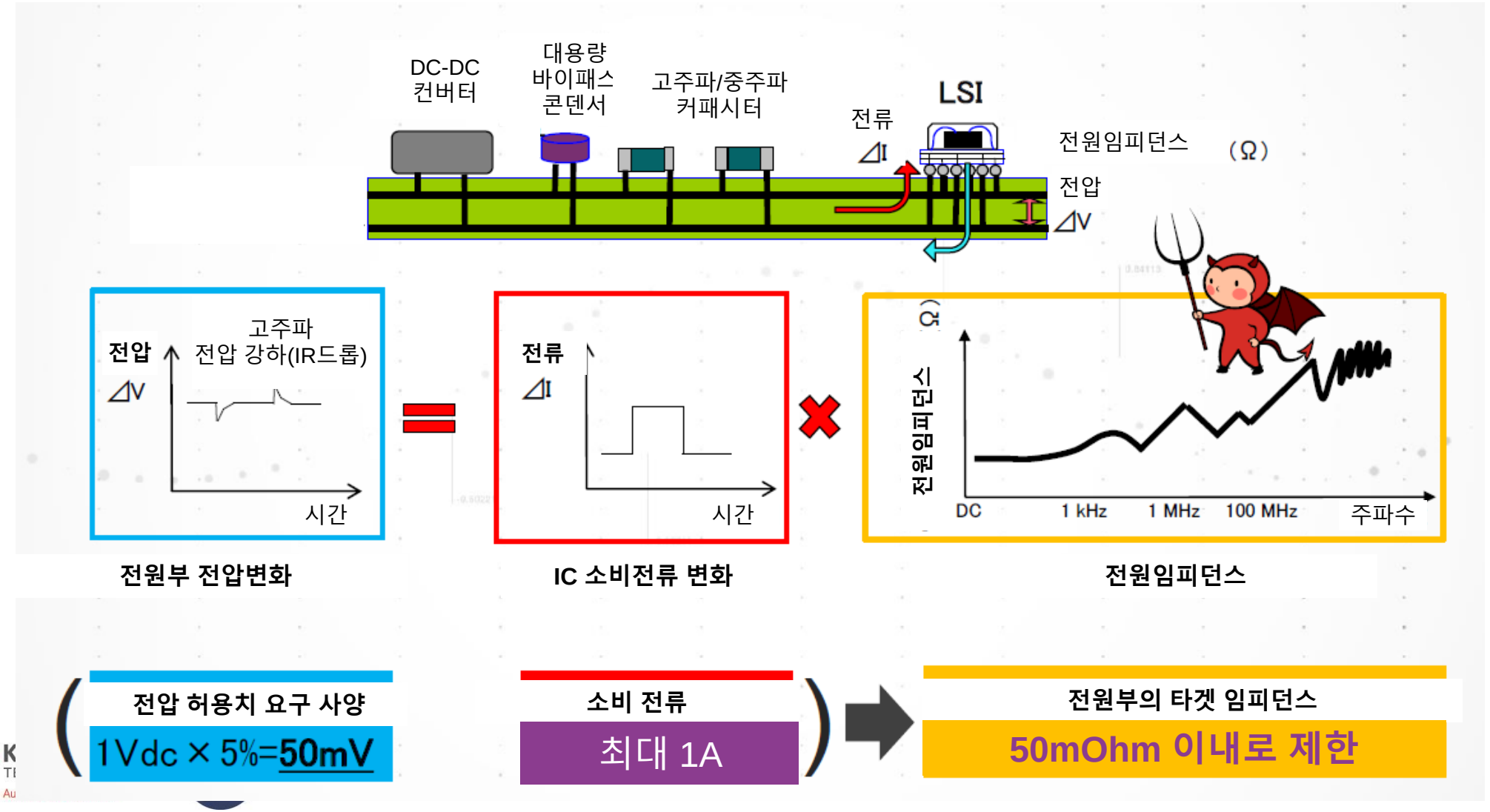
Target Impedance

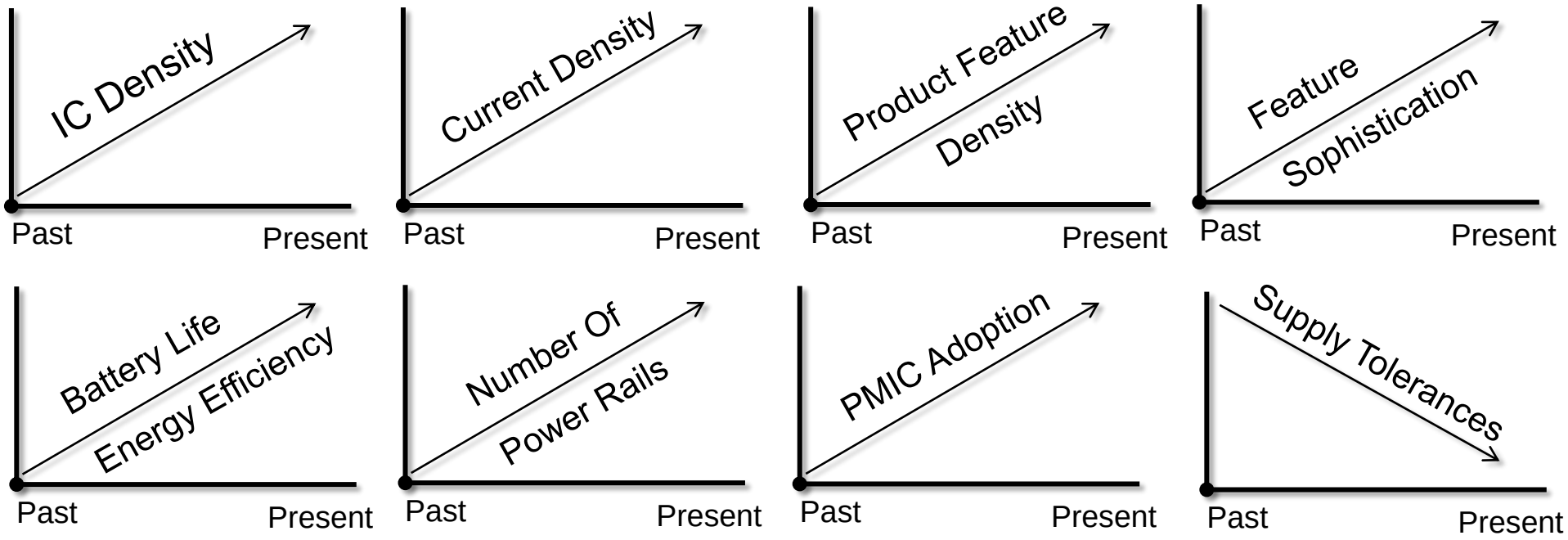
전원 임피던스의 콘트롤이 중요해지는 이유



Power Integrity

왜 점점 중요해지는가요?

– Moore's Law: transistors on an integrated circuit will double every two years.



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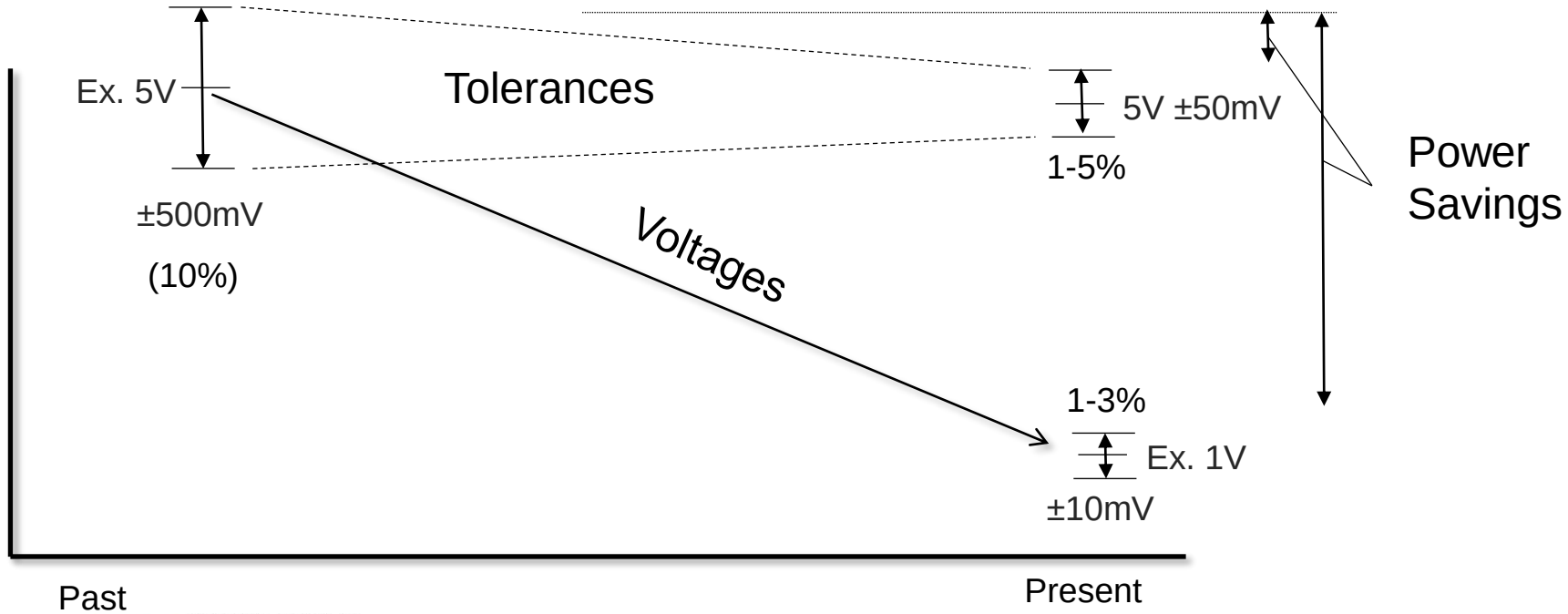
Why? Power and current density

– Operating voltages are decreasing to reduce power—this requires tighter rail tolerances.



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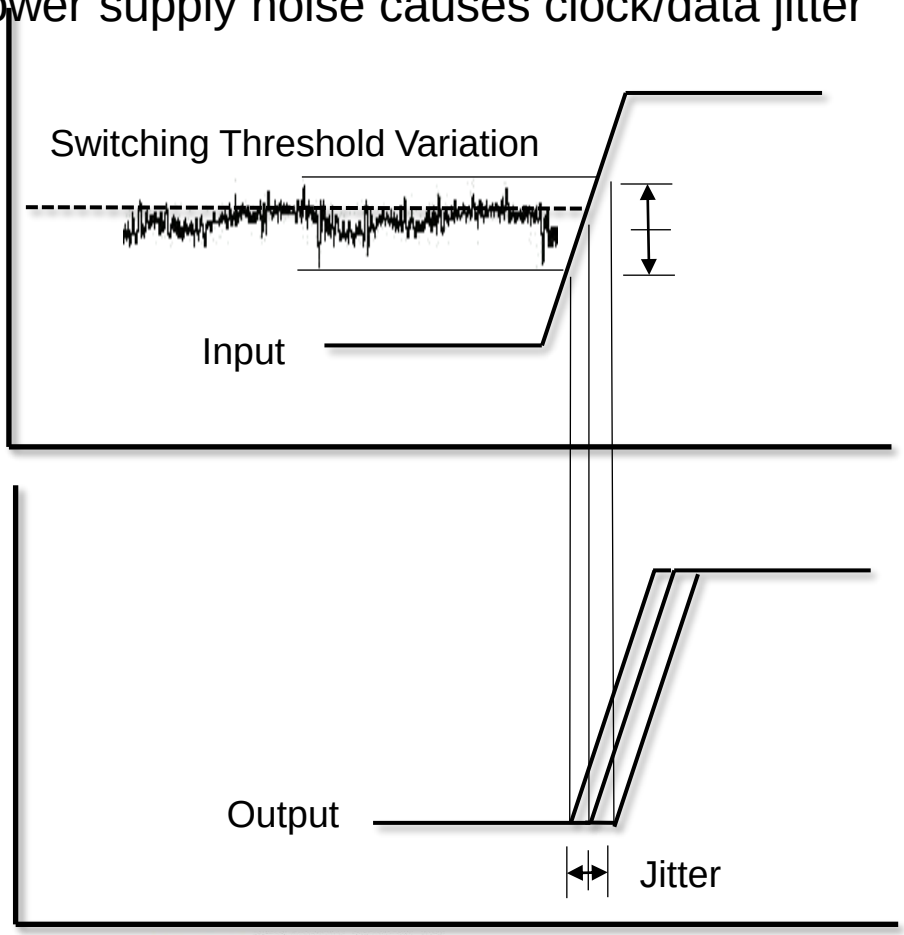
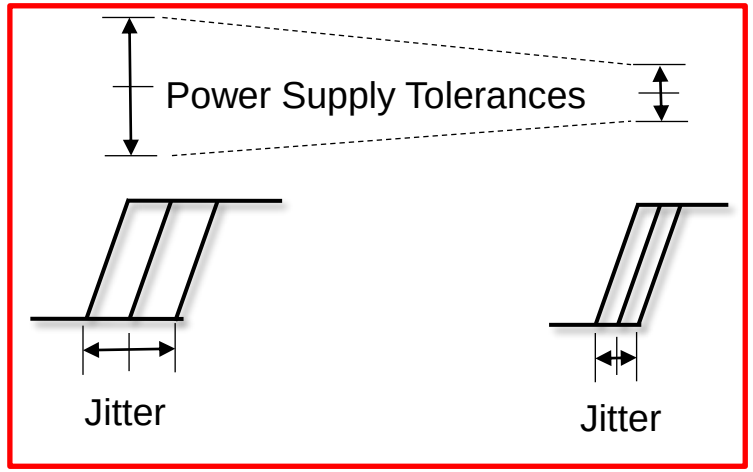
WhY? Power Supply induced jitter (PSIJ)

– Power supply noise causes clock/data jitter

Example 1:





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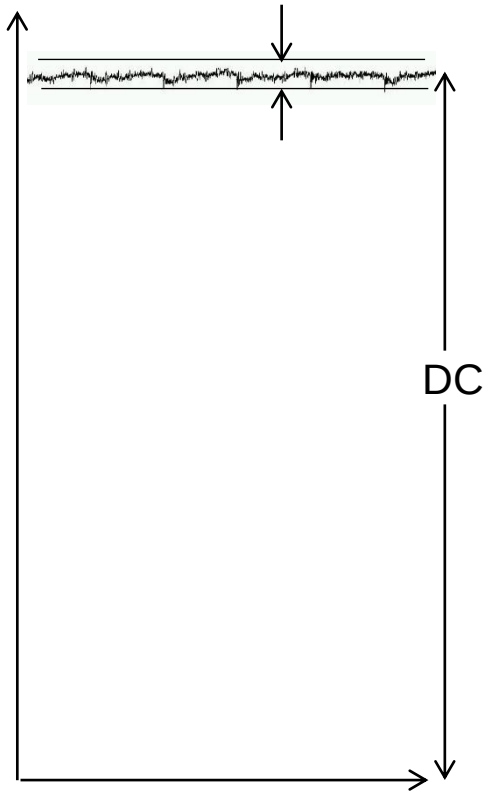
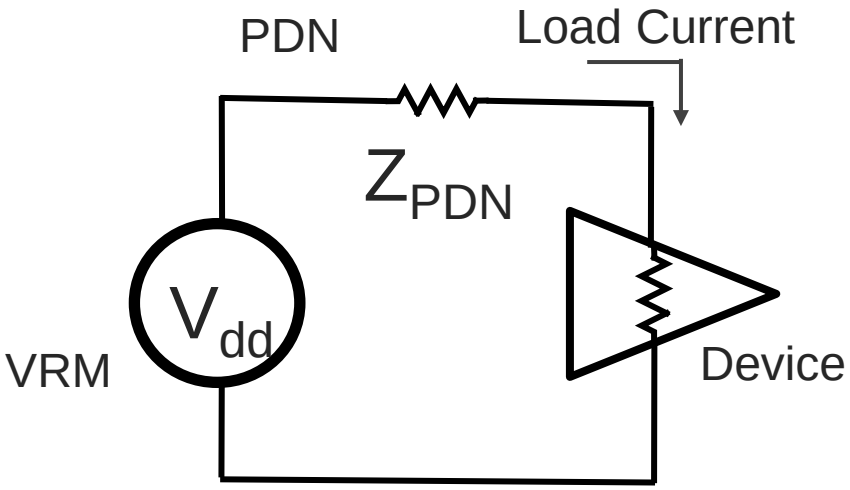
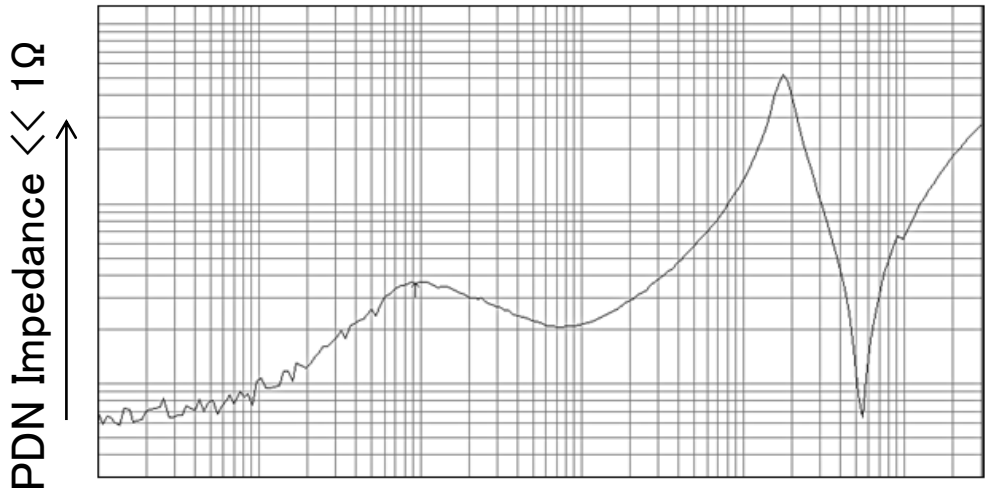
Power Integrity

Pdn(power distribution network) theory and modeling







$$Z_{target}(f) = Z_{PDN}(f) < \frac{V_{Ripple}}{I(f)}$$

$$I_{transient} \sim (1/2)*I_{max}$$

$$I_{peak} = P_{max}/V_{dd} \rightarrow Z_{target}(f) = \frac{2*(V_{dd})^2*(ripple\%)}{P_{max}}$$

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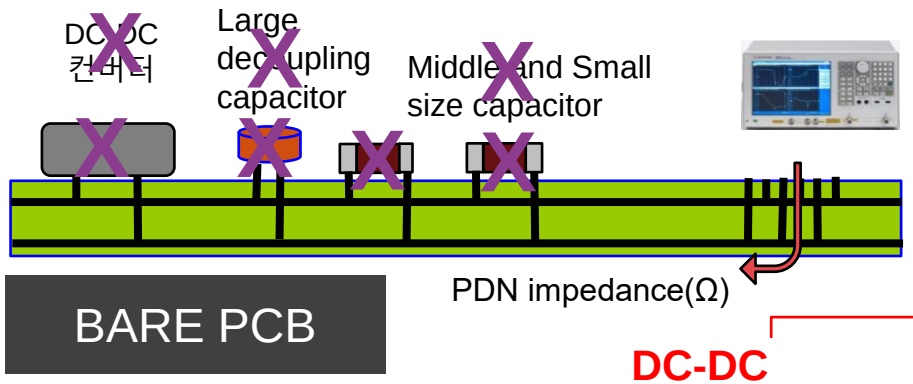
Power Integrity

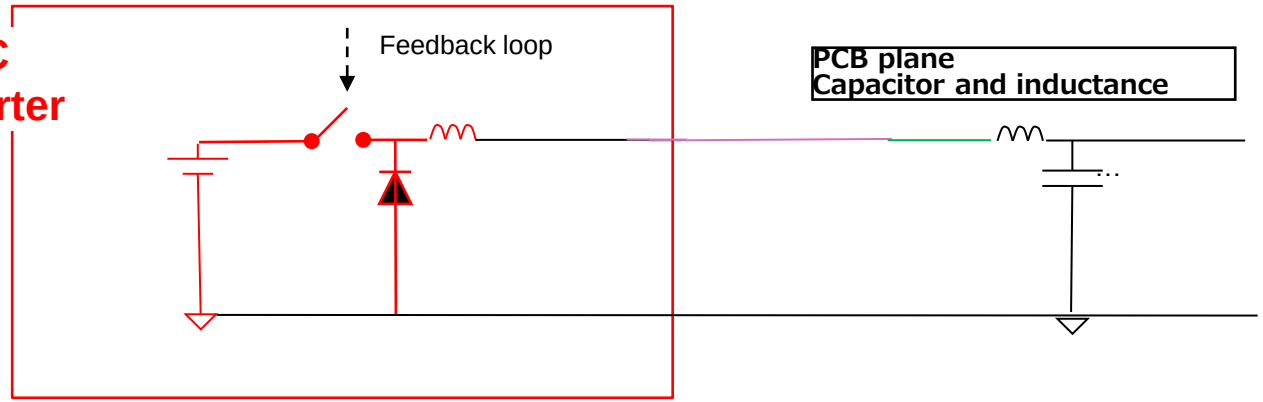
PDN 임피던스의 해석



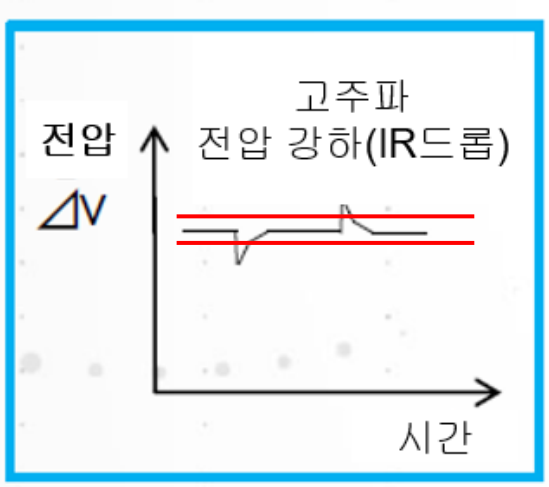
BARE PCB

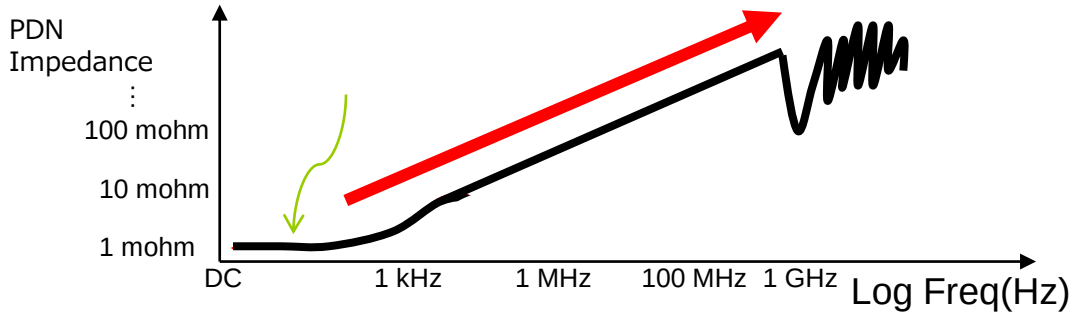
PDN impedance measurement at IC position.

DC-DC converter



PDN impedance measurement at IC position.





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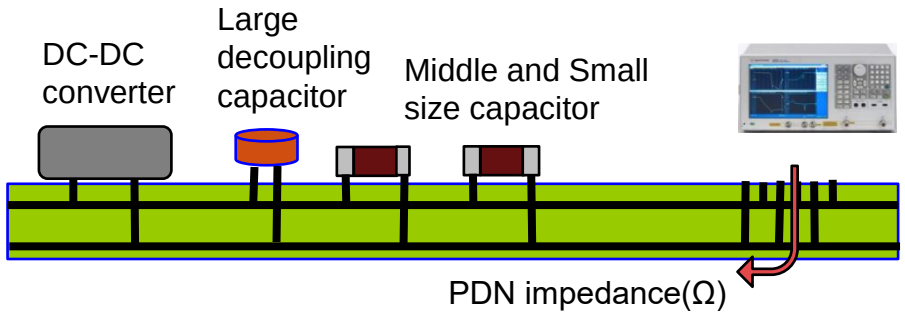
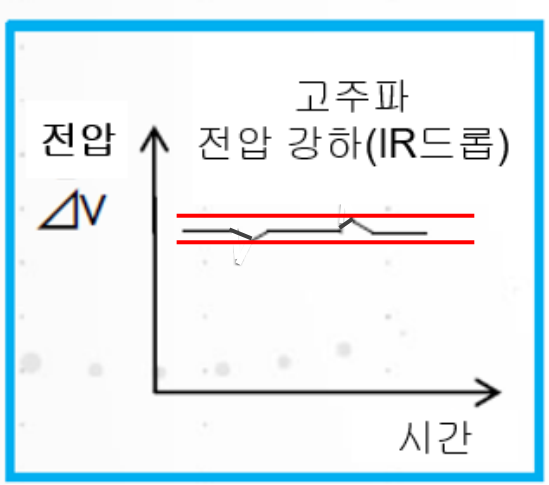
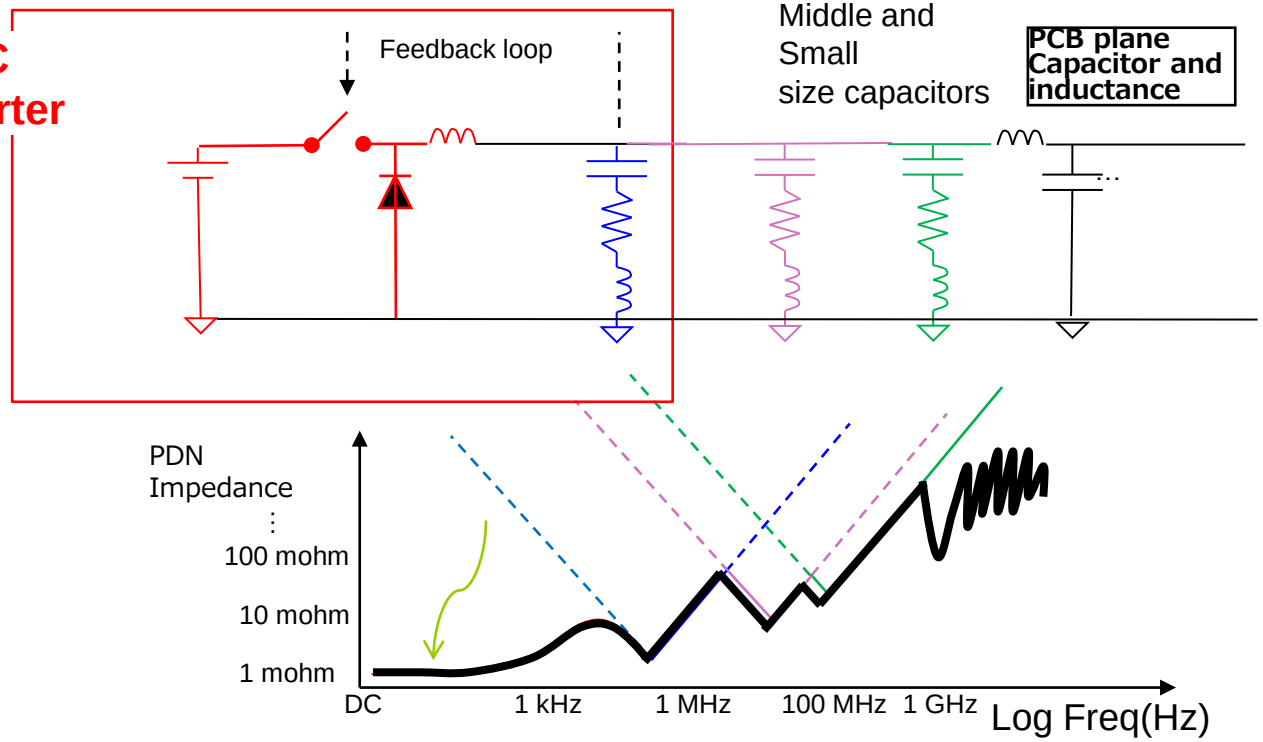
Power Integrity

PDN 임피던스의 해석



PDN impedance measurement at IC position.





PDN impedance measurement at IC position.

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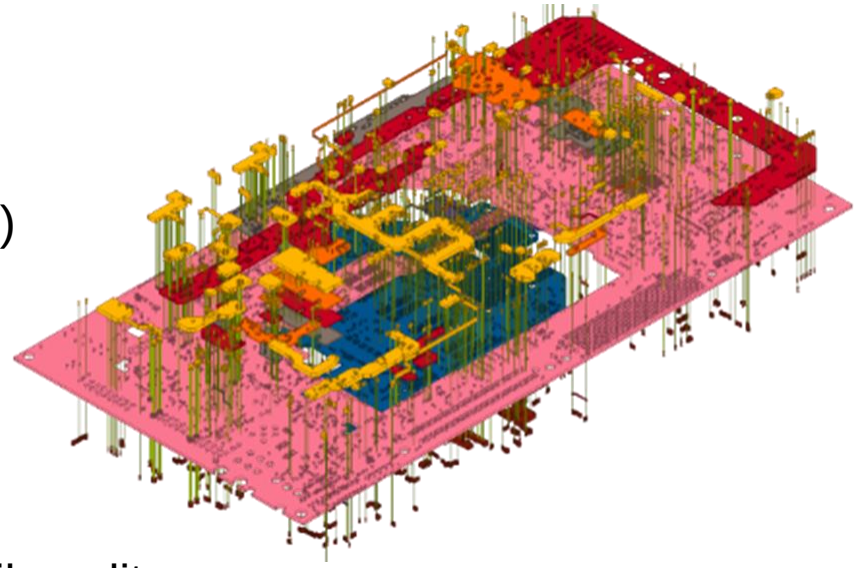
Power Integrity

PDN을 잘 디자인 하면...

– A well designed PDN will maintain a stable voltage (within tolerance) from DC to the bandwidth of the switching current (typically above 1GHz).

– This will help:

- Optimize power consumption
- Minimize switching noise (SSN—simultaneous switching noise)
- Reduce PSIJ (dropped bits, missed clock …)
- Minimize EMI problems



– Therefore, one the primary validation tasks is measuring power rail quality.

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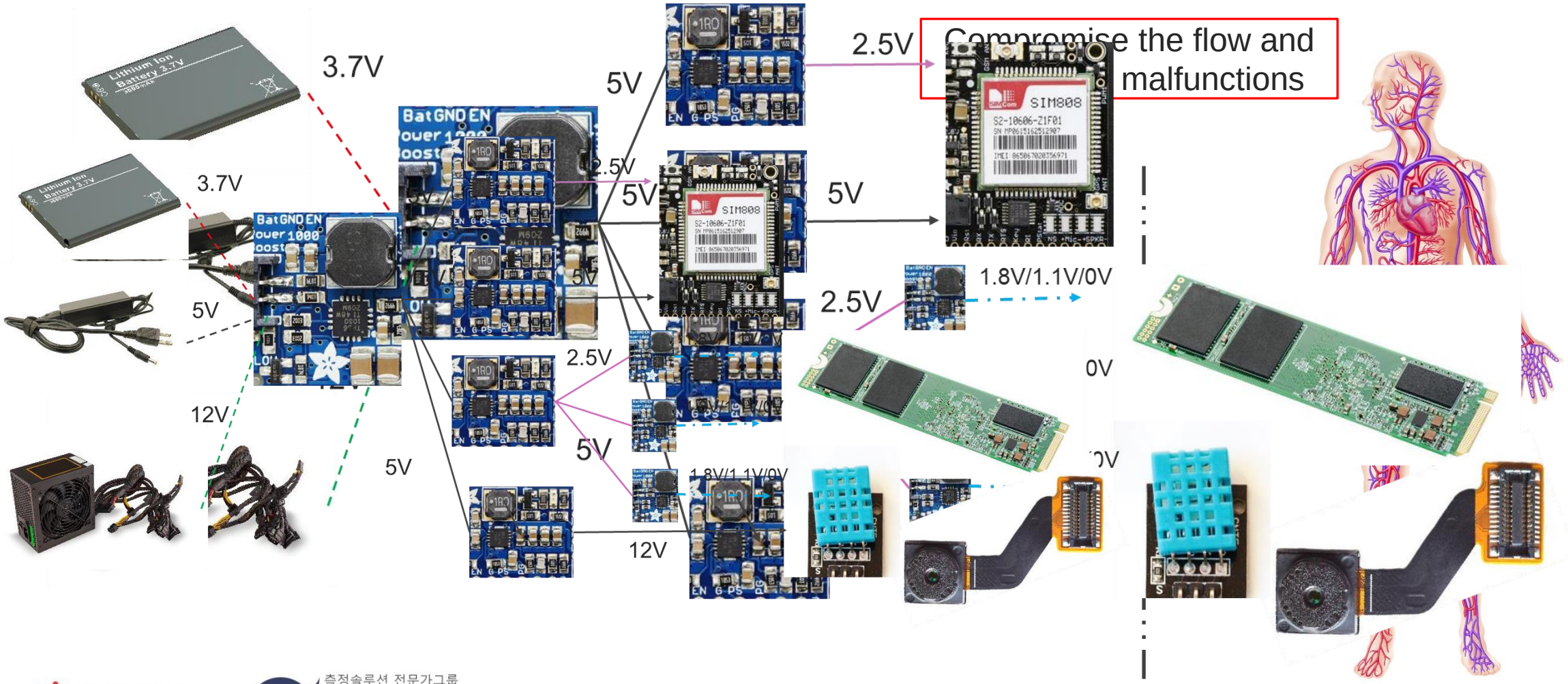
Power Integrity (PI)

Significance of dc power



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Power Integrity

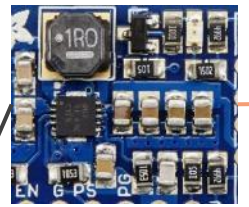
Job of PI engineer

3.7V

5V

12V

5V



2.5V

5V

5V

2.5V

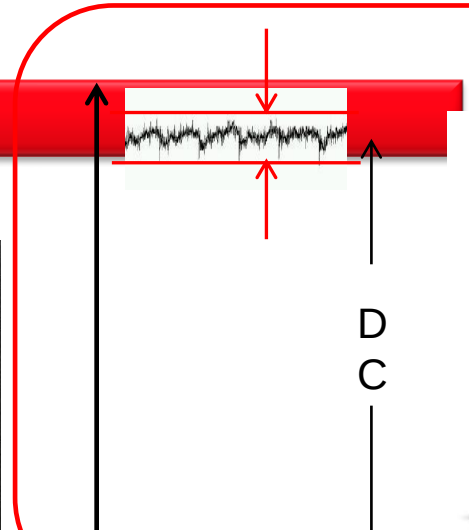
1.8V/1.1V/0V

1.8V/1.1V/0V

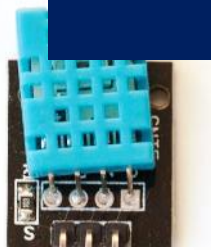
1.8V/1.1V/0V

5V

12V



전력 소비
전류 부하
에너지 효율성



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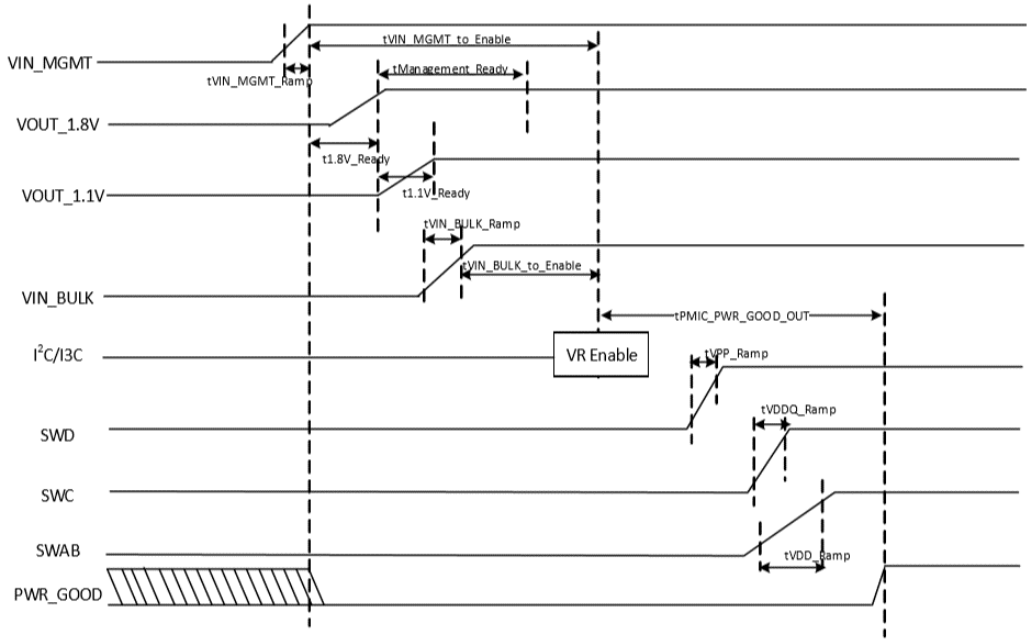
Power Integrity (PI)

파워시퀀스로 인한 설계복잡도 증가

Power Sequence Specification



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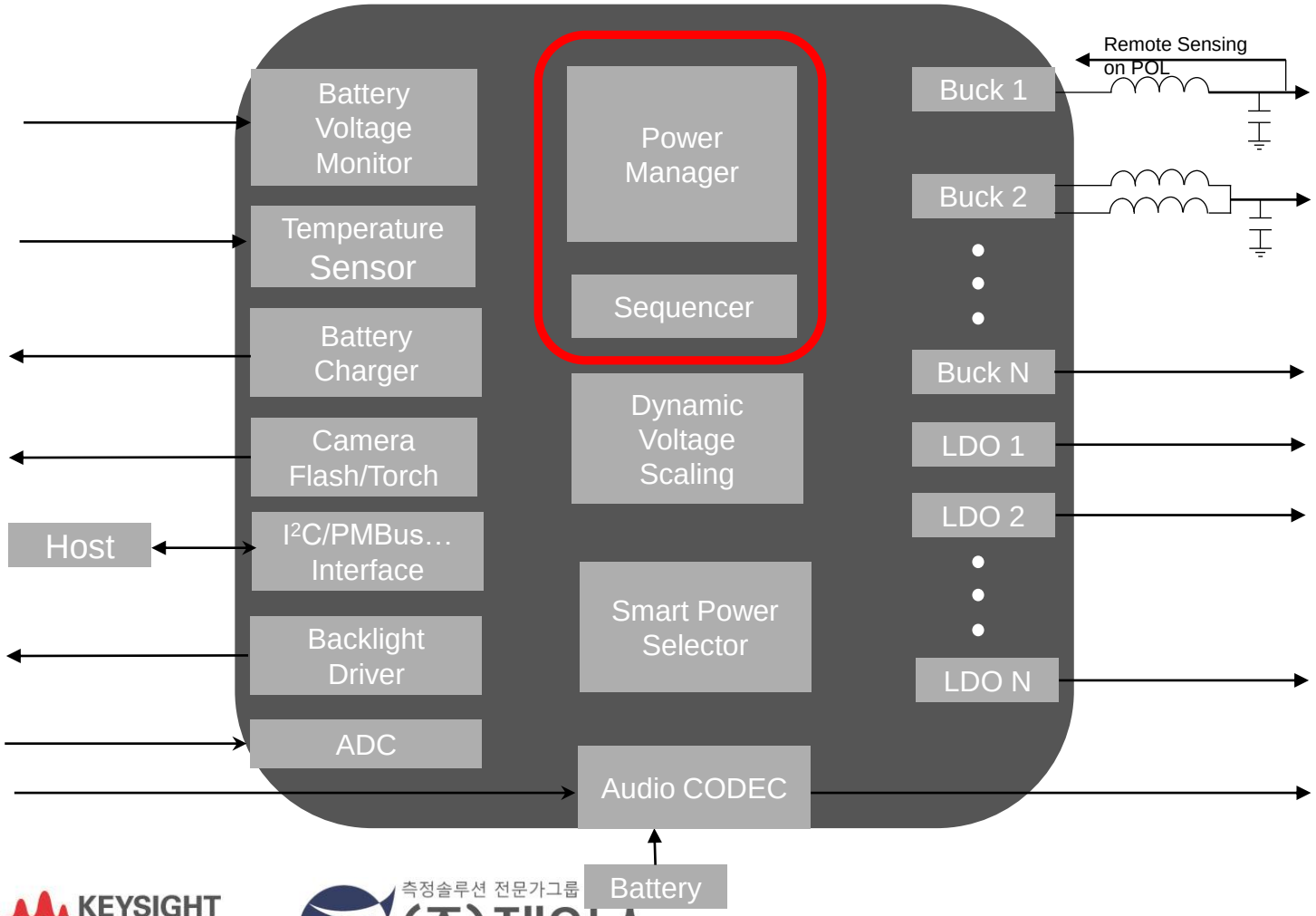
Power Integrity (PI)

Power Management IC (PMIC)



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Power Integrity

Pmic is the traffic officer

3.7V

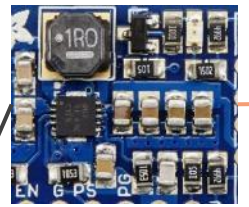
5V

12V

5V

5V

5V



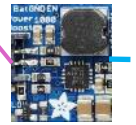
2.5V

5V

2.5V

1.8V/1.1V/0V

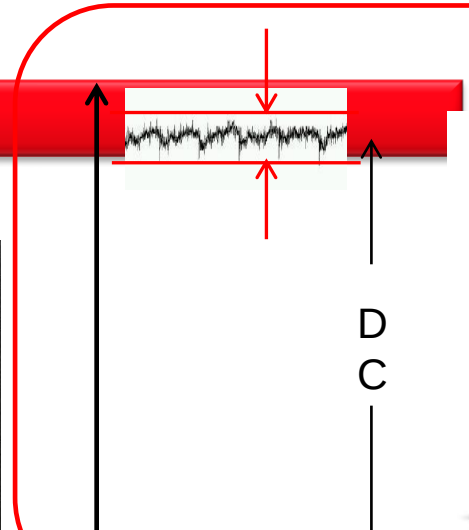
1.8V/1.1V/0V

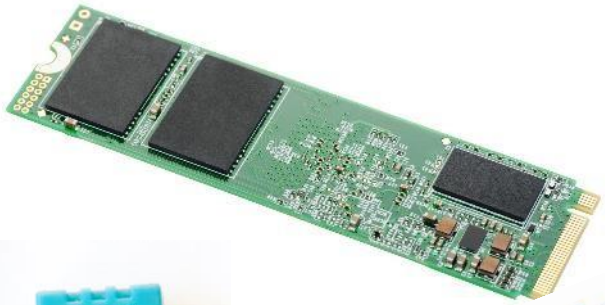


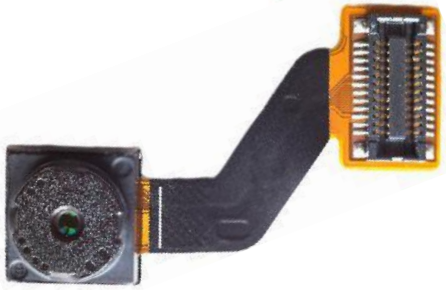
1.8V/1.1V/0V

12V

PMIC







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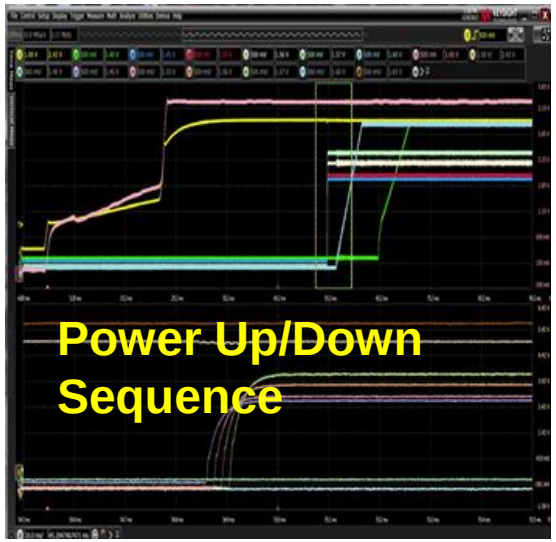
Power Integrity (PI)

Typical test flow

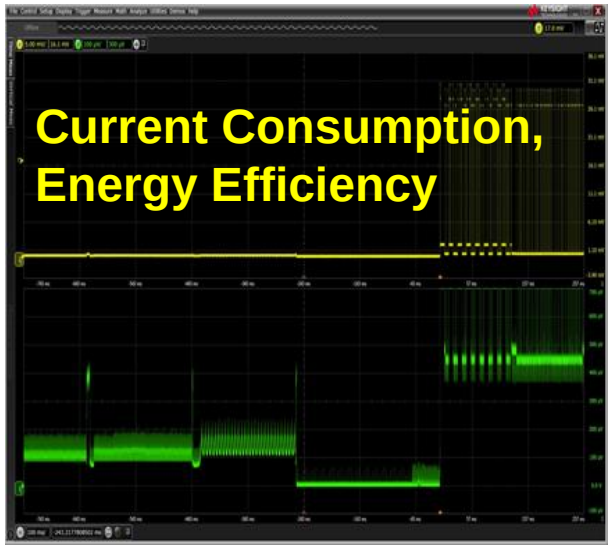
1

2



3

4



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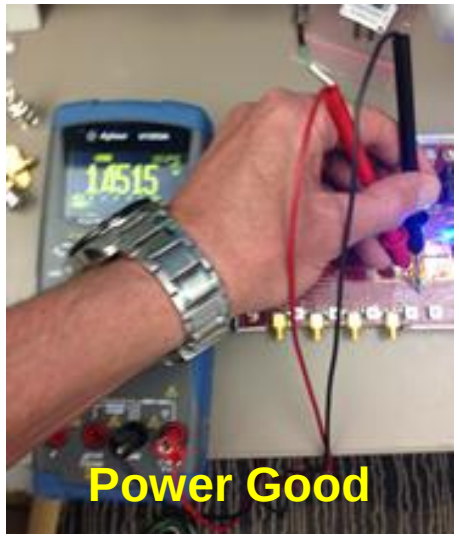
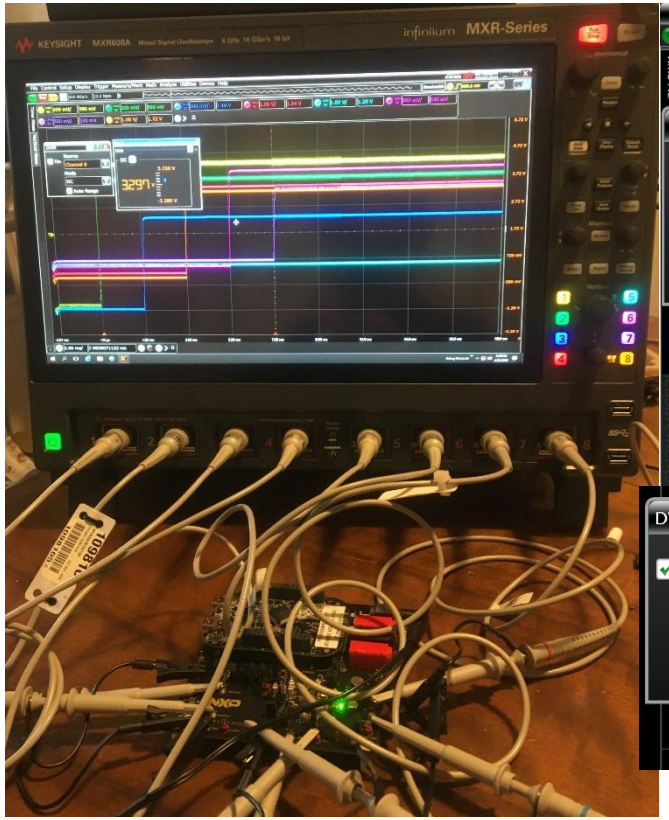
Power Integrity

Power-good using EXR dvm

1





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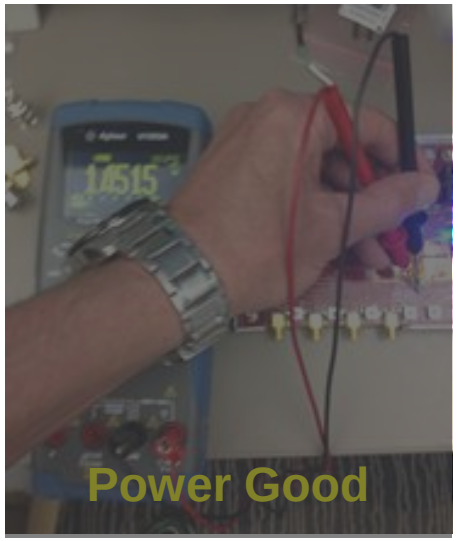
Power Integrity (PI)

Typical test flow

1



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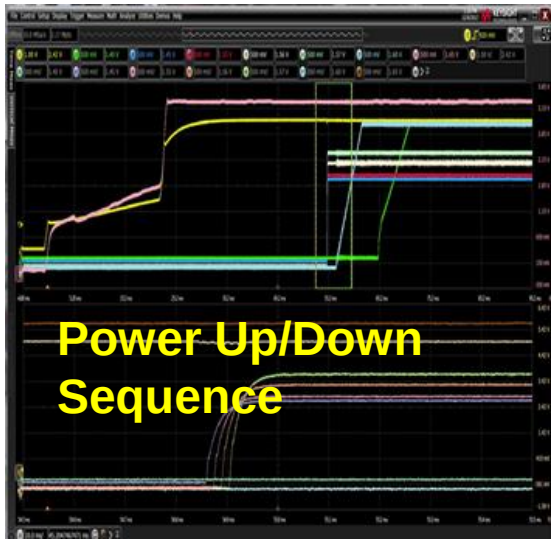

3

4

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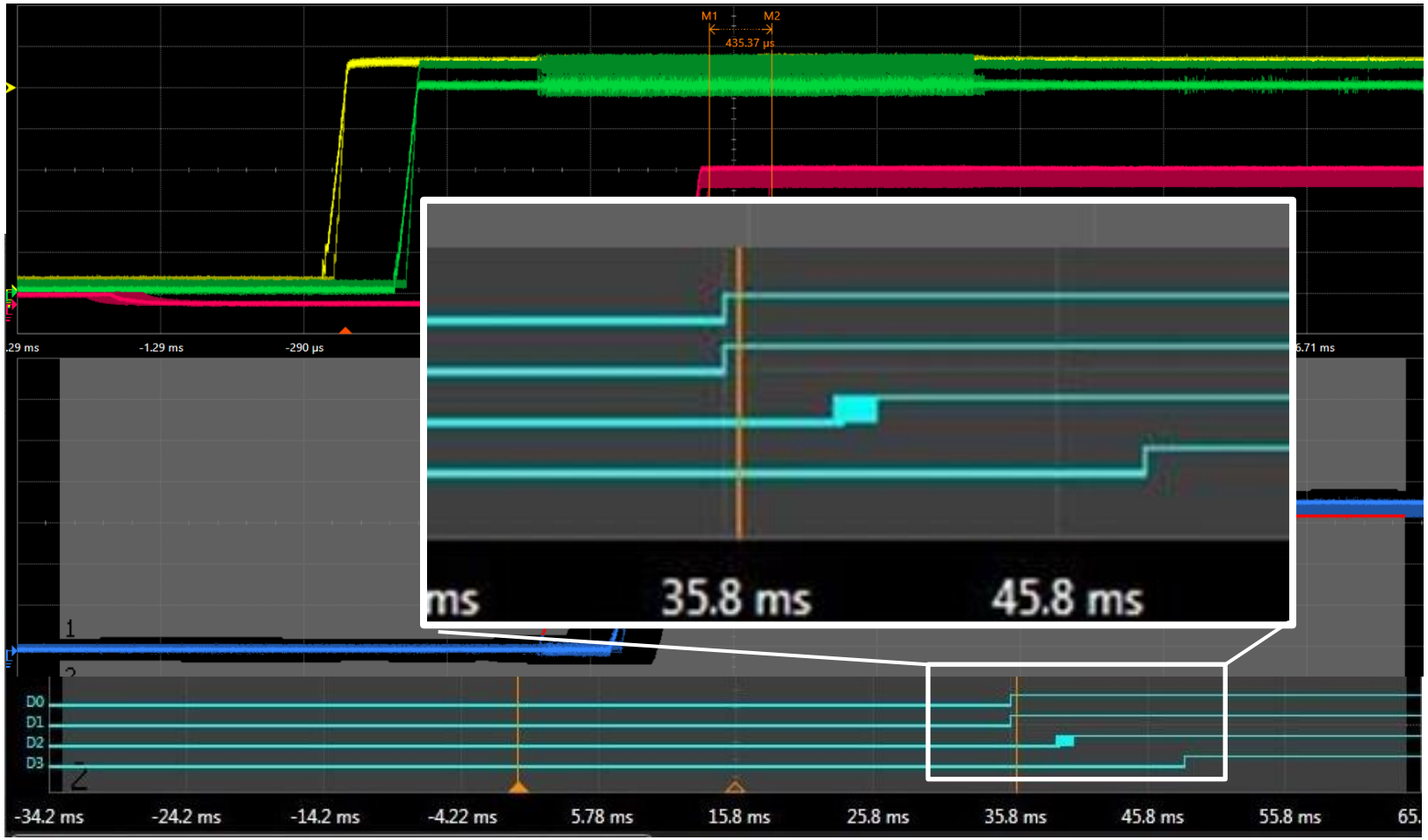
PMIC Testing

Power Seq.—ex. 8 rails, Persistence & Digital



Digital Channels

- No analog information
- No statistics (run/run variations)

Issues

- Uncertainty
- Time consuming

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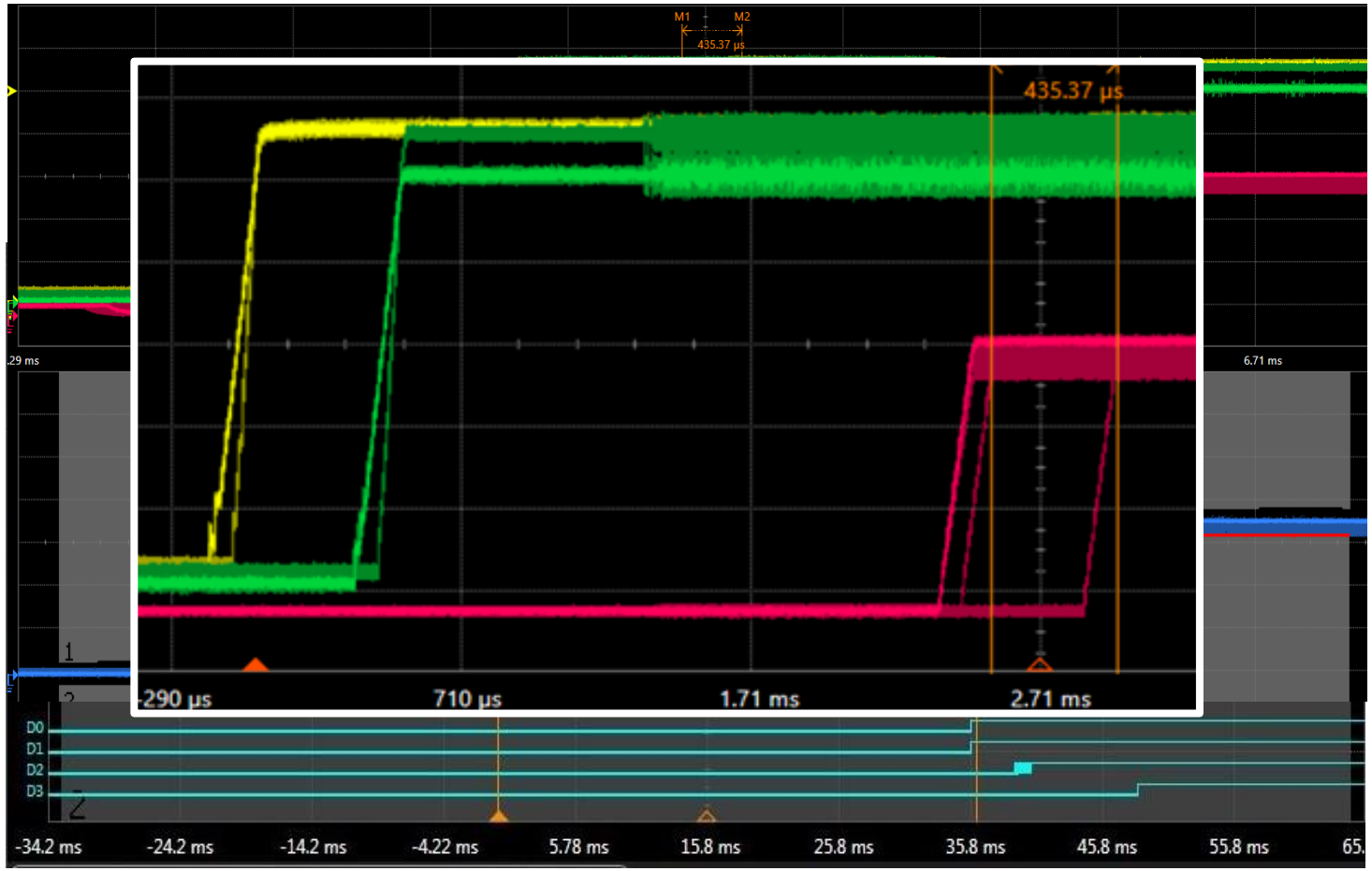
측정솔루션 전문가그룹
(주)제이스

PMIC Testing

Power Seq.—ex. 8 rails, Persistence & Digital



Infinite Persistence

- No ‘count’ of occurrences
- Manually place makers to determine pass/fail

Issues

- Uncertainty
- Time consuming
- Not repeatable/human error

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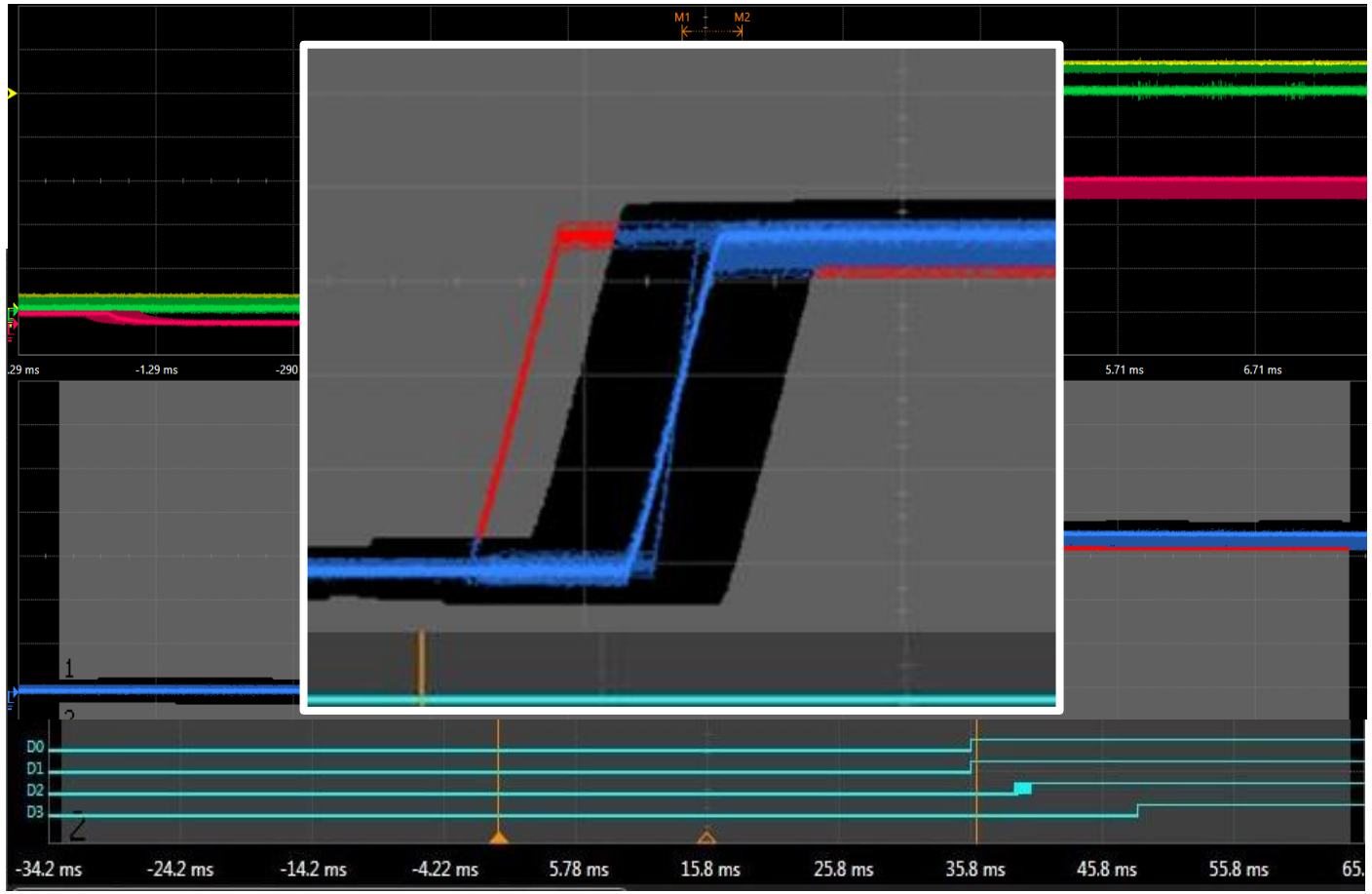
(주)제이스

PMIC Testing

Power Seq.—ex. 8 rails, Persistence & Digital



Mask Test

- Failures clearly identified
- Number of pass/fail measured
- Mask represents specification tolerances

Issues

- Only one mask available

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측정솔루션 전문가그룹
(주)제이스

PMIC Testing

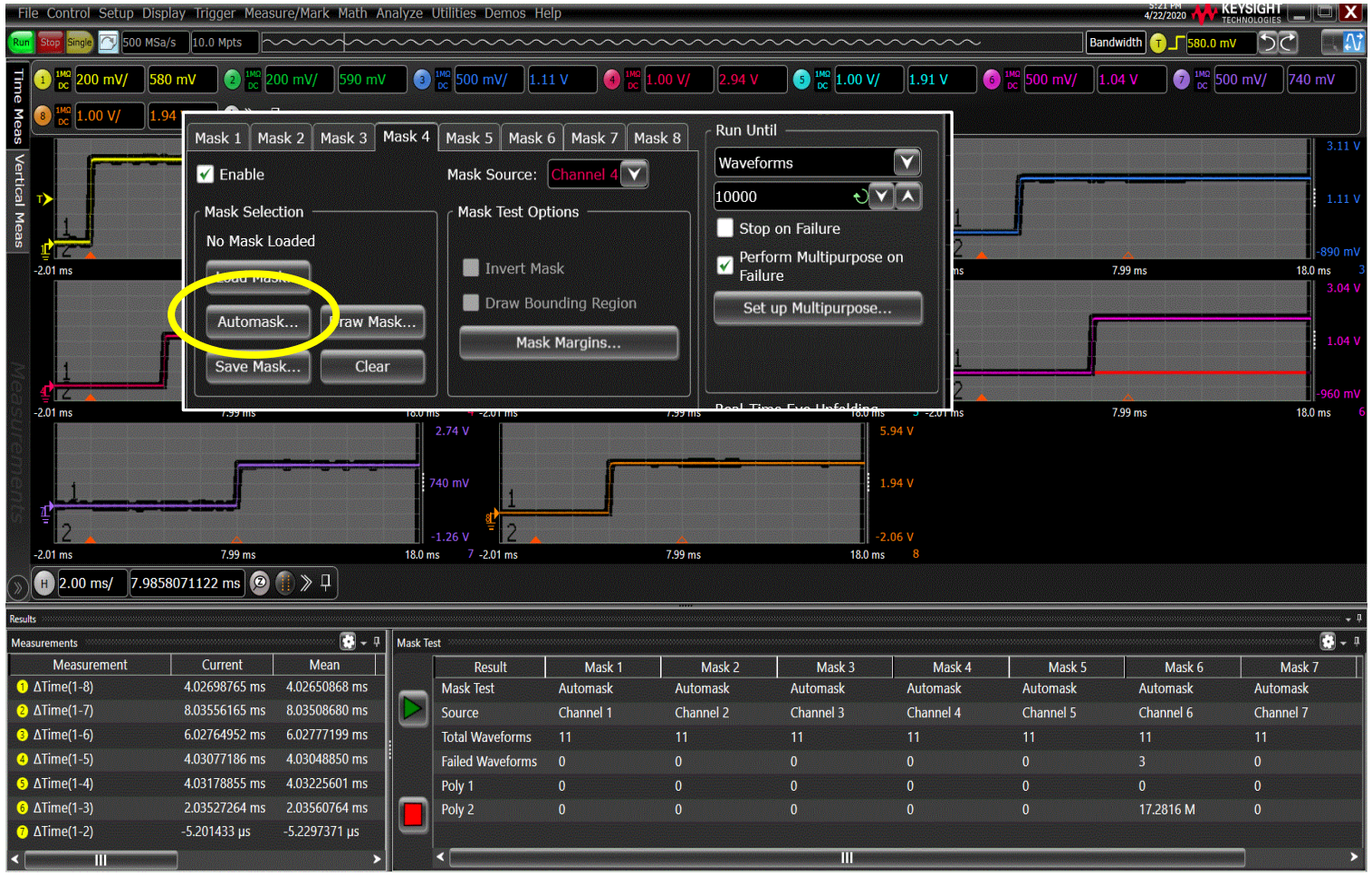
Power Sequence testing—mask on every ch.

Mask for every channel

- Saves time
- Eliminates uncertainty
- Complete test report in one screen shot

Automask

- Saves time
- Simple and easy mask setup



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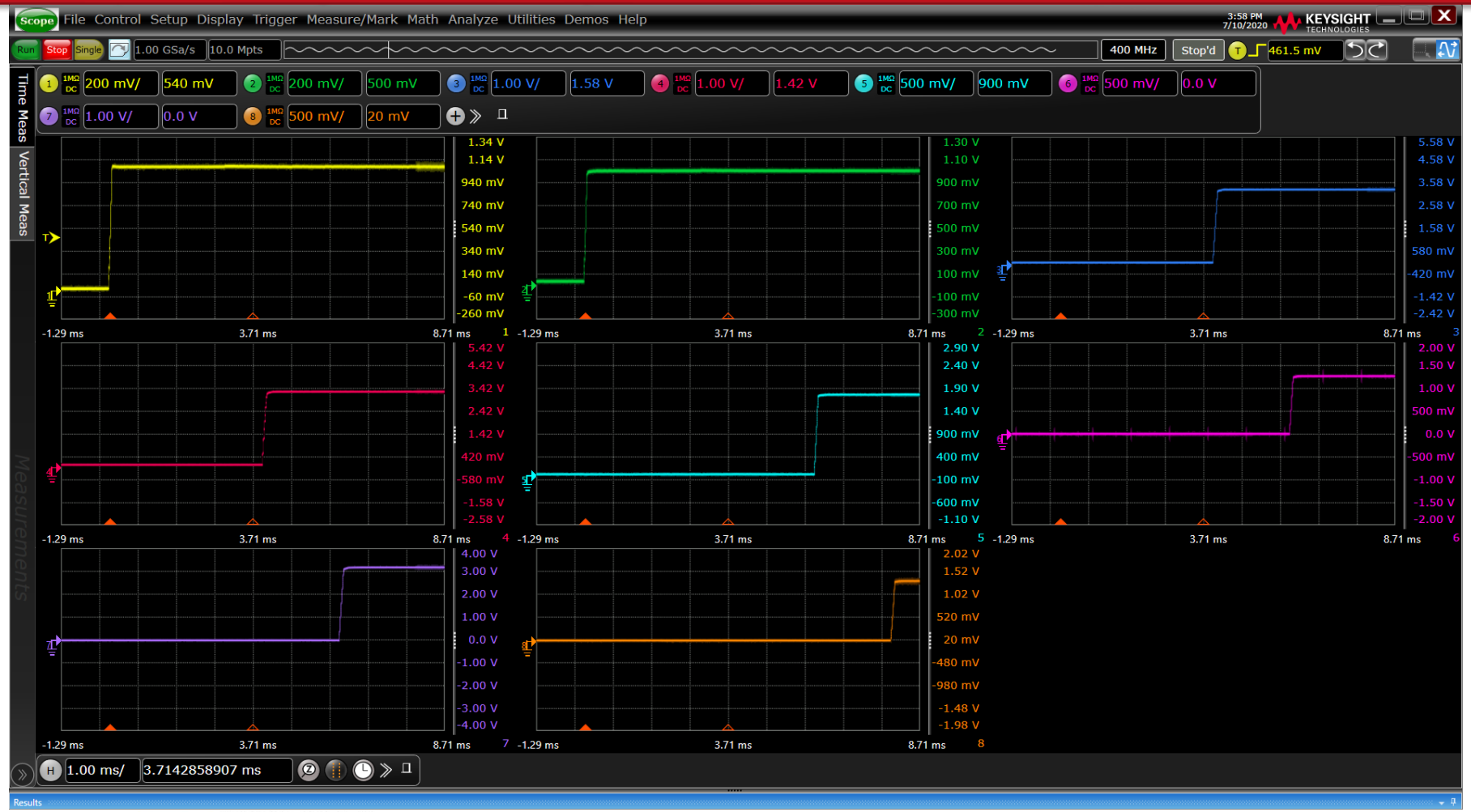
측정솔루션 전문가그룹 (주)제이스

PMIC Testing

Power sequence testing—mask on every ch.



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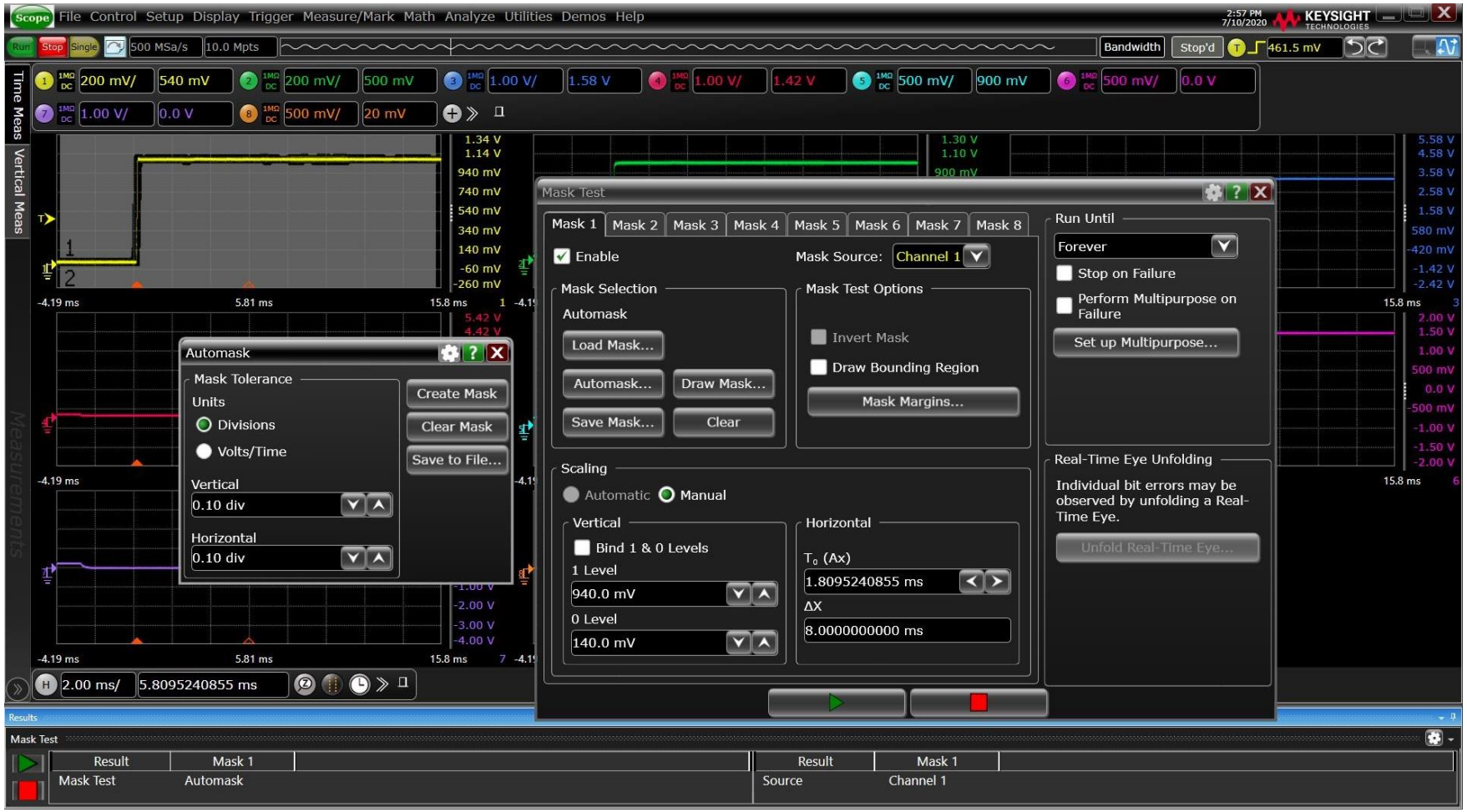
측정솔루션 전문가그룹
(주)제이스

PMIC Testing

Power sequence testing—mask on every ch.



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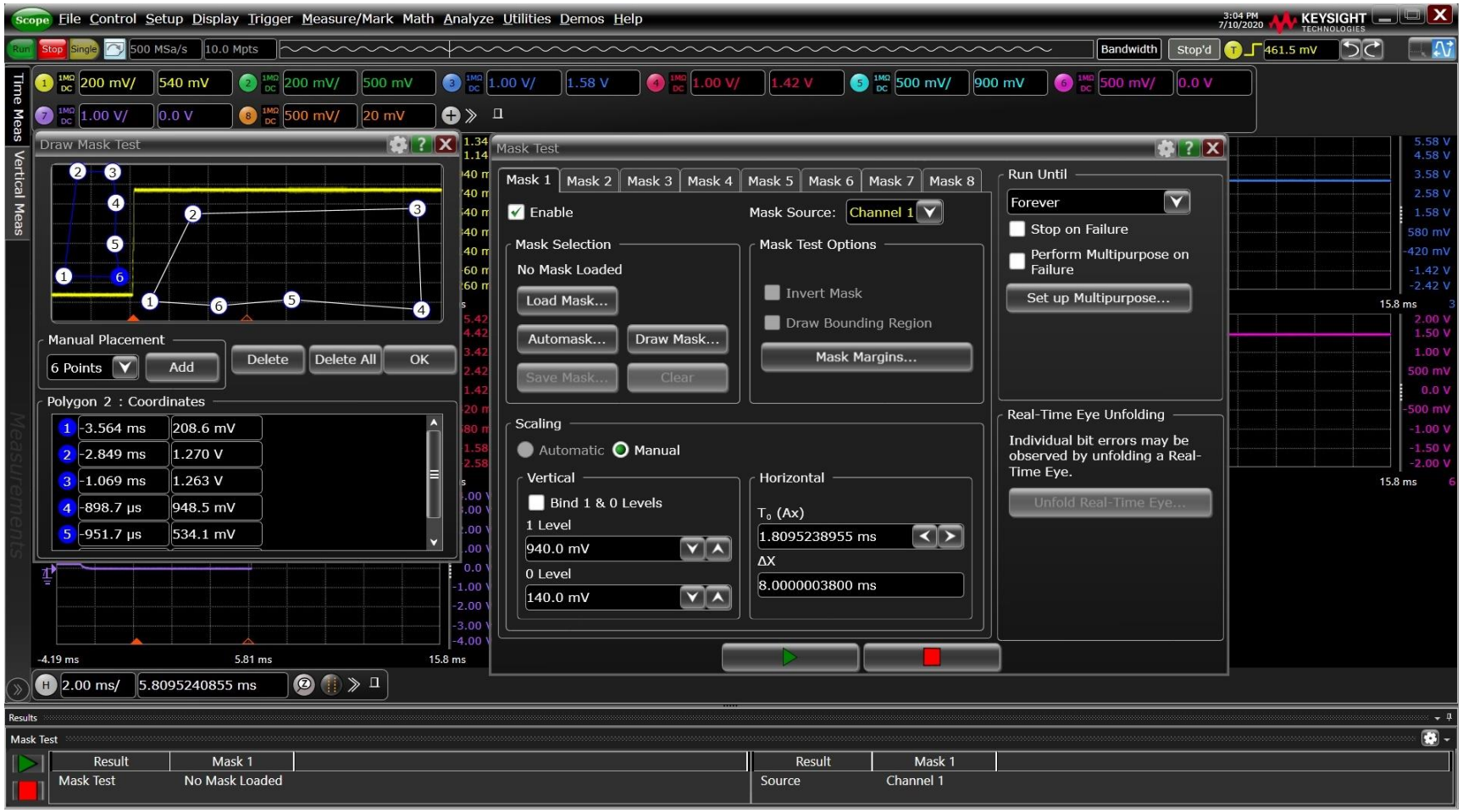
측정솔루션 전문가그룹
(주)제이스

PMIC Testing

Power sequence testing—mask on every ch.



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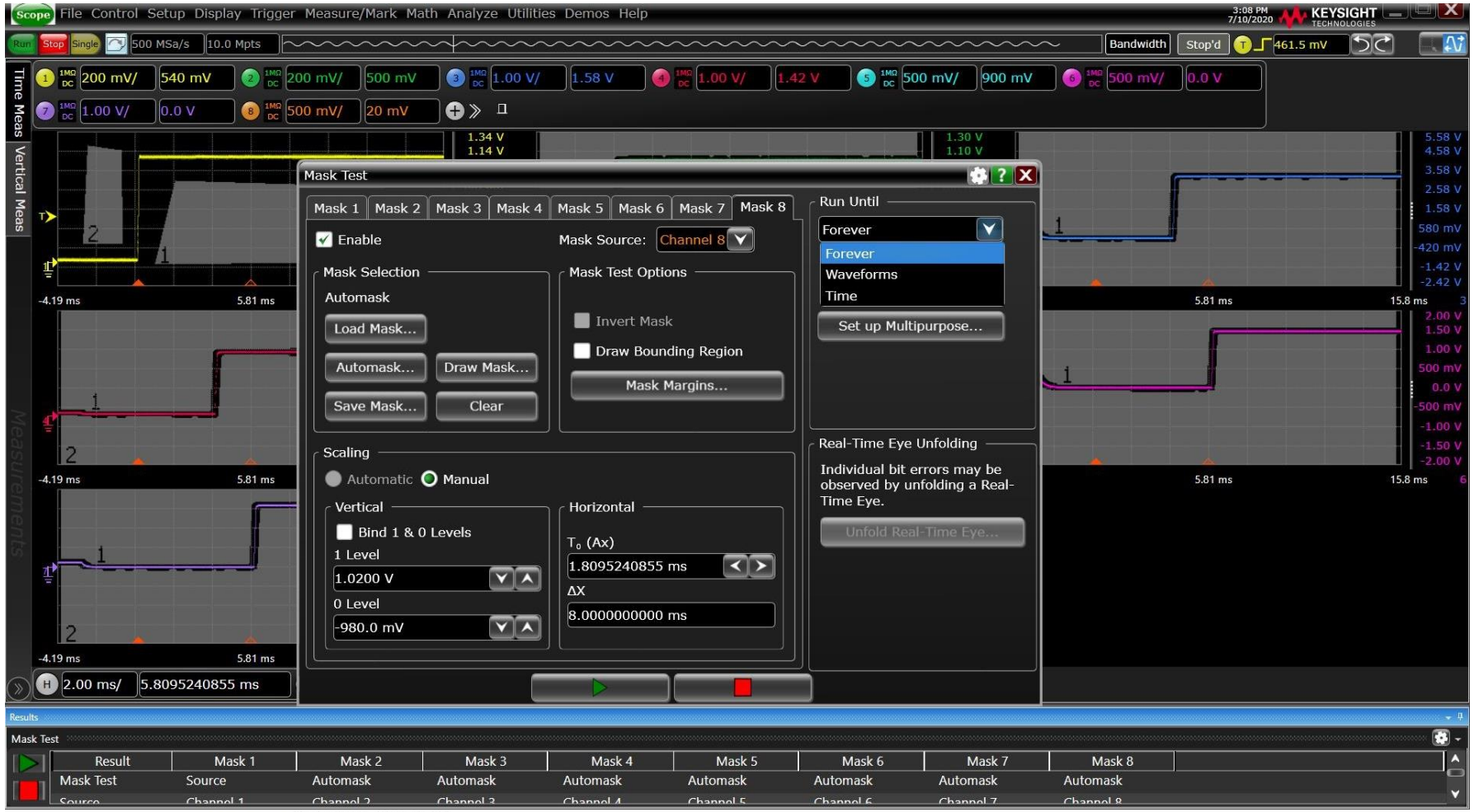
측정솔루션 전문가그룹
(주)제이스

PMIC Testing

Power sequence testing—mask on every ch.



KEYSIGHT TECHNOLOGIES
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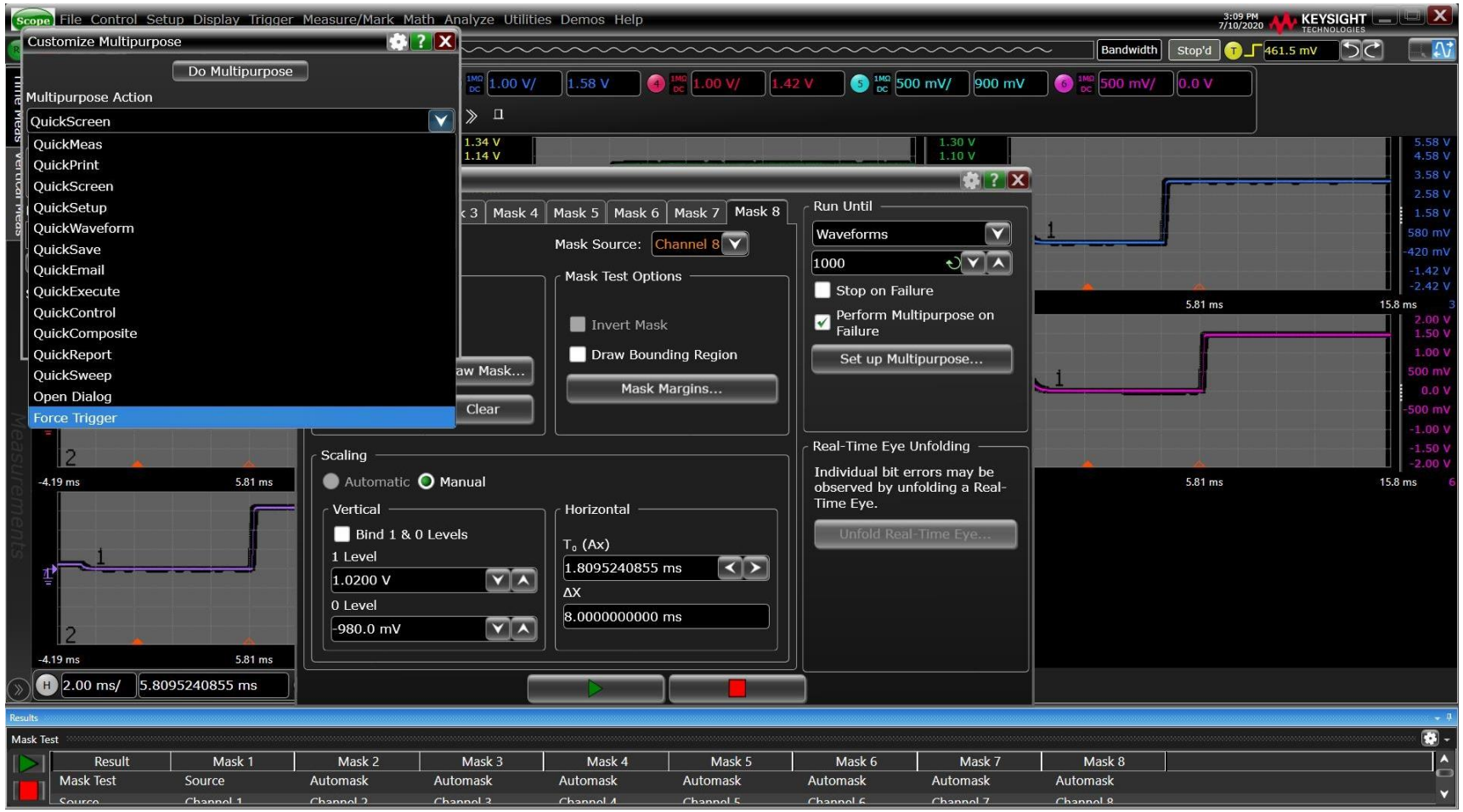
측정솔루션 전문가그룹
(주)제이스

PMIC Testing

Power sequence testing—mask on every ch.



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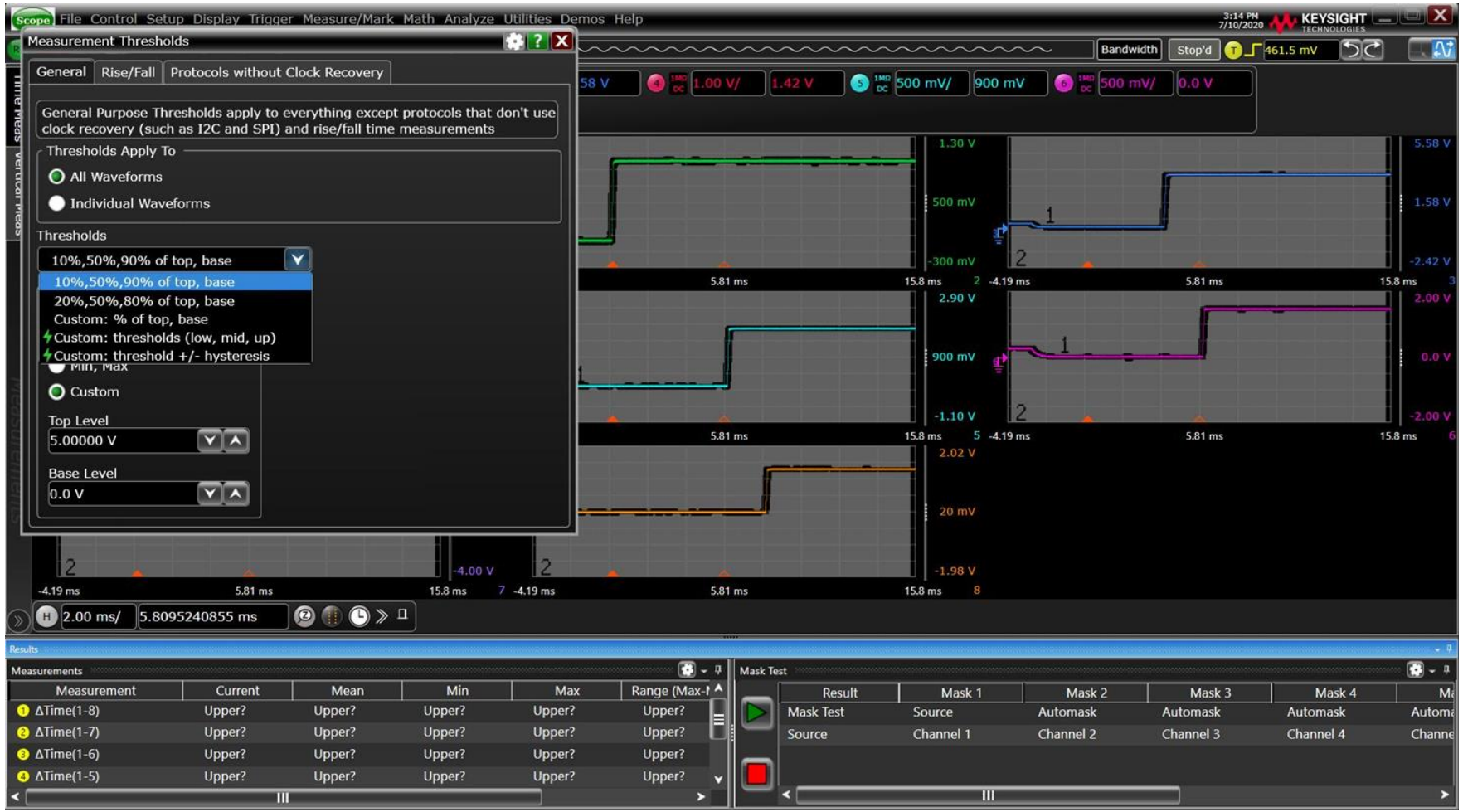
측정솔루션 전문가그룹
(주)제이스

PMIC Testing

Power sequence testing—Δtime measurements



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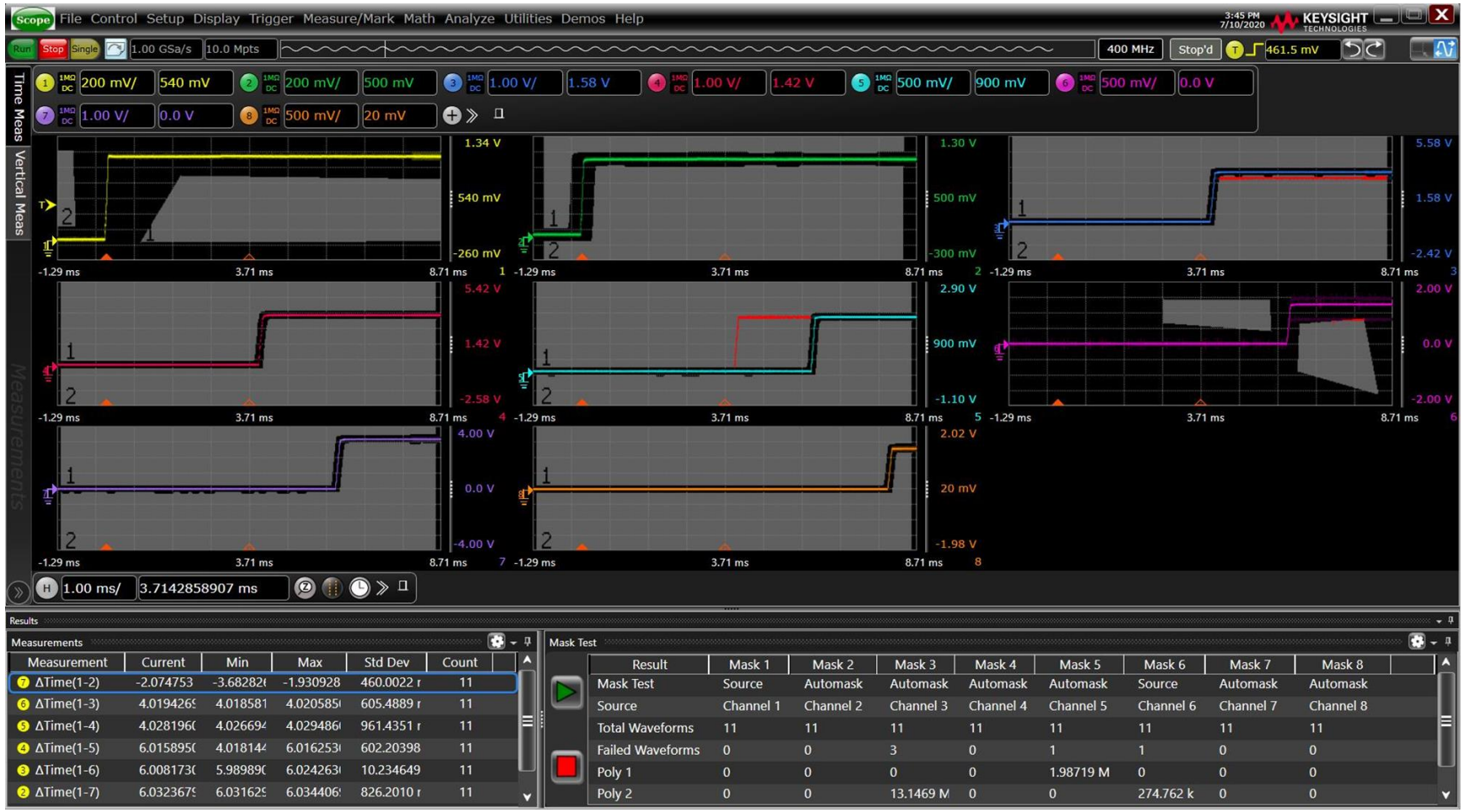
(주)제이스

PMIC Testing

Power sequence testing—one page report.



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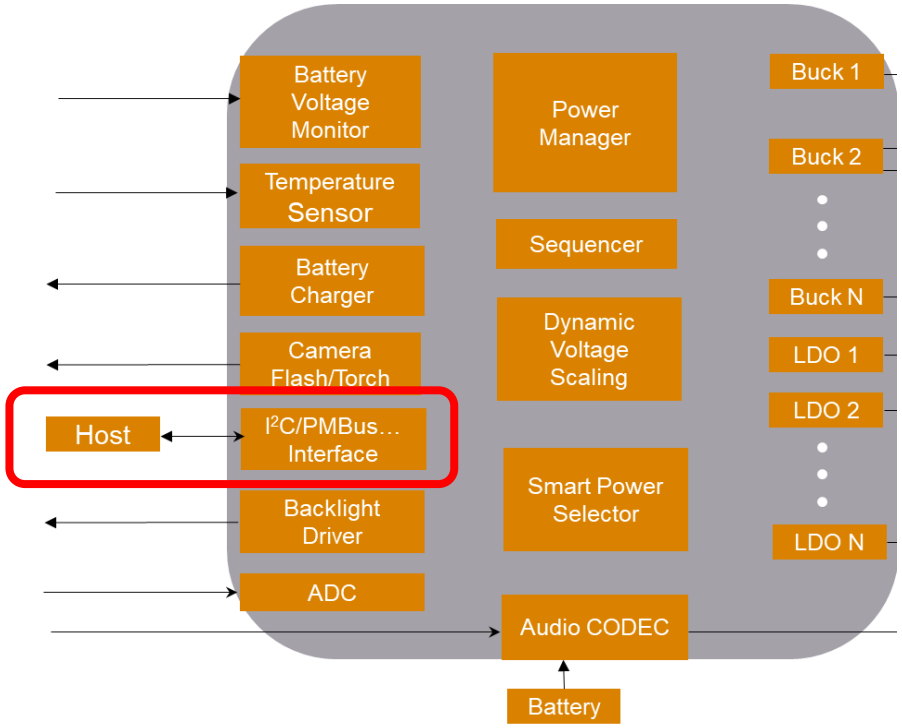
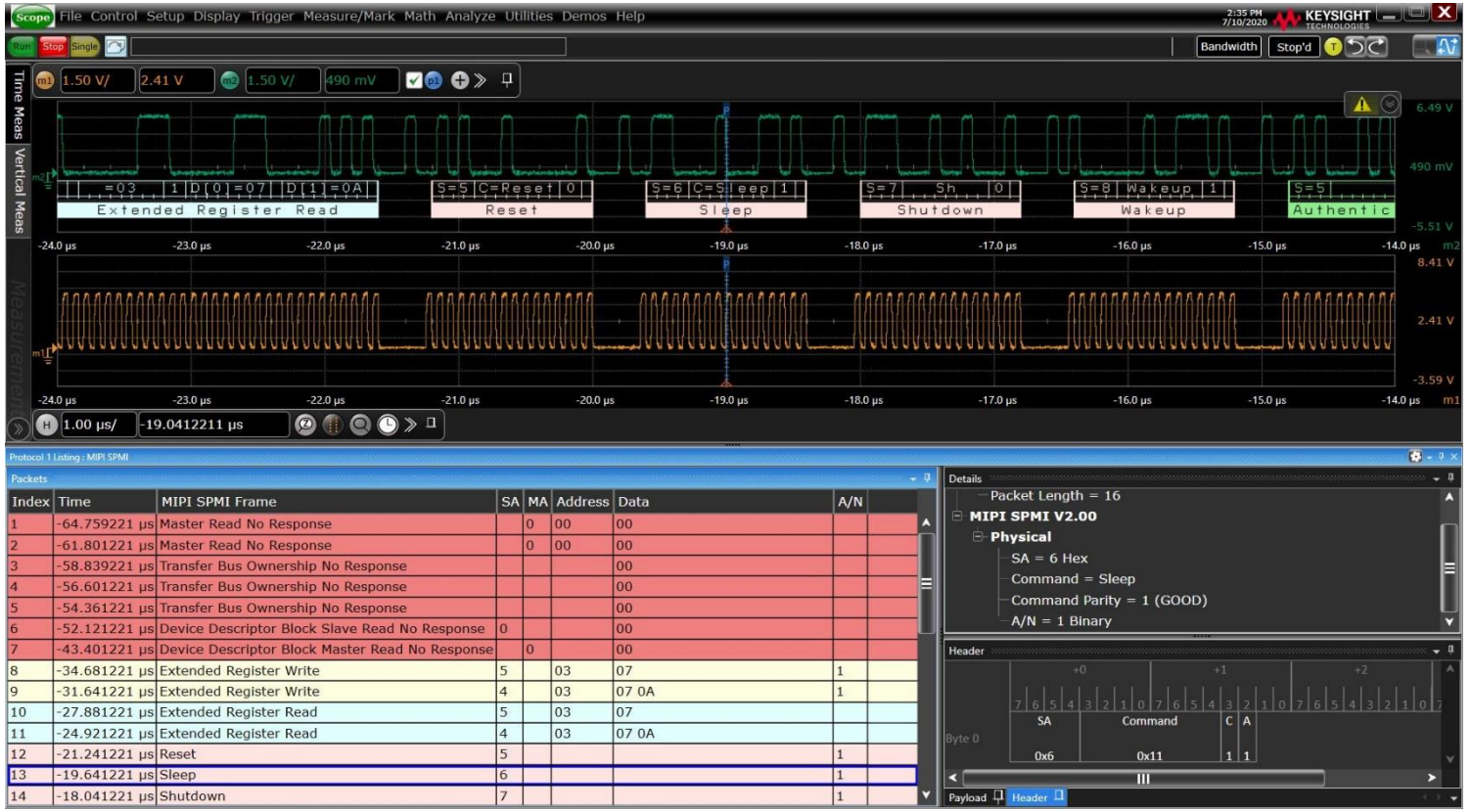
(주)제이스

PMIC Testing

Protocol decode and analysis—spmi example





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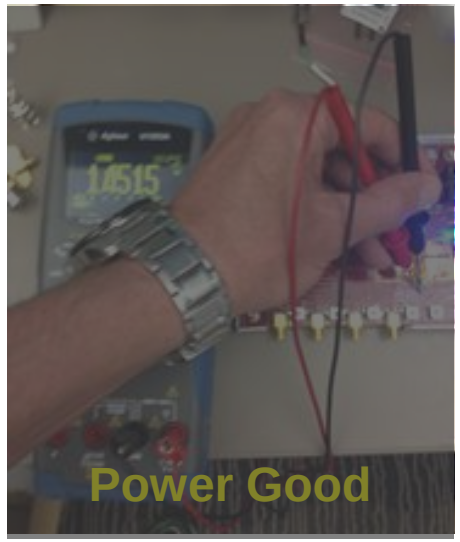
(주)제이스

Power Integrity (PI)

Typical test flow

1



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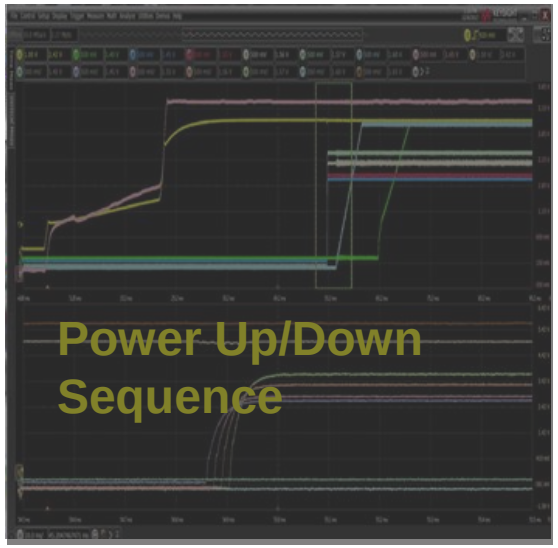

3

4

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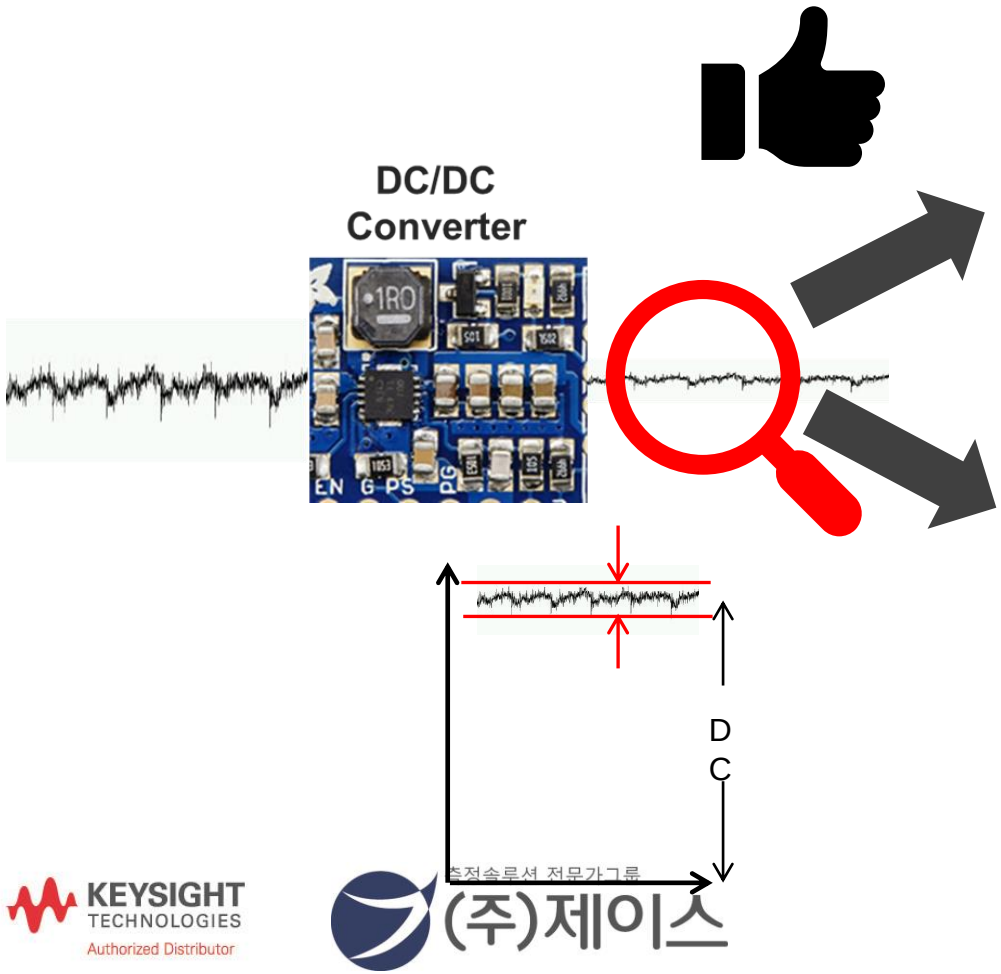
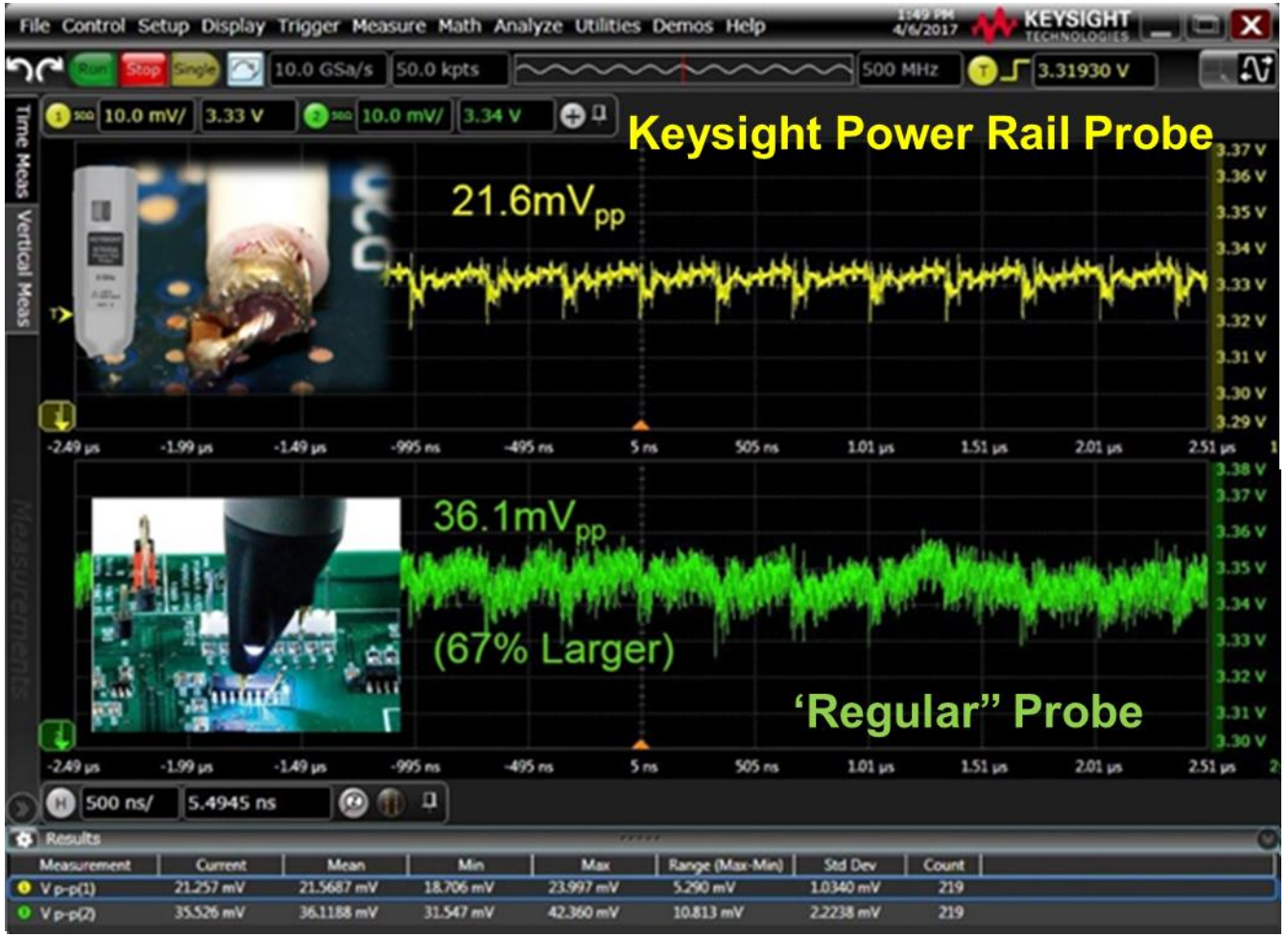
Power Integrity

Power rail quality





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(주)제이스

Power Integrity

Keysight Power Rail Probes for EXR-Series

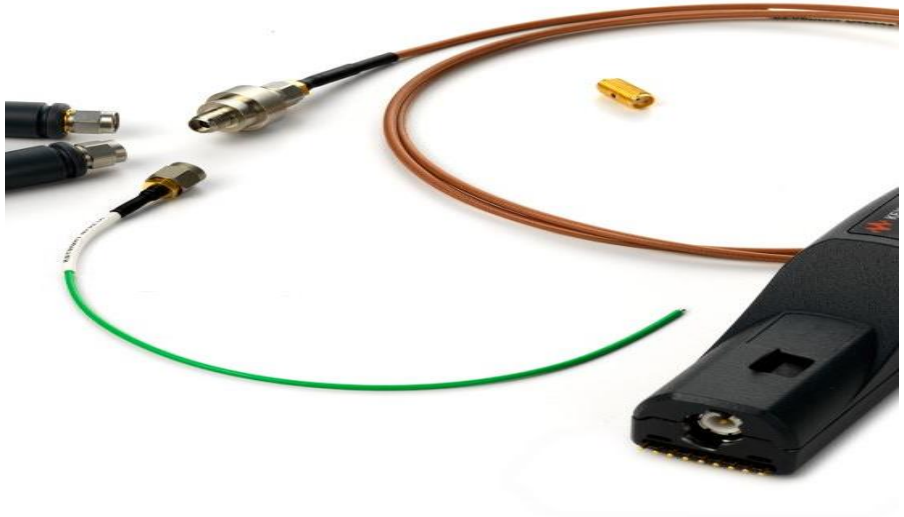
- Keysight invented the Power Rail probe and their use with oscilloscopes
- Optimized for measuring the quality of power rails

N7020A

2GHz

N7024A

6GHz



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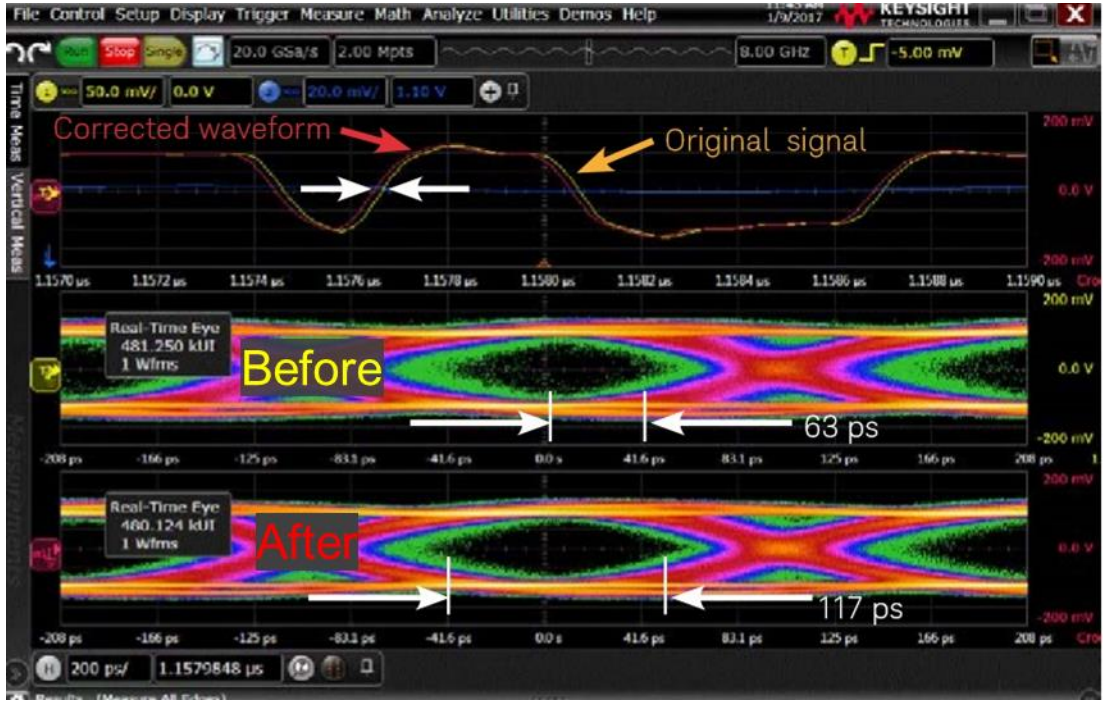
Power Integrity

D9010POWA power integrity analysis app

- Helps you understand power rail noise sources and power rail noise effects

Power Rail, before (with switching loads) & after (effects of switching loads removed).

Data Line before (with the effects of power rail noise) & after (effects of power rail noise removed).



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Authorized Distributor
측정솔루션 전문기업
(주)제이스

Power Integrity

D9010POWA power integrity analysis app

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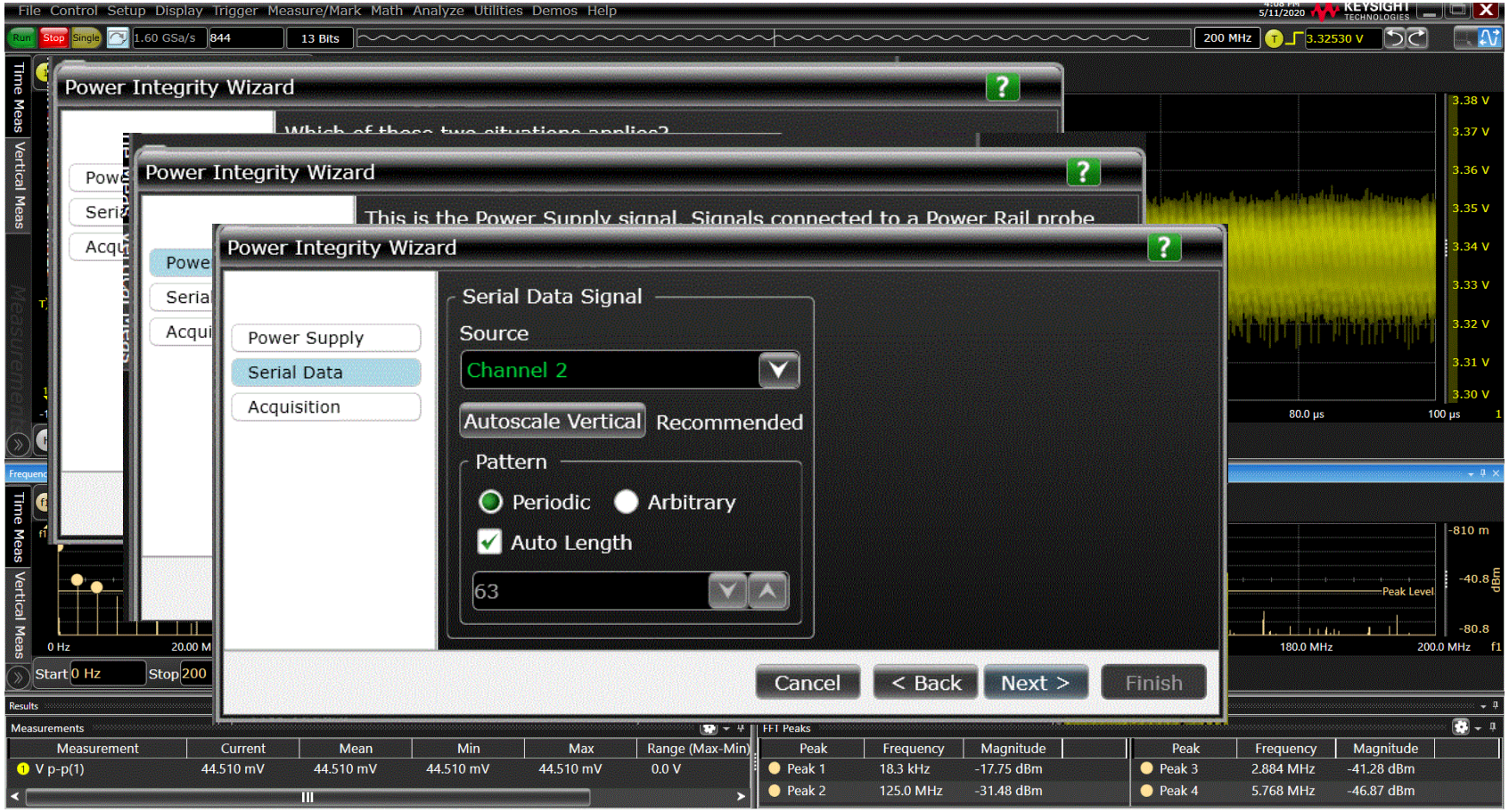
측정솔루션 전문가그룹
(주)제이스

Power Integrity

D9010POWA power integrity analysis app



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(주)제이스

Power Integrity

D9010POWA power integrity analysis app

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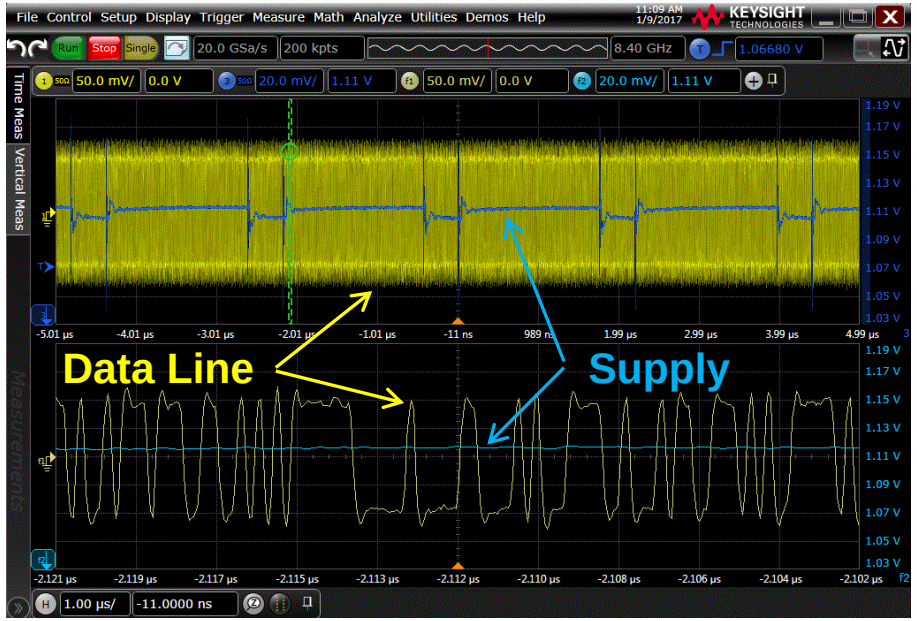
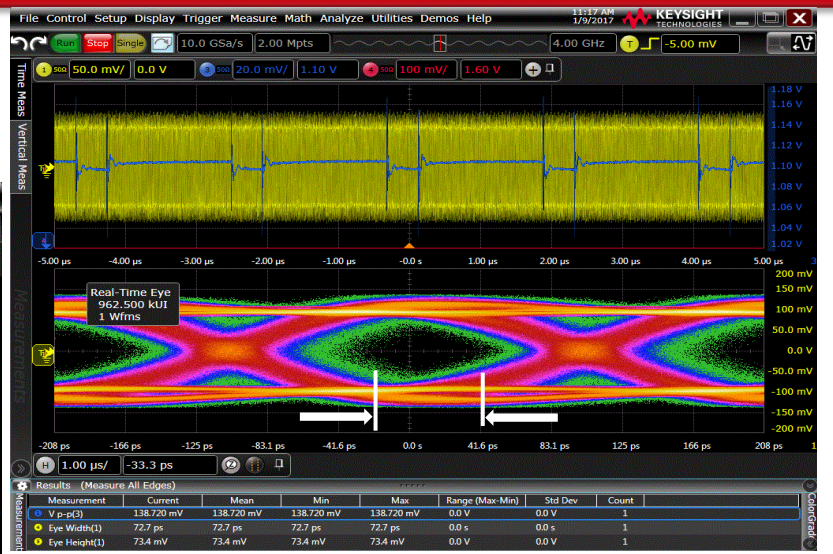
Power Integrity

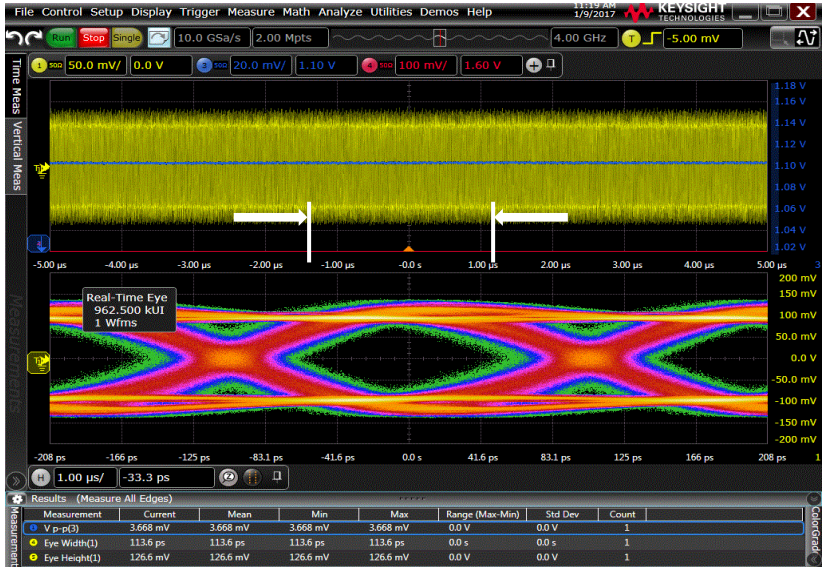
D9010POWA power integrity analysis app

1.10V Supply with 115mV$_{pp}$ Noise (±5%)





1.10V Supply with 3mV$_{pp}$ Noise



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(주)제이스

Power Integrity

D9010POWA power integrity analysis app

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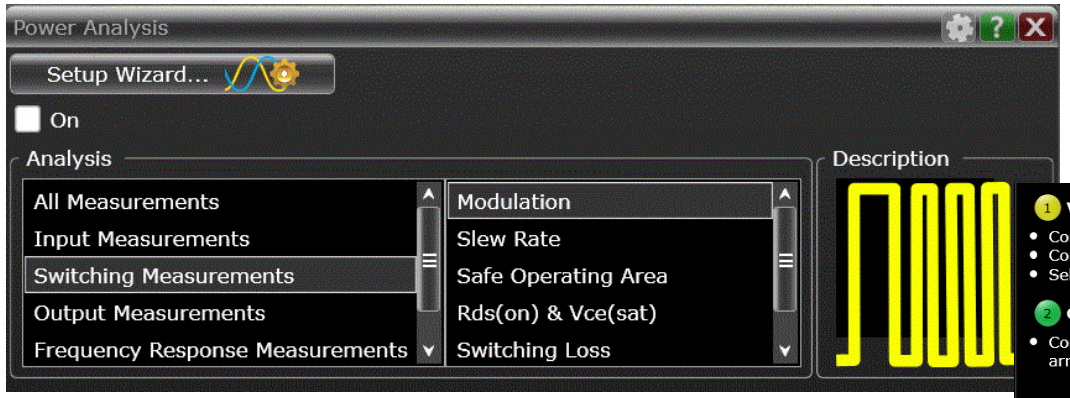
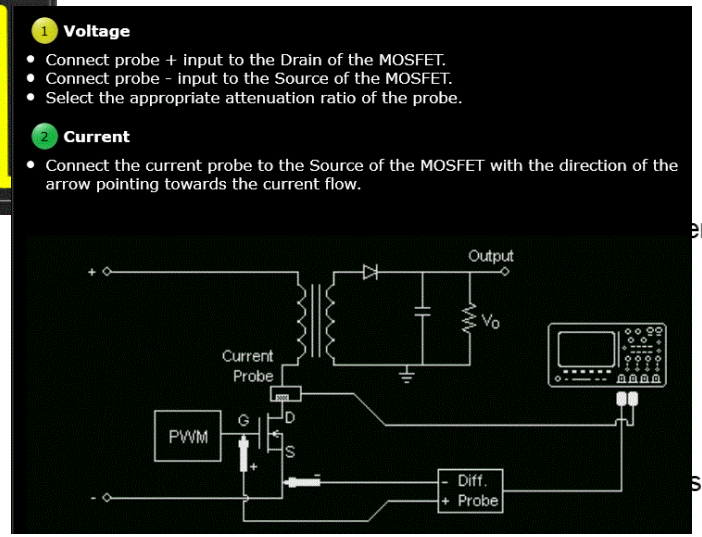
Power Integrity

D9010PWRA—Power analysis application

- Automated, time saving analysis of switch mode and linear power supplies
  - 20 measurements





- ‘Setup Wizard’ provides clear directions.

Type of analysis	Measurement
Input measurements	Power quality • Real power • Apparent power • Reactive power • Power factor • Crest factor • Phase angle
	Current harmonics
	Inrush current
Switching measurements	Switching loss
	Rds(on)
	Vce(sat)
	Slew rate
	Safe operating area
ents	Output ripple
	Turn-on time
	Turn-off time
	Efficiency
	Transient response settling time
se	Power supply rejection ratio (PSRR)
	Control loop response (gain and phase)

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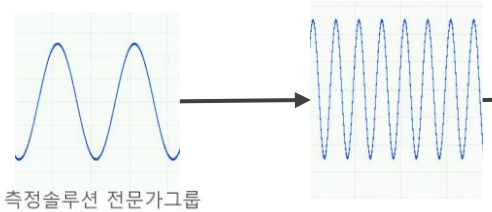
(주)제이스

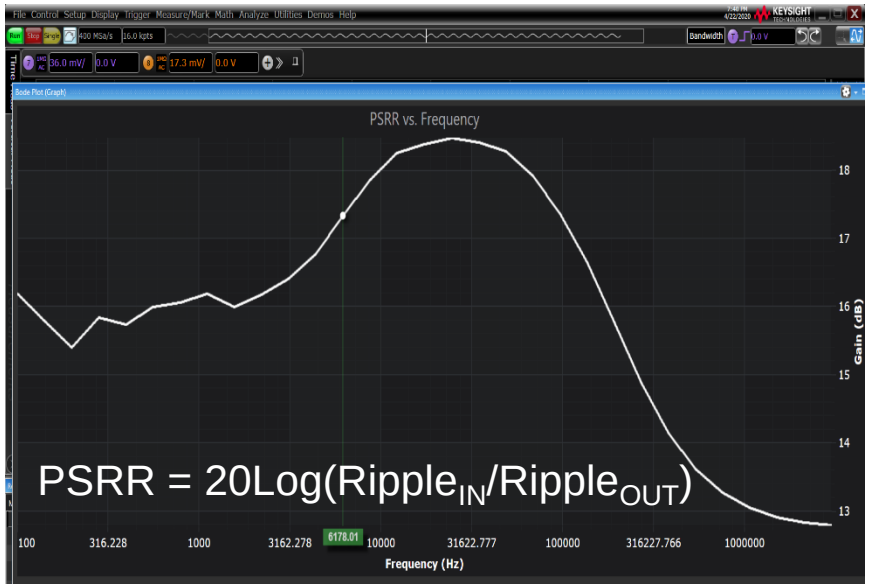
Power Integrity

Power supply rejection ratio--psrr

- PSRR is a measure of how well a DC-DC converter can reject noise on the input from getting to the output.

WaveGen





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Power Integrity

Power supply rejection ratio--psrr

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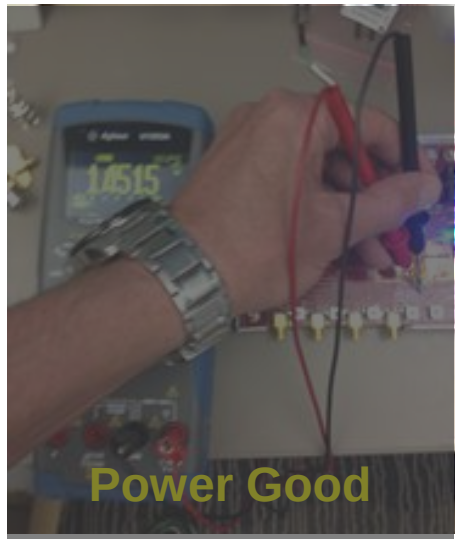
Power Integrity (PI)

Typical test flow

1



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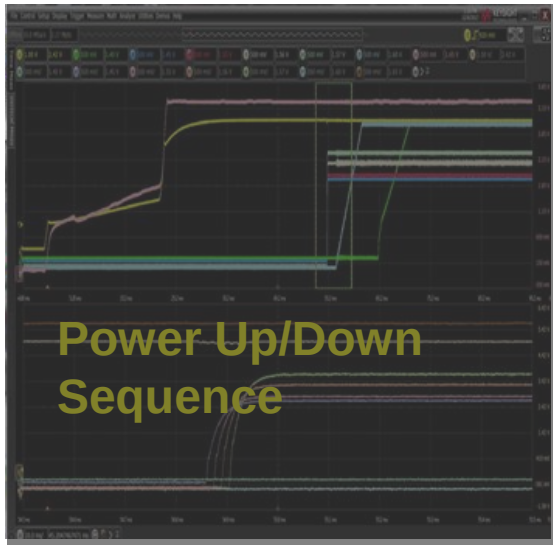

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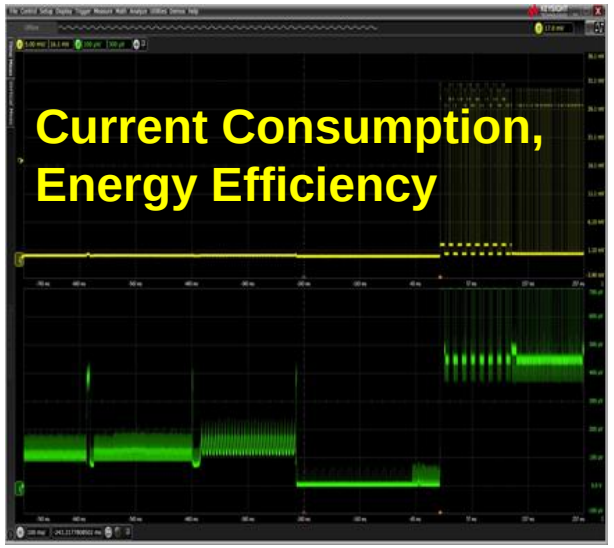

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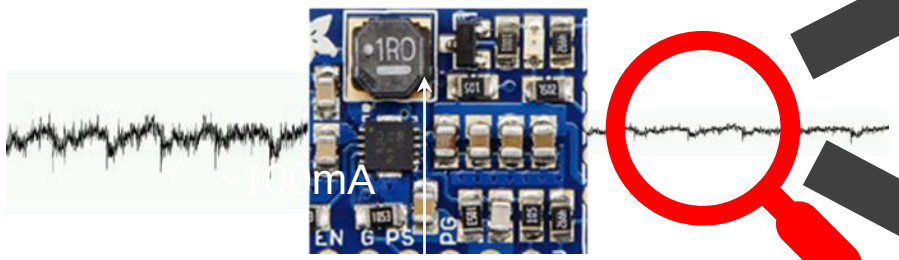
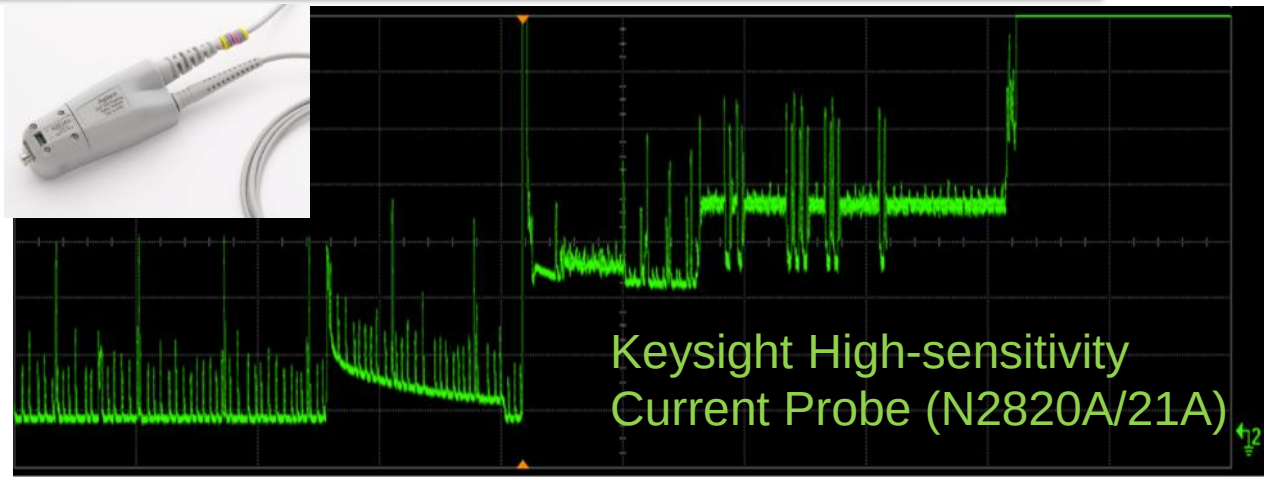
(주)제이스

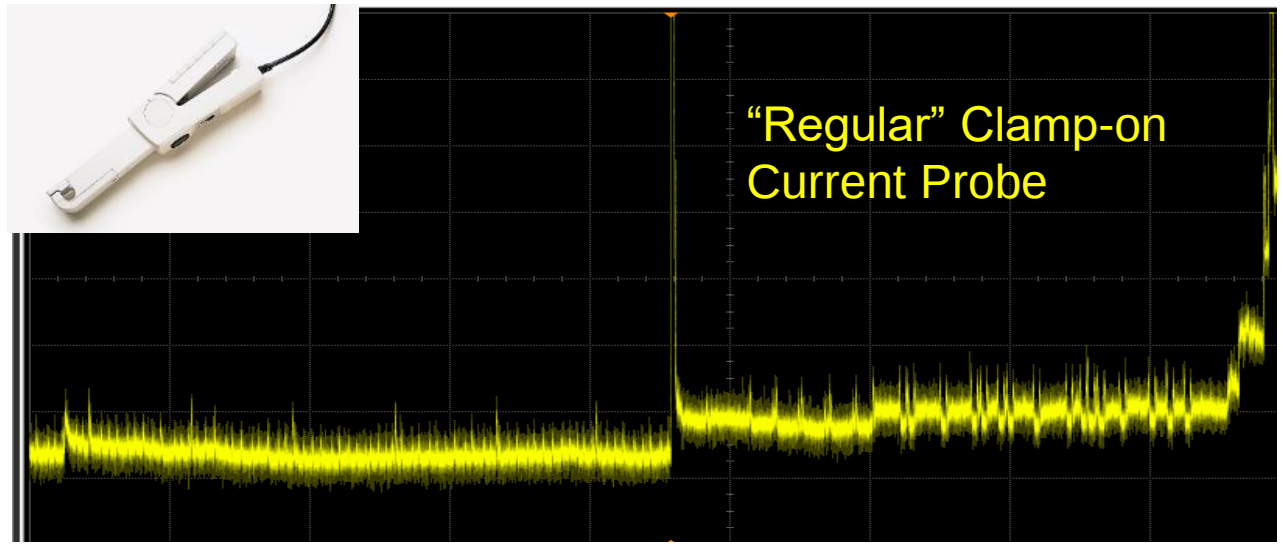
Power Integrity

Current consumption, energy efficiency

DC/DC
Converter







Transient Load response
In-rush current
Power
Efficiency
Etc.

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측정솔루션 전문가그
(주)제이스

Power Integrity

High-sensitivity current probes

– N2820A-Series Current Prob

- High Sensitivity
- High Dynamic Range
- R_{SENSE}: 1mΩ to 1MΩ

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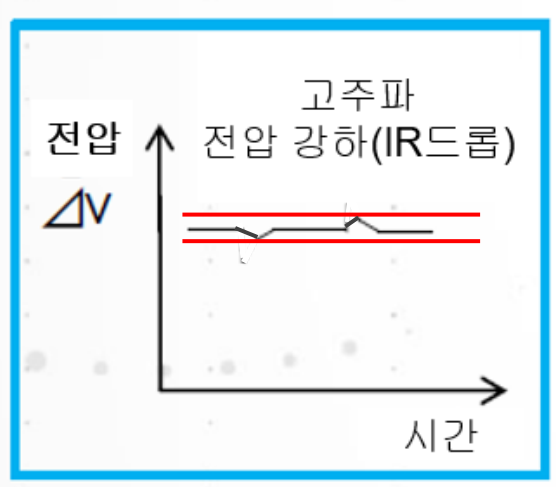
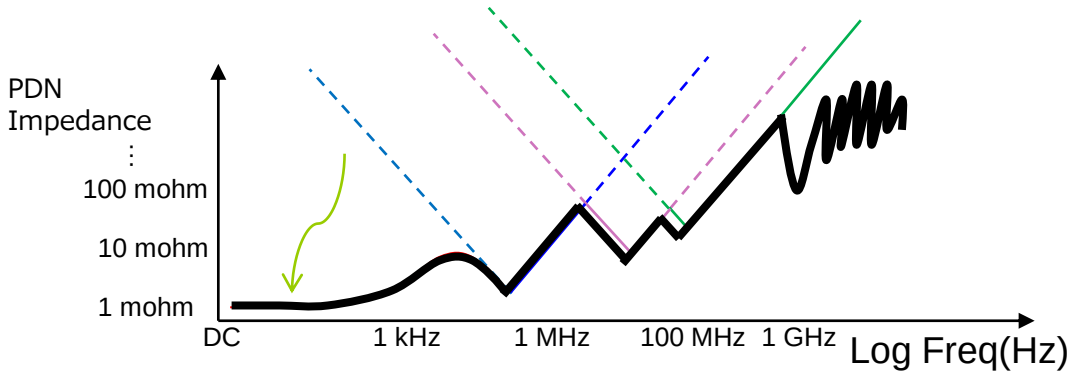
(주)제이스

Power Integrity (PI)

Summary





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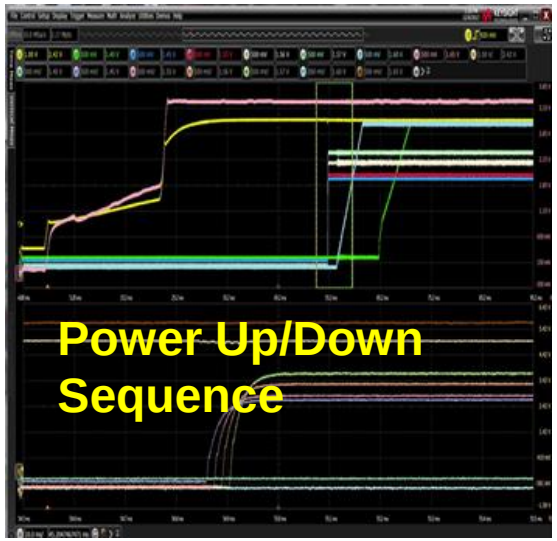
(주)제이스

Power Integrity (PI)

Summary

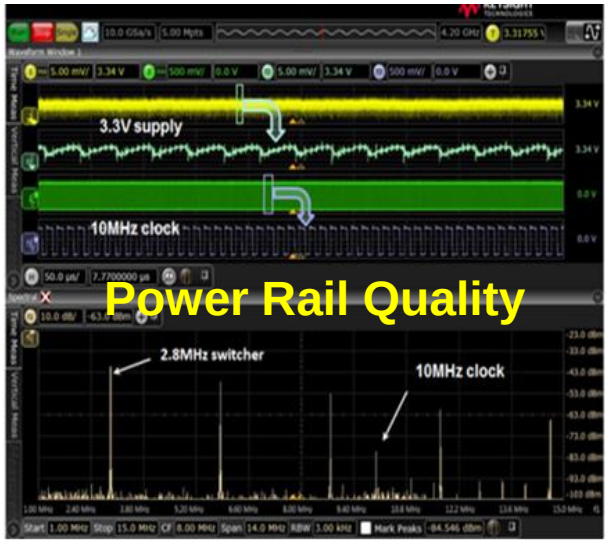
EXR With:

- Built-in Digital Volt Meter (standard feature).



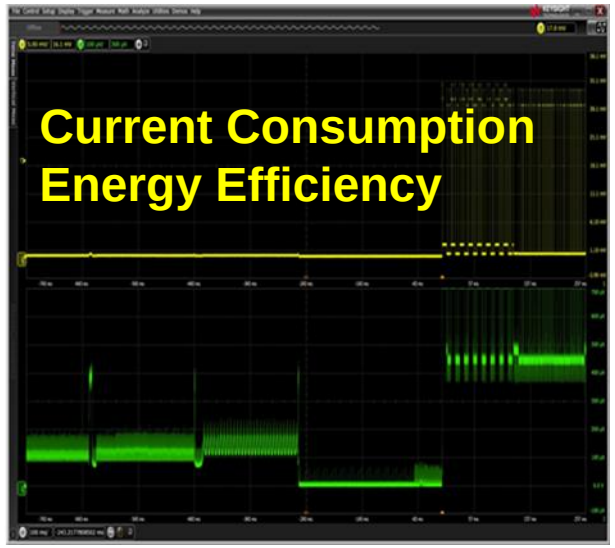
EXR With:

- Simultaneous mask testing on every channel and automatic mask generation (standard feature)



EXR With:

- 2Ghz & 6GHz Power Rail Probes (N7020A, N7024A)
- PI App--D9010POWA
- Power App-D9010PWRA
  - PSRR, etc.



EXR with:

- High-sensitivity current probes (N2820A, N2821A)

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(주)제이스

EXR 시리즈 스코프

KEY SPECIFICATION

Standard Performance

- 100 Mpts per channel memory
- 500 GB SSD
- 4 digit DVM, 10 digit counters
- Segmented / history mode
- Fault Hunter
- Eye diagrams, clock recovery
- FFT, 50+ voltage/timing measurements
- ***Training signals, auto demo modes***

Key Specifications				
Analog Channels	4 or 8, upgradeable			
Bandwidth	500 MHz → 2.5 GHz			
Sample rate	16 GSa/s			
Memory Depth	100 Mpts/ch → 400 Mpts/ch			
Update Rate	>200,000 wfm/s			
Resolution (high res)	10 bits (16 bits)			
	500 MHz	**1 GHz**	**2 GHz**	**2.5 GHz**
ENOB	8.2	8	7.6	7.5
Noise @ 1 mV/div	63 µV	73 µV	91 µV	100 µV
Logic Analysis	16 channels, separate connector			
DVM	4 digits			
Counter	2x 10 digit, 1x 8 digit			
AWG / FRA	50 MHz			

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측정솔루션 전문가그룹 (주)제이스

Hardware Configuration

Instrument Upgrades	Model
Add memory, 200/400 Mpts/ch	EXR2MEM
Add AWG, 50 MHz	EXR2WAV
Add MSO, 16 channels	EXR2MSO

Model Numbers by Bandwidth and Channels		
Bandwidth	**4 Channels**	**8 Channels**
500 MHz	EXR054A	EXR058A
1 GHz	EXR104A	EXR108A
2 GHz	EXR204A	EXR208A
2.5 GHz	EXR254A	EXR258A

Additional Equipment	Model
Extra SSD, 500 GB / 1 TB (removable)	EXR2SSD
Rackmount kit, 8U	EXR2RACK
Transit case (Case Cruzer)	3F2002-1910C [1]
BNC(m) - SMA(f) Adapters	54855-67604
GPIB adapter (ICS Electronics)	4865B [1]

1. Sold directly by the manufacturer, not by Keysight.

Calibration Options	Model
ISO 17025 Cal. (Not Accredited)	EXR000-1A7
ISO 17025 Cal. (Accredited)	EXR000-AMG

Future Upgrades	Model
Add bandwidth, up to 2.5 GHz	EXR2BW
Add analog channels, 4 to 8	EXR28CH

Software Configuration

Protocol Decode/Trigger Applications	Model
I^2C, SPI, Quad SPI, RS232/UART, I^2S, SVID, Manchester, eSPI, JTAG	D9010LSSP
USB 2.0, USB-PD, 10/100 Ethernet	D9010EMBP
CAN/CAN-FD/CAN-dbc, LIN, SENT	D9010AUTP
I^3C, SPMI, RFFE	D9010MPLP
ARINC 429, MIL-1553, SpaceWire	D9010MILP
Infiniium Basic Protocol Trigger/Decode Bundle: Includes all of the above	D9011BDLP
Automotive Ethernet	D9020AUTP

Offline Applications (PC Based)	Model
Infiniium Offline (full Infiniium UI)	D9010BSEO
EZJit Complete Offline	D9010JITO
DMBA + ASIA + PAMA Offline	D9010ASIO
Protocol Decode Offline (Protocols are split up in two packages, see datasheet)	D9010LSPO D9010HSPO

Power Applications	Model
Power Integrity (Rails, Distribution)	D9010POWA
Switch Mode Power (w/ FRA)	D9010PWRA

Signal Integrity Applications	Model
EZJit Complete: Jitter Analysis	D9010JITA
InfiniiScan Zone Triggering	D9010SCNA
De-Embedding	D9010DMBA
Equalization and Crosstalk	D9020ASIA

Advanced Applications	Model
PAM-3 and PAM-4 Analysis	D9010PAMA
User-Defined Application	D9010UDAA

Compliance Applications	Model
USB 2.0	D9010USBC
10/100 Ethernet	D9010ETHC
Automotive Ethernet	AE6900T

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