



AHEAD OF WHAT'S POSSIBLE™

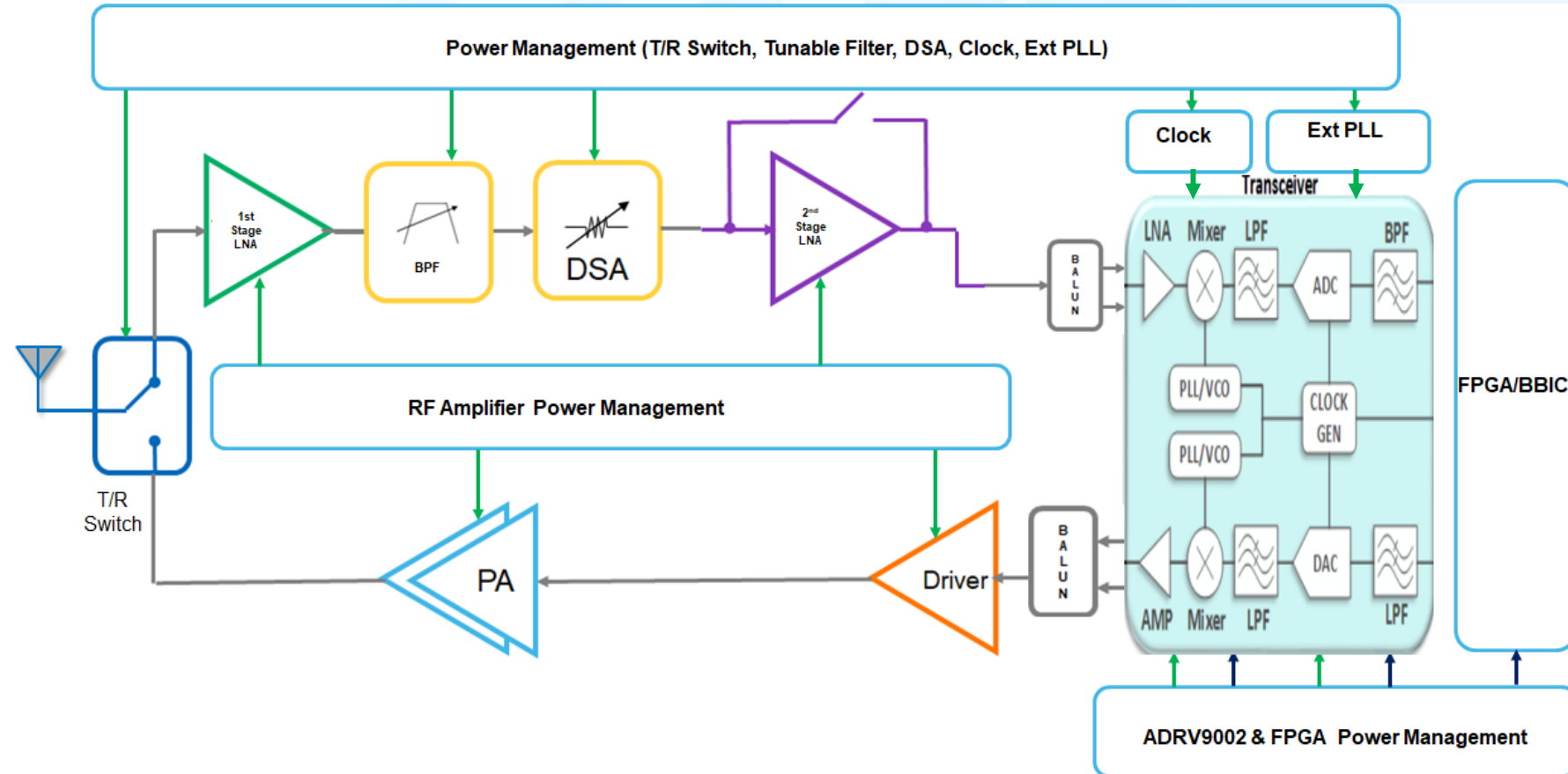
RF Front-End Design for the ADRV9002 Narrow/Wideband Transceiver

Oisin Watkins, Eamon Nash, Larry Prestia

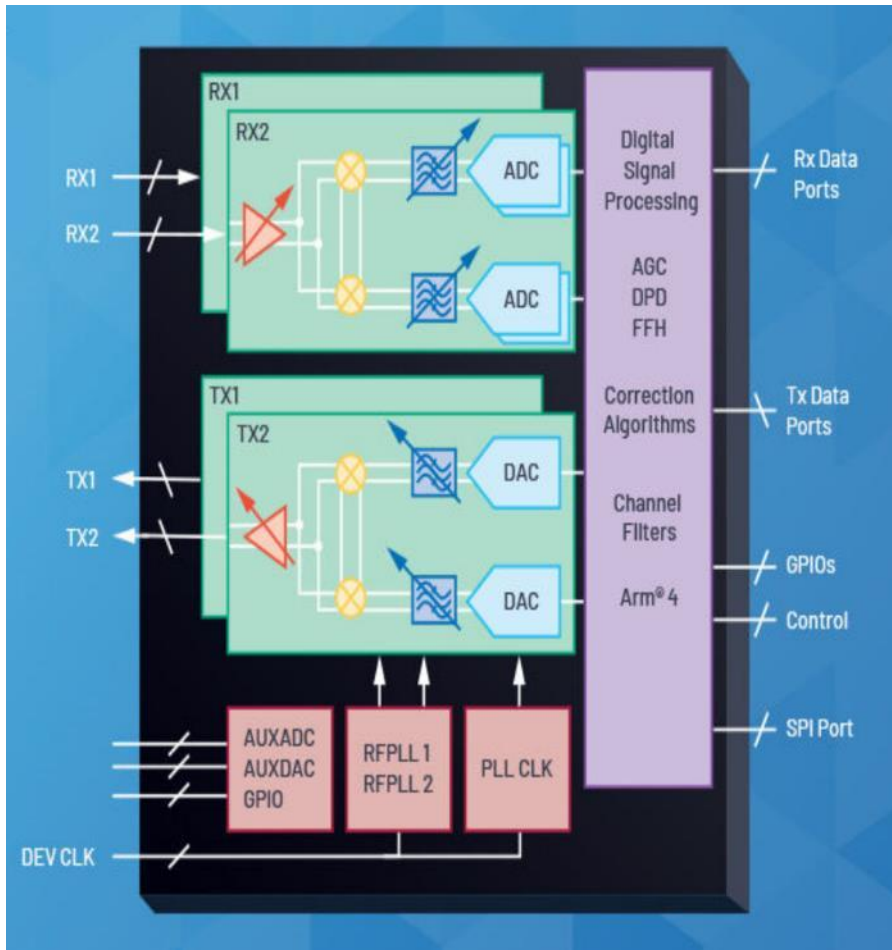
RF Front-End Design for the ADRV9002 Narrow/Wideband Transceiver

Agenda

- ▶ ADRV9002 Overview
- ▶ Low Noise Amplifiers
- ▶ Attenuators and Switches
- ▶ Tunable Filters
- ▶ Tx Amplifiers and DPD
- ▶ External LO and Clocking
- ▶ Power Management
- ▶ Summary & Conclusions
- ▶ Q&A



The ADRV9001 Family



*Land Mobile Radio
Private Mobile Radio
Tetra, P25, DMR*



*Industrial IoT
Security Network
Fixed Wireless Access
UAV / Drones / Robotics*



*Avionics
Marine Radio
Test Equipment
Long Haul Links*

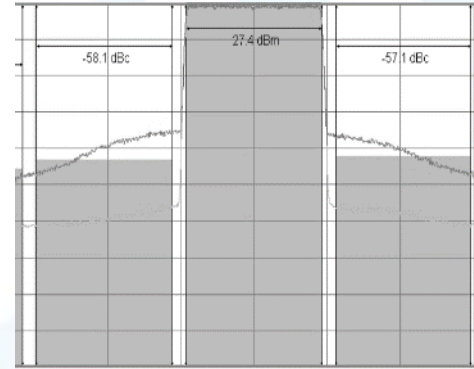
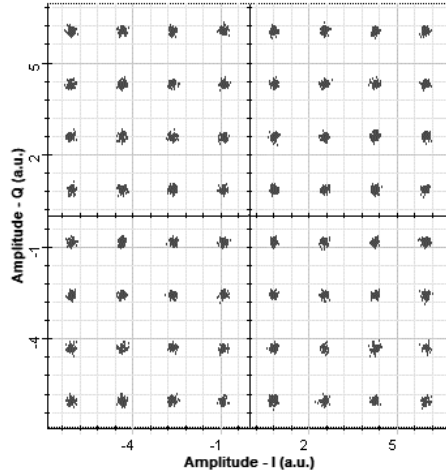
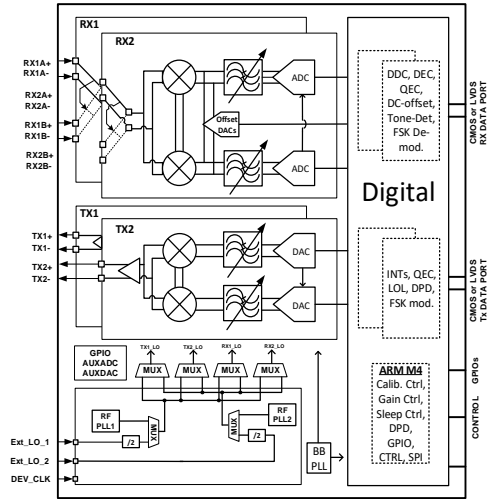


*Private LTE
CBRS Networks
LTE-M*



- ▶ **30MHz to 6GHz RF Range**
- ▶ **12KHz to 40MHz Carrier Bandwidth**
- ▶ **Optional DPD**
- ▶ **Single and Multi-Channel Options**
- ▶ **12 mm x 12 mm Package** December 2021

ADRV9002



IC / RF Performance

- Highest Linearity
- Highest TX output Power
- Lowest Integrated Phase Noise
- Best RF Sensitivity
- Flexible Digital Interface
- Integrated Digital Channel Filters
- Lowest NF, Noise Floor

RF System SW

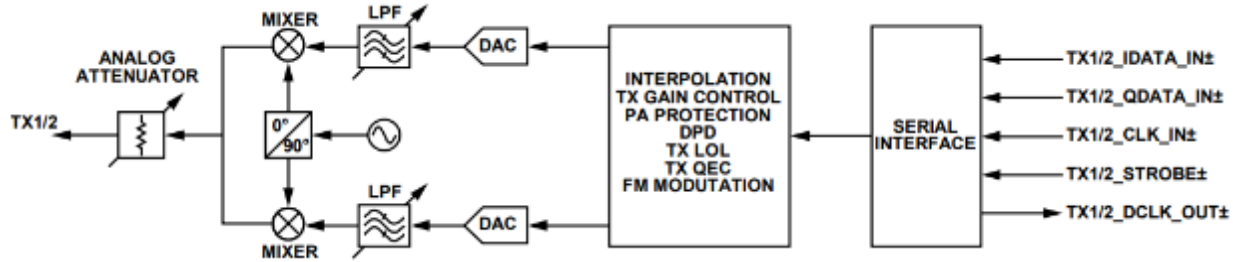
- Tx QEC
- Tx LOL Correction
- Tx Control Loops
- Rx DC Offset
- Rx QEC
- Rx Distortion Correction

System Features

- Monitor Power Modes
- Fast Freq Hopping
- Digital Pre-Distortion
- Multi Chip Synch
- Dynamic Profile Switching
- Manual or Auto AGC
- Fast Wake up Modes

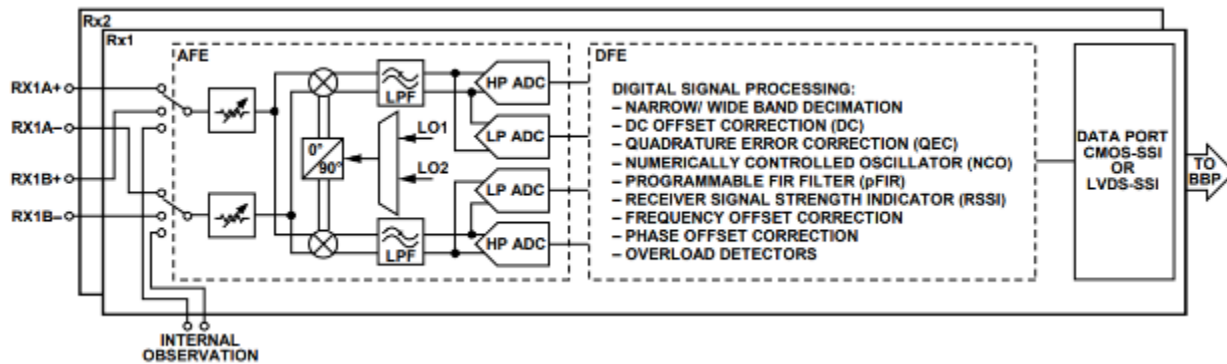


Tx / Rx Signal Chains



The ADRV9001 device integrates dual direct-conversion (Zero-IF) transmitters, capable of transmitting both narrowband (NB) and wideband (WB) signals.

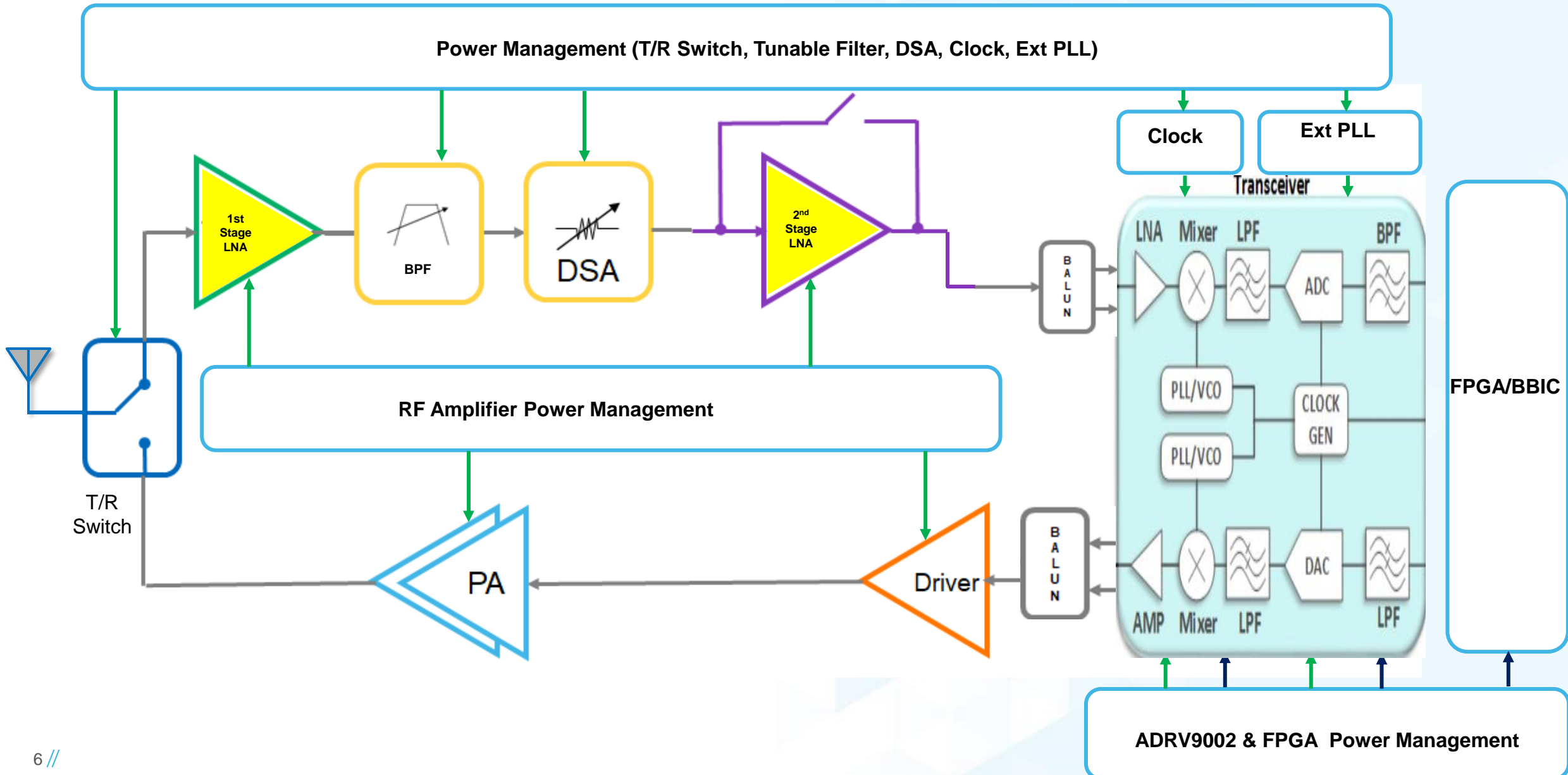
- Independent I and Q signal paths
- Separate digital filters
- DACs
- 2nd-order Butterworth LPFs
- Up-Conversion mixers.
- Analog Attenuator



The ADRV9001 offers dual receive channels. With a minimum number of external components, each receive channel could build a complete RF-to-bits signal chain.

- Support for NB and WB signals up to 40 MHz.
- Capable of supporting sample rates between 24 kHz and 61.44 MHz.

1st and 2nd Stage Low Noise Amplifiers



Low Noise Amplifiers

- Amplify Signal adding as little noise as possible
- Must be able to handle blockers
- Must be able to survive high input power levels
- Pulsed survivability can be higher than CW survivability
- May have adjustable bias Control
- Gain is usually fixed but some have bypass path
- Newer devices operate on a single positive supply

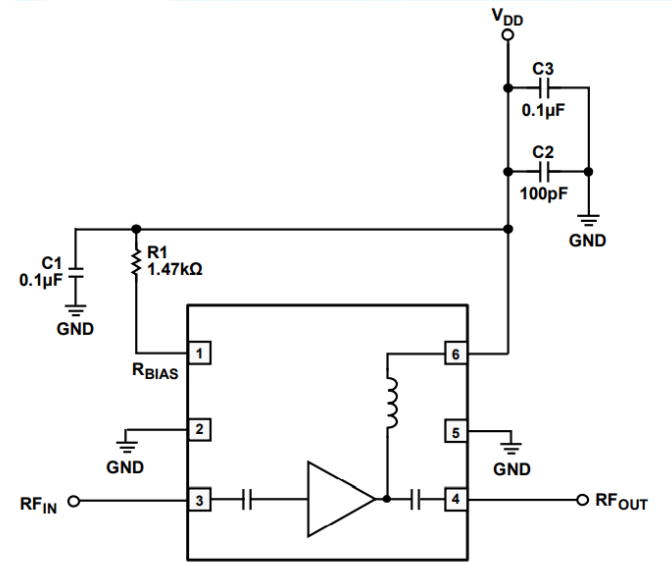
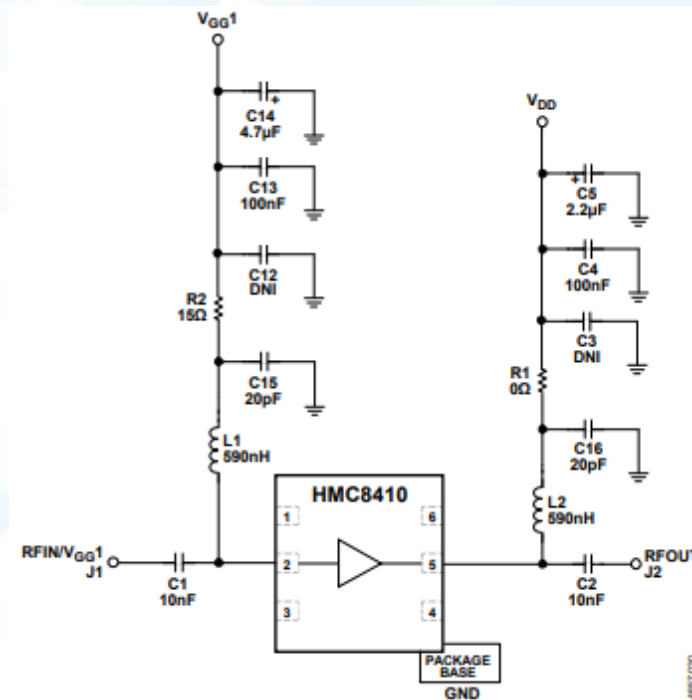


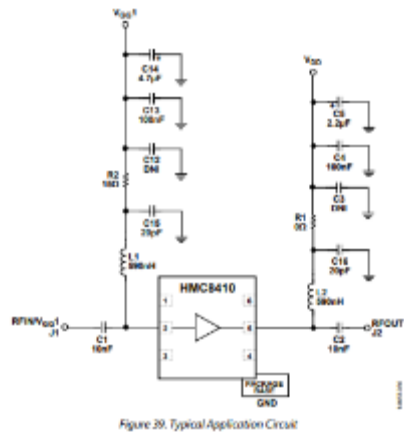
Figure 60. Typical Application Circuit



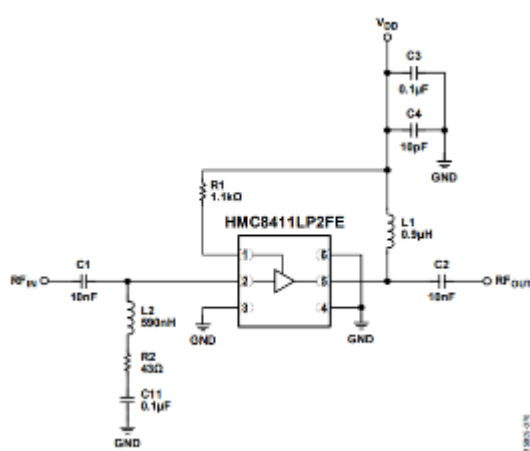
Internally Matched Wideband Low Noise Amplifiers

Part Number	Frequency (GHz)	Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	Noise Figure (dB)	V _S (V)	I _{SY} (mA)	Package (mm)	Comment
HMC8410	0.01 to 10	19.5	21	33	1.1	5	65	2 x 2 LFCSP	Wideband LNA with external gate bias control
HMC8411 ^Φ	0.01 to 10	15.5	20	34	1.7	2-6	55	2 x 2 LFCSP	Single Positive Supply, self-biased, Wideband LNA
HMC8412	0.4 to 11	15.5	19	33	1.4	5	60	2 x 2 LFCSP	Single Positive Supply, self-biased, Wideband LNA with Integrated Bias Choke
HMC8413 ^Φ	0.01 to 10	19.5	20	35	1.9	5	95	2 x 2 LFCSP	Single Positive Supply, self-biased, High OIP3, Wideband LNA (pre-release)
ADL8111	0.01 to 8	12.5	19.5	34	2.8	5	70	6 x 6 LGA	Wideband LNA w Internal and External Bypass

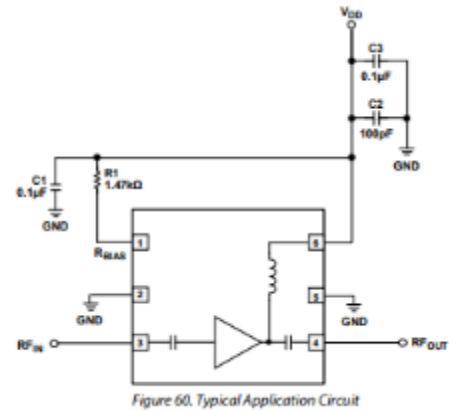
Φ – External Input Match Required



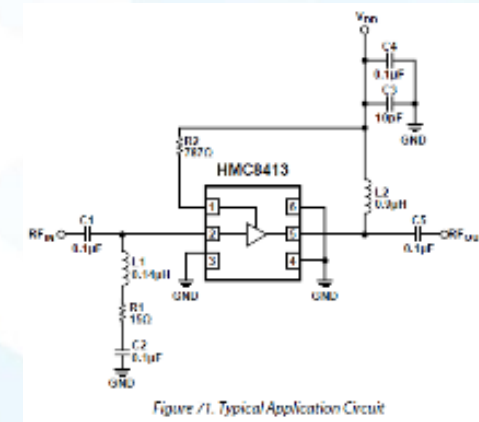
HMC8410



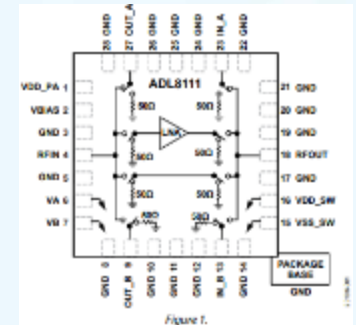
HMC8411



HMC8412

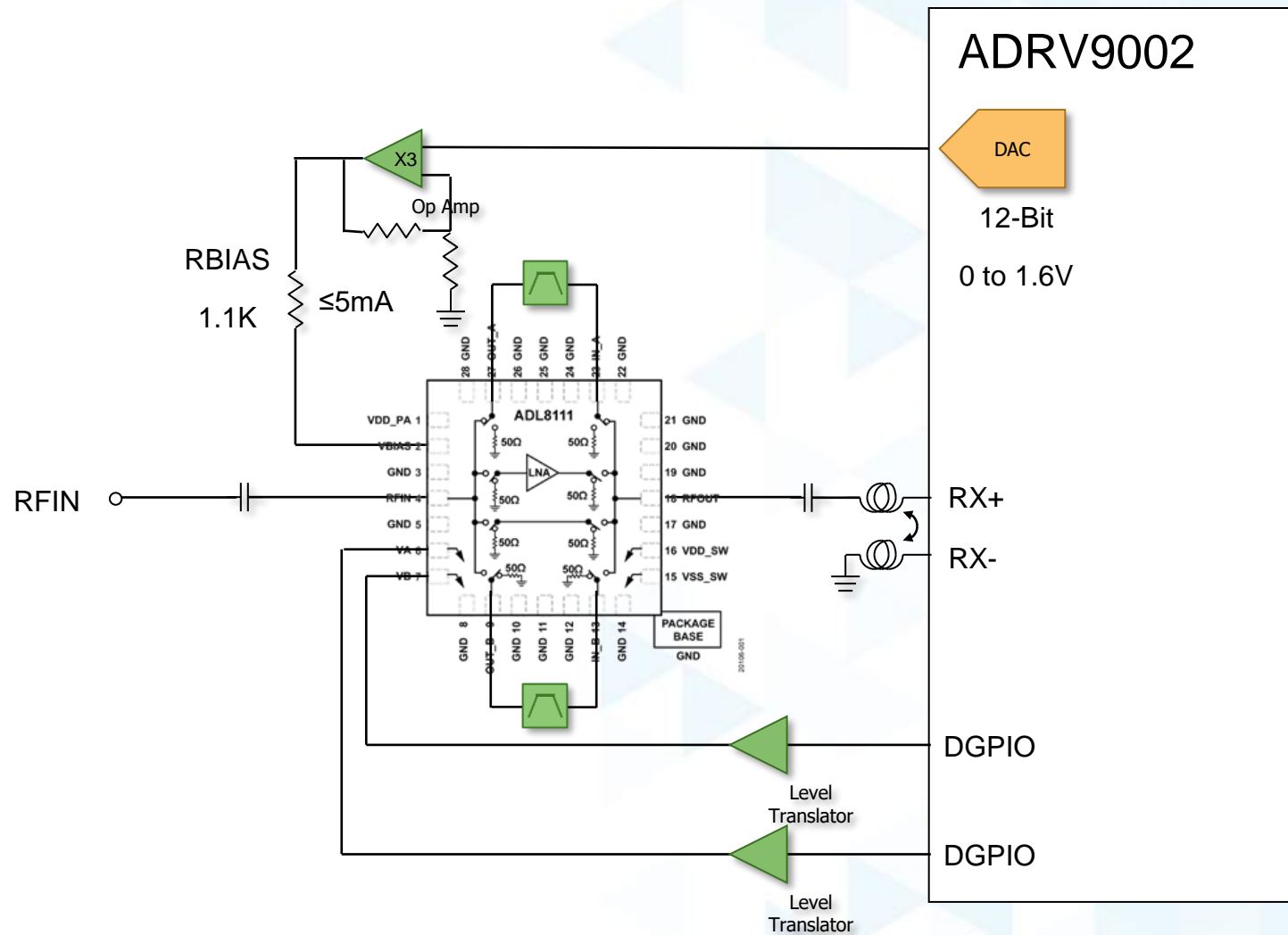


HMC8413



ADL8111

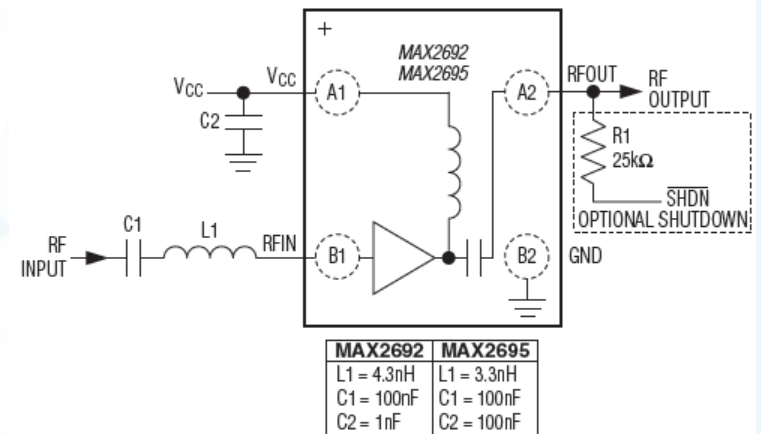
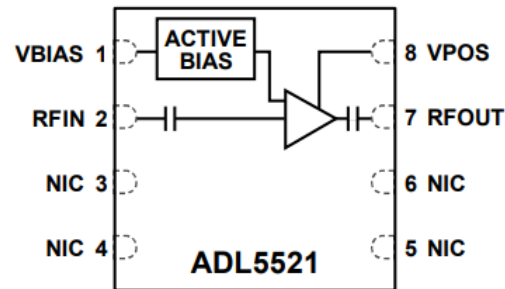
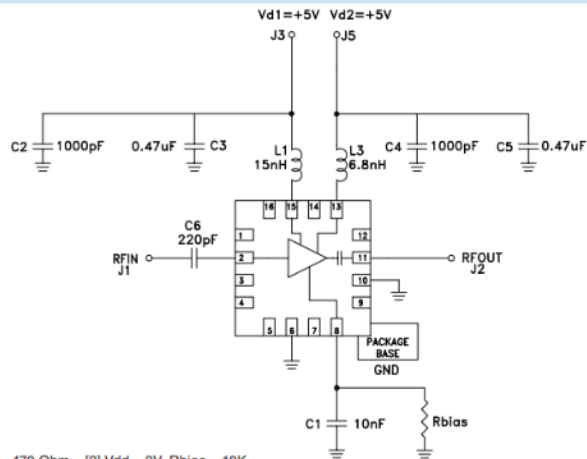
Amplifier Bias and Bypass Control from ADRV9002



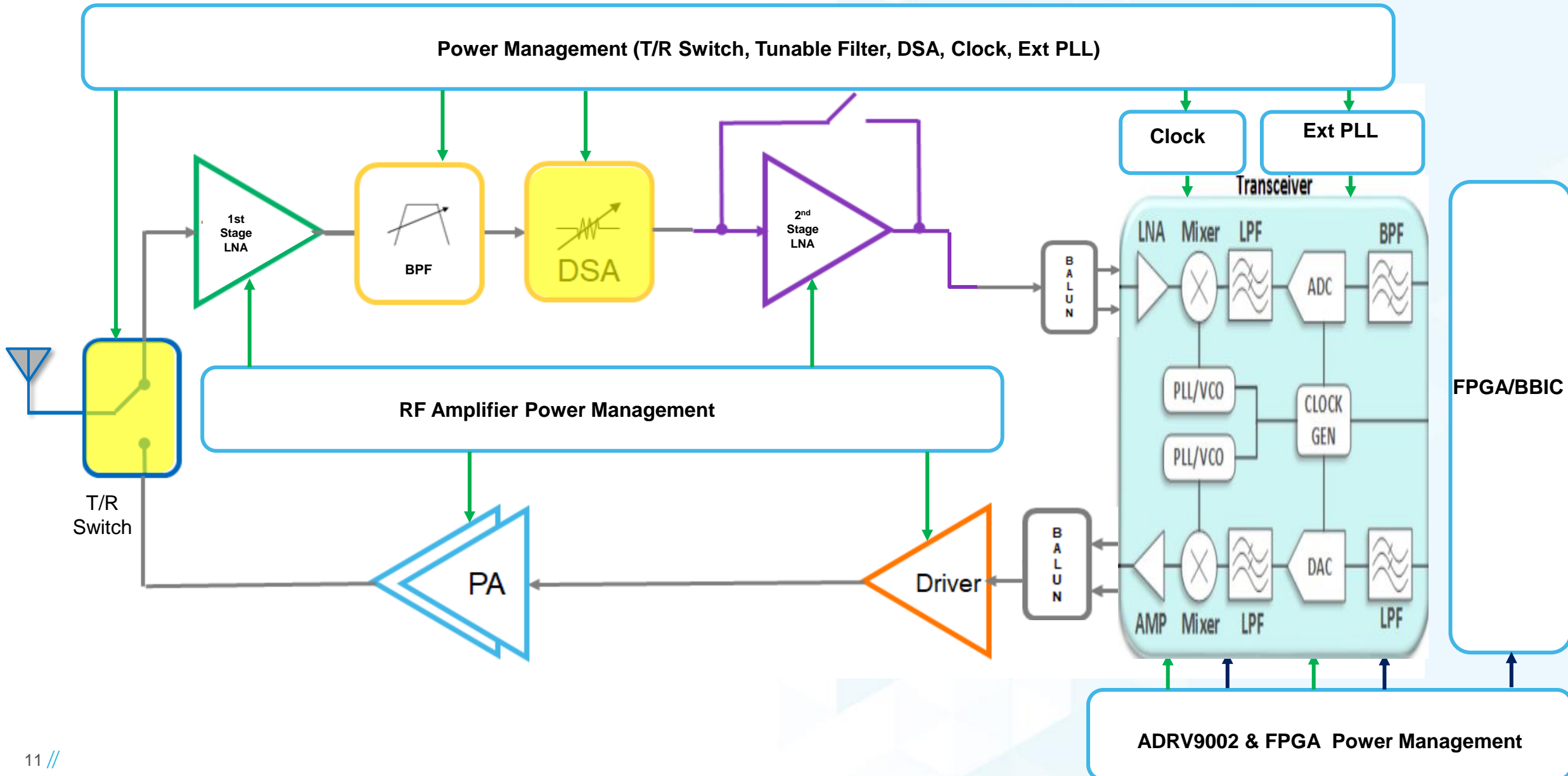
Lower Noise Figure Narrow Band LNAs

Part Number	Freq Range MHz	NF dB	Gain dB	OIP3 (dBm)	VDD (V)	IDD mA
HMC376	700 – 1000	0.7	15	36	5	73
HMC618A	1200 - 2200	0.75	19	35	3/5	117
ADL5523 ^Φ	400 – 4000	0.8	21.5	34	3/5	60
ADL5521 ^Φ	400 - 4000	0.9	20.8	37	3/5	60
HMC717A	4800 - 6000	1.1	14.5	30	3/5	68
MAX2686L ^Φ	1575 – 1610	0.88	19	15	1.6 to 4.2	5
MAX2691 ^Φ	1150 - 1300	0.93	17.5	14.5	1.6 to 3.6	4.3
MAX2692 ^Φ	2200 – 2900	1.1	18.2	15.2	1.6 to 3.6	4
MAX2659 ^Φ	1450 - 1750	0.8	20.5	15.5	1.6 to 3.6	4.1
MAX2640 ^Φ	400 -1500	0.9	15.1	5.1	2.7 to 5.5	3.5

Φ – External Input and/or Output Match Required



Variable Attenuators and Switches

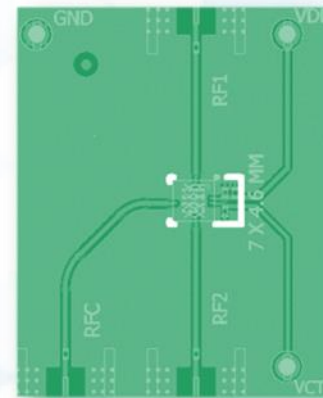


Switches and Attenuators – Critical Specifications

- **Insertion loss**
- **RF Power Survivability (average and peak) power levels**
- **Isolation**
- **Settling Time**
- **Easy-to-Use Digital Interface**
- **Silicon on Insulator (SOI) Technology offers:**
 - **Excellent Isolation and Insertion Loss**
 - **Very low DC current consumption (<1mA)**
 - **Smaller PCB area and easier biasing and control compared to discrete PIN Diodes**

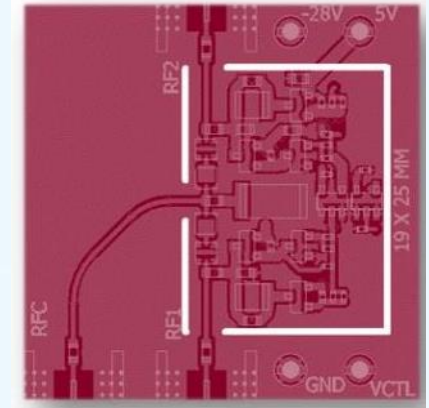


SOI Switch



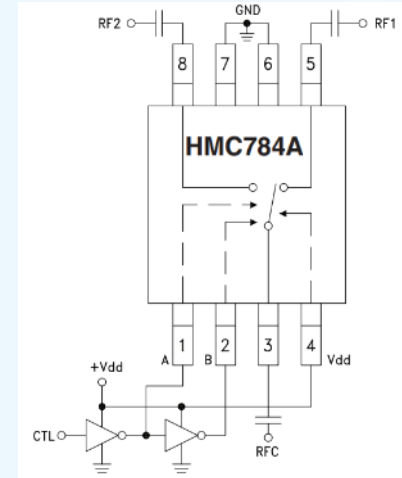
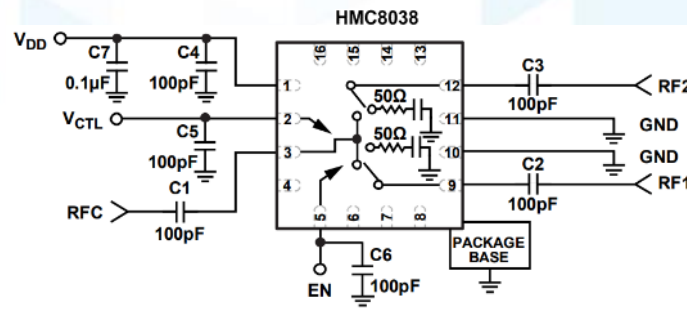
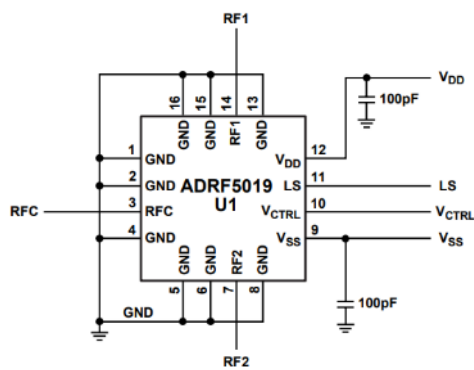
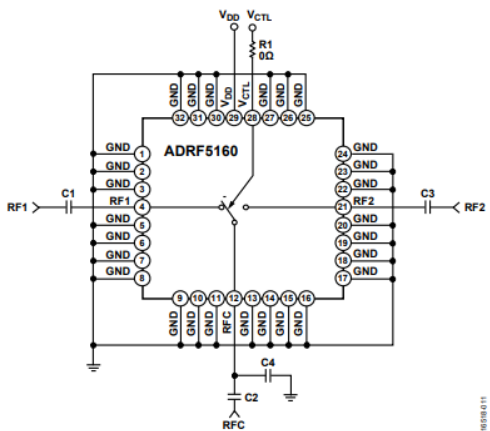
VS

Discrete PIN-Diodes



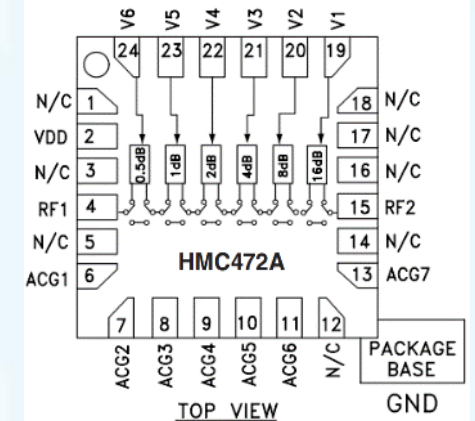
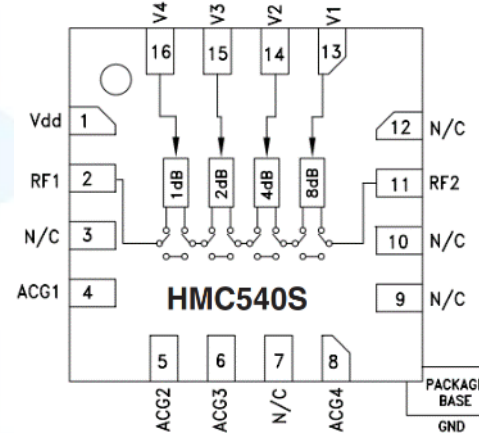
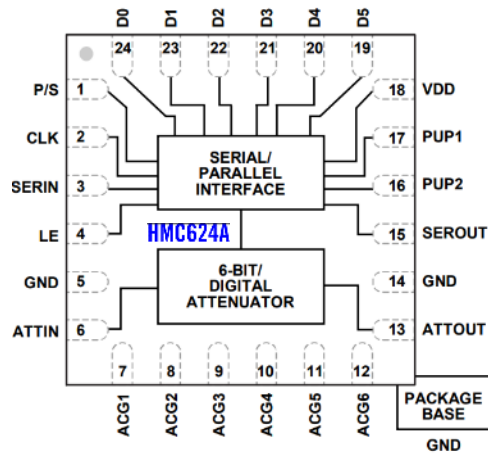
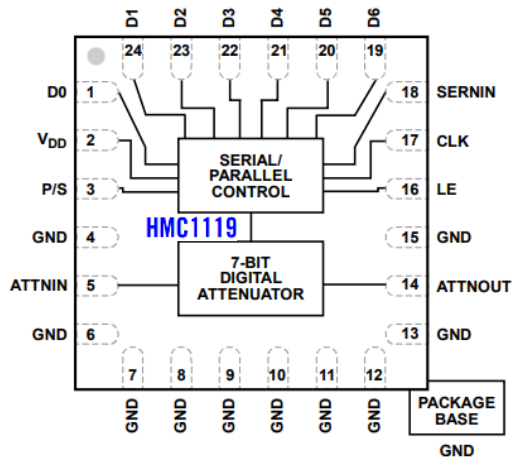
Product Recommendations for the T/R Switch (SPDT)

Part Number	Frequency (GHz)	Insertion Loss (dB)	Max Inp Power (dBm) Avg. / Peak	Input IP3 (dBm)	Isolation (dB)	Switching Speed (us)	Supply (V)	Package (mm)	Comment
ADRF5160	0.7 to 4.0	0.7	43 / 49	70	45	1.20	5	5 x 5 LFCSP	Single positive supply, SOI, narrow band, reflective
ADRF5130	0.7 to 3.8	0.7	41 / 46	65	45	0.75	5	4 x 4 LFCSP	Single positive supply, SOI, narrow band, reflective
ADRF5132	0.7 to 5.0	0.6	38 / 43	65	45	0.55	5	3 x 3 LFCSP	Single positive supply, SOI, narrow band, reflective
ADRF5019	0.1 to 13.0	0.6	35 / 38	60	50	0.15	3.3 / -2.5	3 x 3 LFCSP	Dual or single supply, SOI, absorptive
HMC1118	0.0 to 13.0	0.6	35 / 35	60	50	2.70	3.3 / -2.5	3 x 3 LFCSP	Dual supply, SOI, wideband, absorptive
HMC8038	0.1 to 6.0	0.8	31 / 34	60	60	0.15	3.3 to 5	4 x 4 LFCSP	Single positive supply, SOI, absorptive
HMC646	0.1 to 2.1	0.6	43 / 43	70	30	0.35	3 to 8	2 x 2 DFN	Single positive supply, GaAs, reflective
HMC784	0.1 to 4.0	0.6	35 / 35	60	25	0.15	3 to 8	4 x 4 MSOP8G	Single positive supply, GaAs, reflective
HMC536	0.1 to 6.0	0.6	33 / 33	50	30	0.10	3 to 5	2 x 2 DFN	Single positive supply, GaAs, reflective



Product Recommendations for Rx Variable Attenuators (DSA)

Part Number	Frequency (GHz)	Attenuation Range (dB)	Attenuation Step (dB)	Max Inp Power (dBm) Avg. / Peak	Input IP3 (dBm)	Switching Speed (us)	Supply (V)	Package (mm)	Comment
HMC1122	0.1 to 6	31.5	0.5 (6-bit)	24 / 30	55	0.15	3.3 to 5	4 x 4 LFCSP	Single positive supply, SOI
HMC1119	0.1 to 6	31.75	0.25 (7-bit)	24 / 30	54	0.15	3.3 to 5	4 x 4 LFCSP	Single positive supply, SOI
HMC624A	0 to 6	31.5	0.5 (6-bit)	27 / 33	55	0.1	3 to 5	4 x 4 LFCSP	Single positive supply, GaAs
HMC472A	0 to 3.8	31.5	0.5 (6-bits)	27 / 30	50	0.1	5	4 x 4 LFCSP	Single positive supply, GaAs
HMC540S	0.1 to 8	15	1 (4-bits)	24 / 30	55	0.15	3.3 to 5	3 x 3 LFCSP	Single positive supply, SOI
HMC305S	0.4 to 7	15.5	0.5 (5-bit)	25 / 28	50	0.15	3.3 to 5	4 x 4 LFCSP	Single positive supply, SOI
HMC792A	0 to 6	15.75	0.25 (6-bits)	22 / 28	53	0.15	3 to 5	4 x 4 LFCSP	Single positive supply, GaAs
HMC468A	0 to 6	7	1 (3-bits)	26 / 26	55	0.1	5	3 x 3 LFCSP	Single positive supply, GaAs



Low Frequency Operation

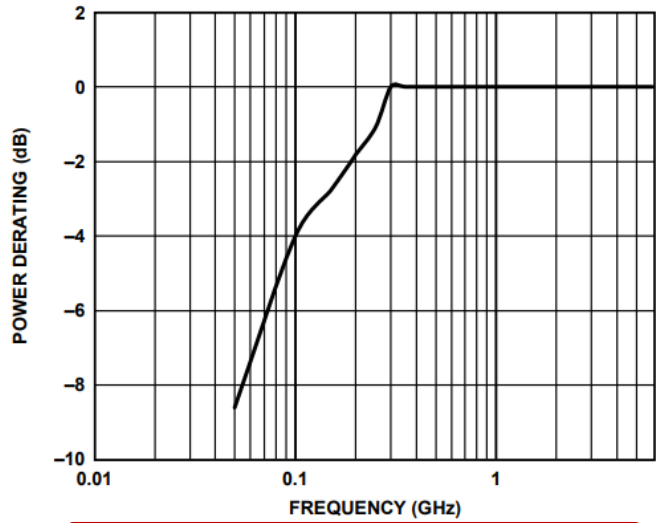
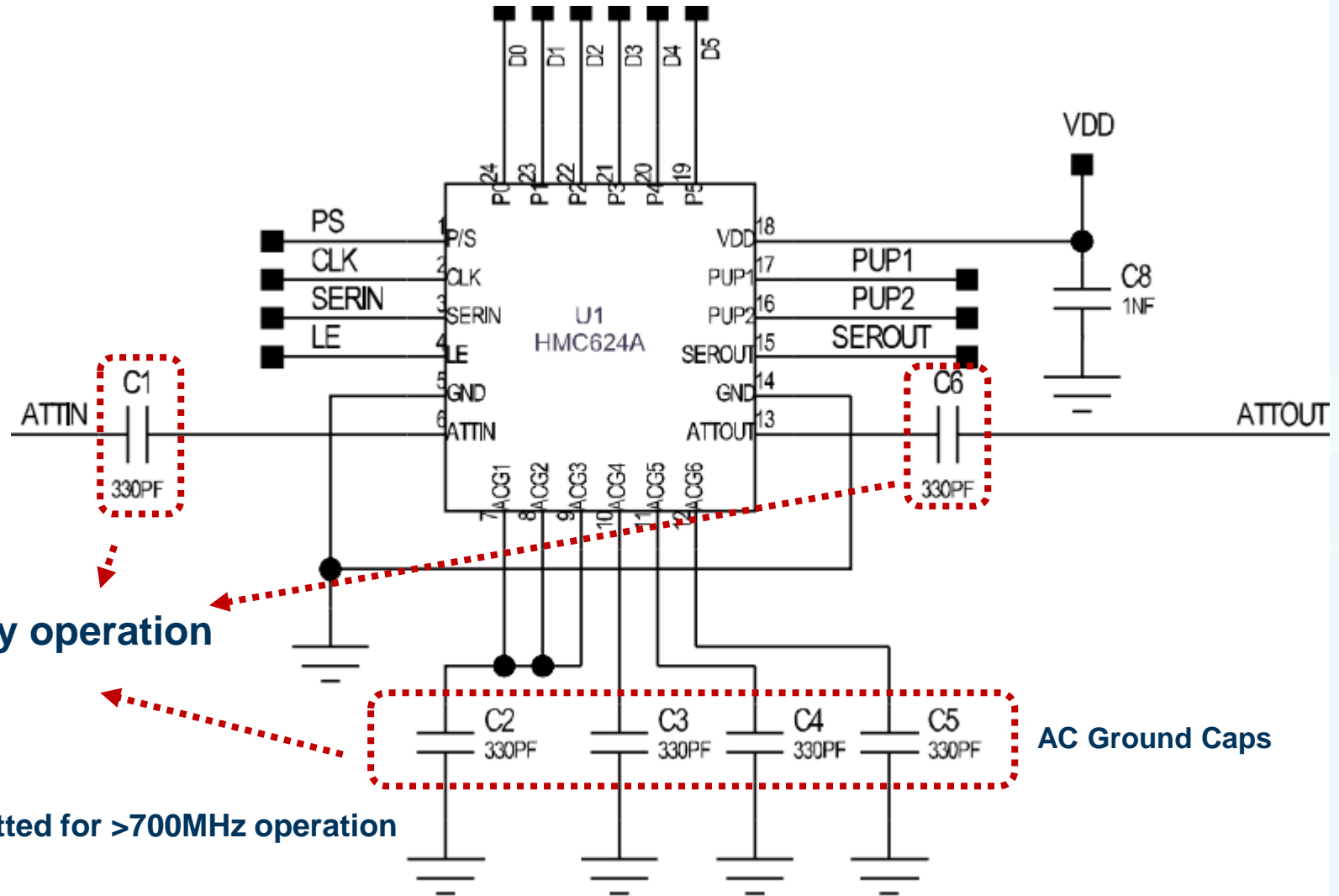


Figure 2. Power Derating at Frequencies Less Than 250 MHz

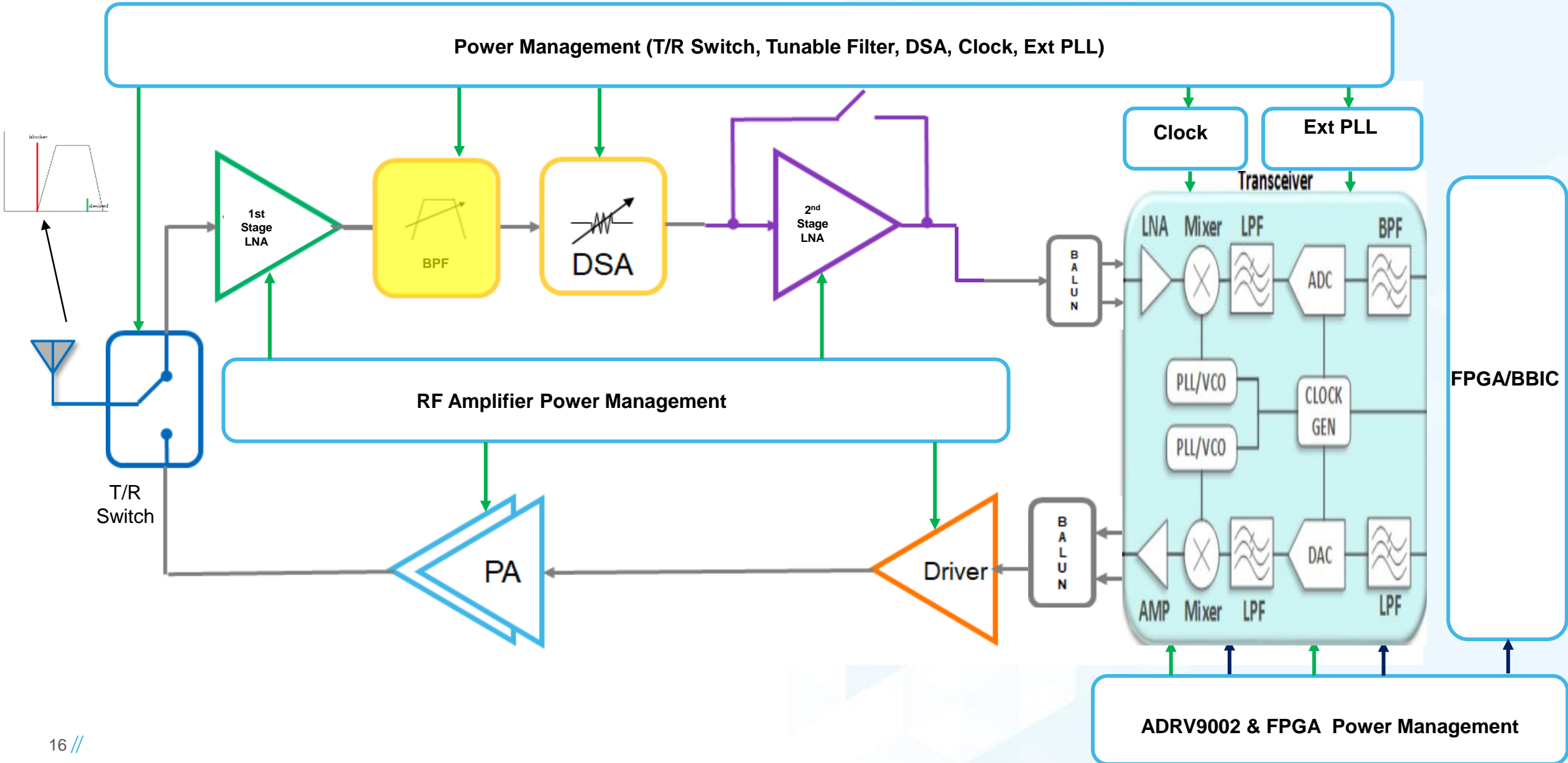
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Larger caps for lower frequency operation

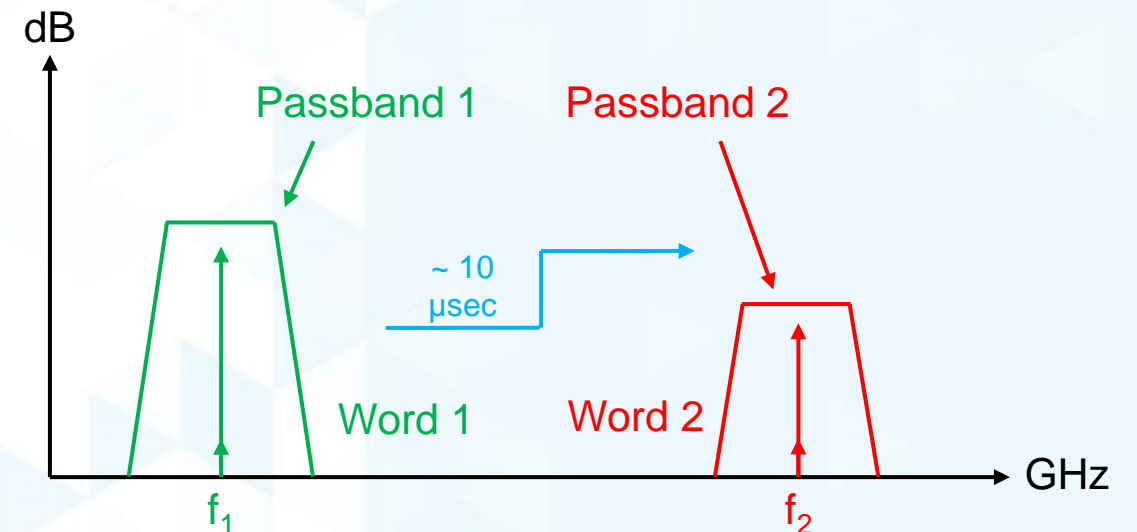
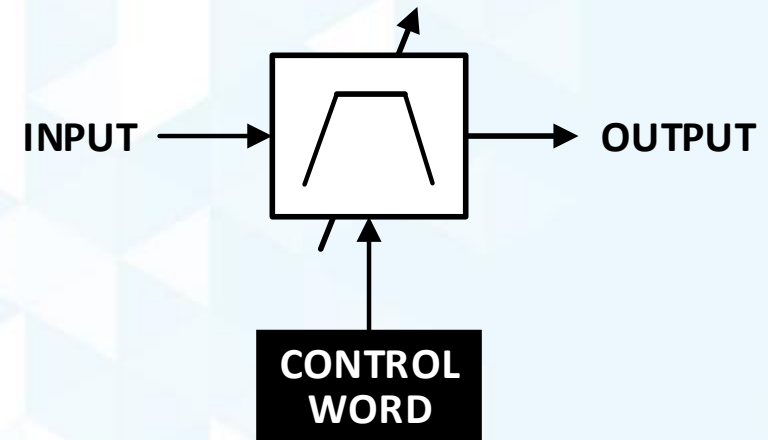
ACG Caps can be omitted for >700MHz operation

Tunable Filters

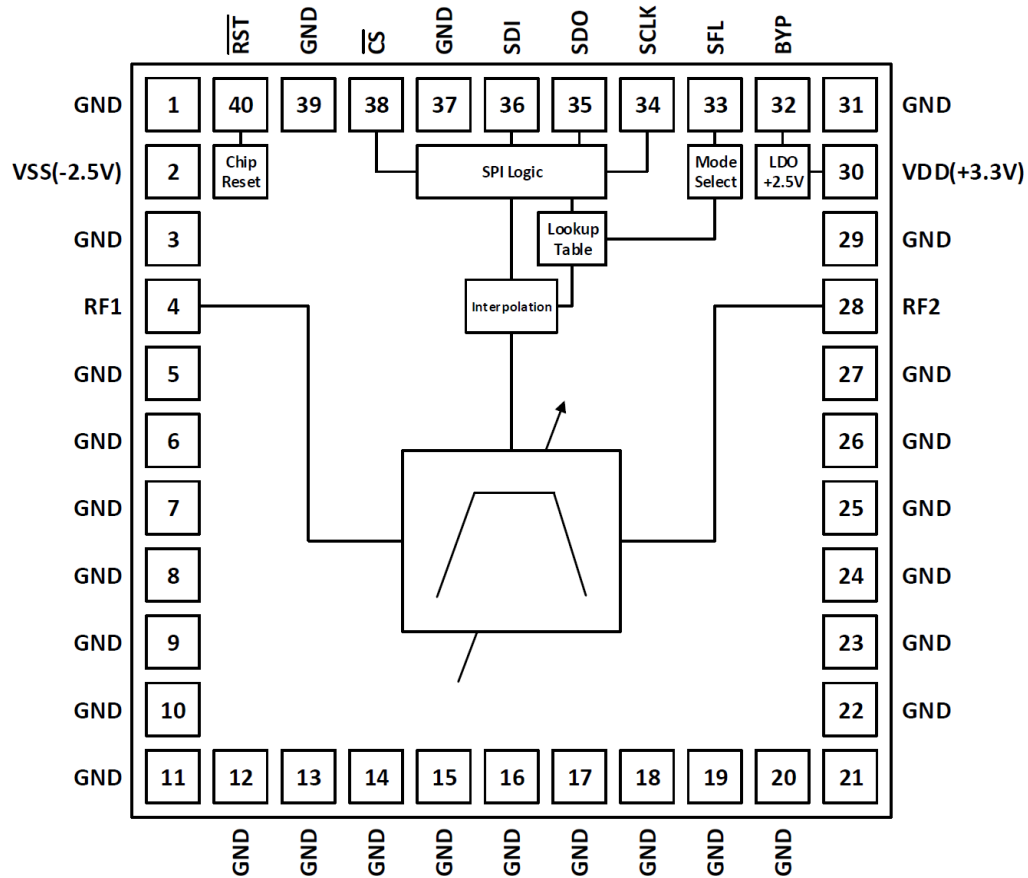


New Digitally Tunable Solutions

- ▶ Utilizes an enhanced semiconductor process with digital capabilities
- ▶ Industry friendly packaging techniques
- ▶ Small and compact
- ▶ Low power consumption
- ▶ Easy system implementation
- ▶ Highly flexible and reconfigurable
- ▶ Simple SPI logic programming
- ▶ On-chip lookup tables for fast frequency hopping
- ▶ Extremely low residual phase noise performance
- ▶ Fast RF switching speeds



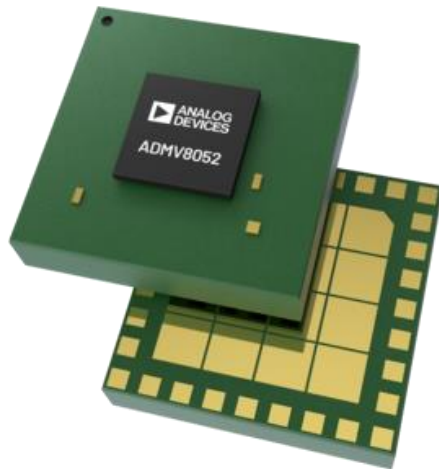
ADMV8526 (1.25 to 2.60GHz Band-Pass Filter)



- ▶ **Function:** BPF
- ▶ **Coverage:** 1.25 to 2.60 GHz
- ▶ **BW:** 9% ± 2% typical
- ▶ **Tuning:** patent pending interpolation technique
- ▶ **Control:** SPI interface
- ▶ **IL:** 4dB
- ▶ **20dB Rejection:** 12% from f_{3dB}
- ▶ **Input IP3:** > 40dBm
- ▶ **Residual phase noise:** -165 dBc/Hz
- ▶ **Power consumption:** 200μW
- ▶ **SPI fast latch:** capability for quickly sequencing through 32 state LUT

Tunable Bandpass Filter Family for ADRV9002

Part Number	Center Frequency (MHz)	Insertion Loss (dB) - typical	Output IP3 (dBm) - typical	Return Loss (dB)	V _s (V)	Power Consumption (mW)	Tunable Bandwidth (%)	Package (mm)	Comment
ADMV8052	30 to 520	5	45	20	3.3 & -2.5	<1	5~11	22 x 22 x 5.7 LGA	Tunable bandpass filter with sub-band controls of center frequency from 30MHz~520MHz
ADMV8501	30 to 90	6	45	20	3.3 & -2.5	<1	5~11	10 x 10 x 2.86 LGA	Tunable bandpass filter with center frequency from 30MHz~90MHz
ADMV8502	90 to 225	3.5	45	20	3.3 & -2.5	<1	5~11	10 x 10 x 2.86 LGA	Tunable bandpass filter with center frequency from 90MHz~225MHz
ADMV8505	225 to 520	4.2	45	20	3.3 & -2.5	<1	5~11	10 x 10 x 2.86 LGA	Tunable bandpass filter with center frequency from 225MHz~520MHz
ADMV8513	520 to 1,300	4.2	45	20	3.3 & -2.5	<1	5~11	10 x 10 x 2.1 LGA	Tunable bandpass filter with center frequency from 520MHz~1.3GHz
ADMV8526	1,250 to 2,600	4.2	45	20	3.3 & -2.5	<1	5~10	10 x 10 x 2 LGA	Tunable bandpass filter with center frequency from 1.25~2.6GHz



ADMV8052

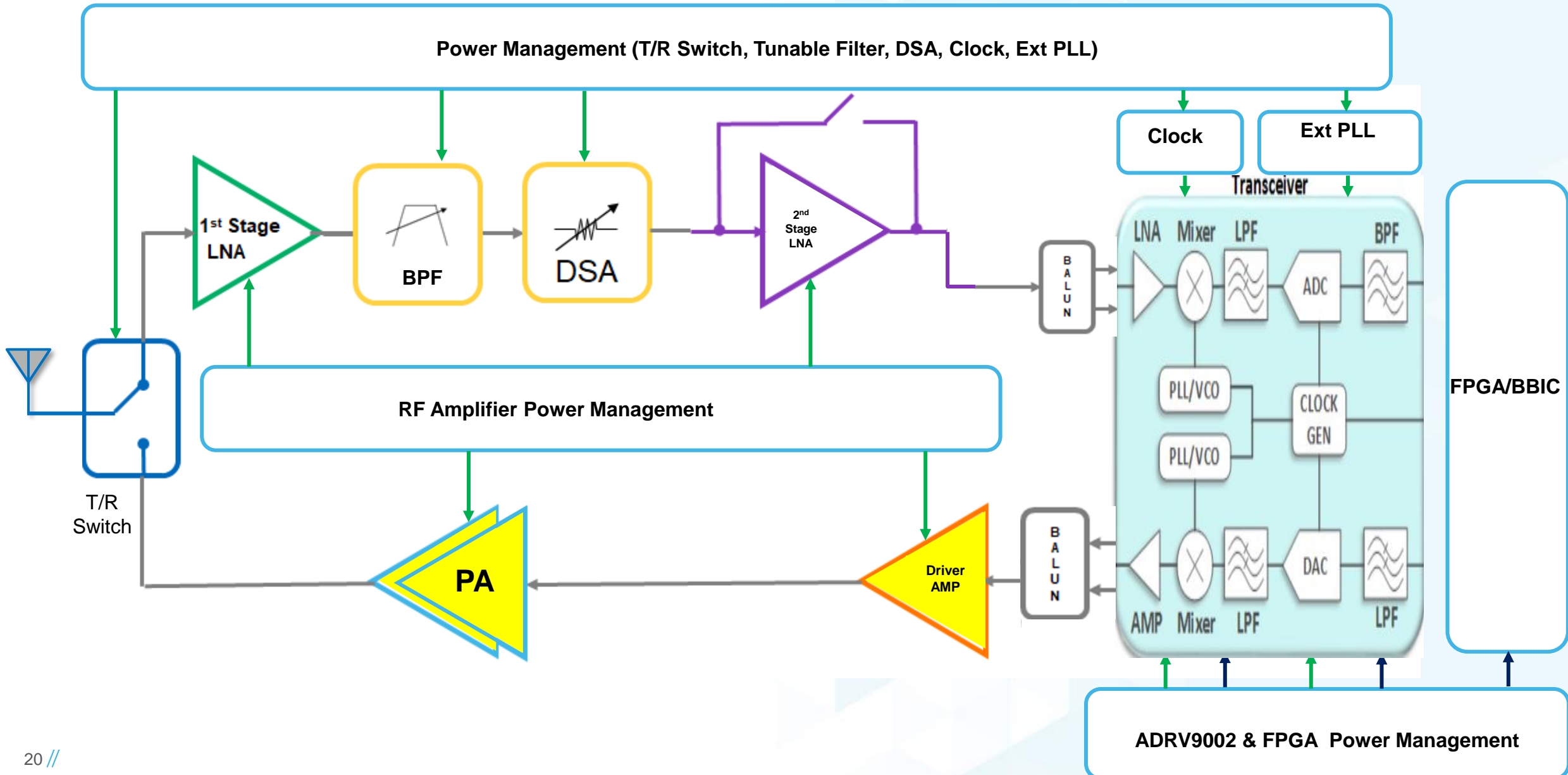


ADMV8526



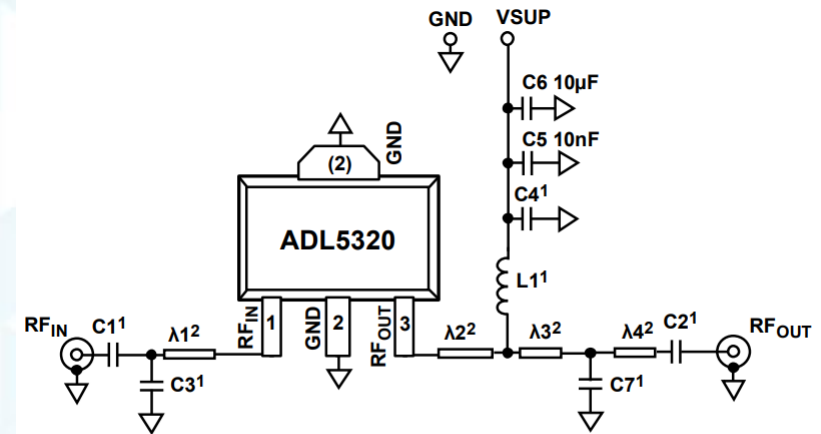
ADMV8501/8502/8505/8513/8526-EVALZ

Driver Amplifiers and Power Amplifiers



Gain Blocks and Driver Amplifiers

- **OP1dB: 15 dBm to 25 dBm**
- **OIP3: 30 dBm to 40 dBm**
- **Noise Figure: 3 dB to 5 dB (less critical)**
- **Pout: 5 dBm to 15 dBm**
- **Critical to understand expected output power level and operating mode (saturated or backed off)**
- **Matching may be internal external or integrated**
- **Narrow band devices with external matching tend to have higher performance**
- **Avoid devices with integrated distortion cancellation when doing DPD**



¹SEE TABLE 6 FOR FREQUENCY SPECIFIC COMPONENTS.
²SEE TABLE 7 FOR RECOMMENDED COMPONENT SPACING.

Figure 34. Basic Connections

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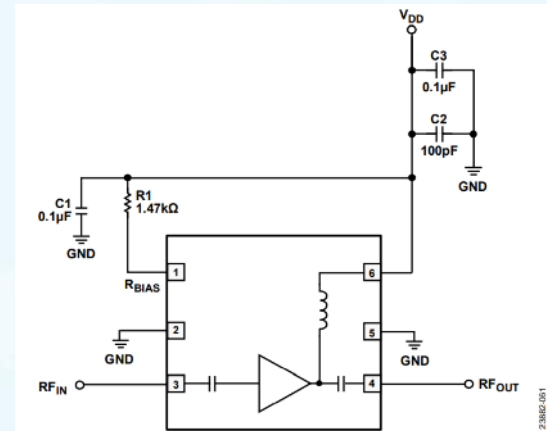


Figure 60. Typical Application Circuit

2386C.001

Driver Amplifiers for ADRV9002

Part Number	Description	Freq (GHz)	Gain (dB)	OP1dB (dBm)	OIP3 (dBm)	V _s (V)	I _{sy} (mA)
HMC8413	Single Positive Supply, self-biased, High OIP3, Wideband LNA (pre-release)	0.01 to 10	19.5	20	35	5	95
HMC453	1.6 Watt Driver Amplifier/Power Amplifier SMT, 0.4 - 2.2 GHz	0.4 to 2.17	31.5	21	47	5	725
HMC413	Driver Amplifier/Power Amplifier SMT, 1.6 - 2.2 GHz	1.6 to 2.2	23	27	40	5	270
HMC409	1 Watt Driver Amplifier/Power Amplifier SMT, 3.3 - 3.8 GHz	3.3 to 3.8	30	31	45.5	5	615
HMC408	1 Watt Driver Amplifier/Power Amplifier SMT, 5.1 - 5.9 GHz	5.1 to 5.9	20	30	43	5	750
ADL5320	Externally Matched Driver self-biased	0.4 to 2.7	13.2	26	42	3.3/5	47
ADL5324	Externally Matched 0.5 W driver amp	0.4 to 4	14	29	44	3.3	60
HMC8411	Single Positive Supply, self-biased, Wideband LNA	0.01 to 10	15.5	20	34	2-6	55

- For applications using DPD, avoid devices with internal active linearization (large OP1dB to OIP3 delta)
- Quiescent current (shown) will generally increase with RF Output Power

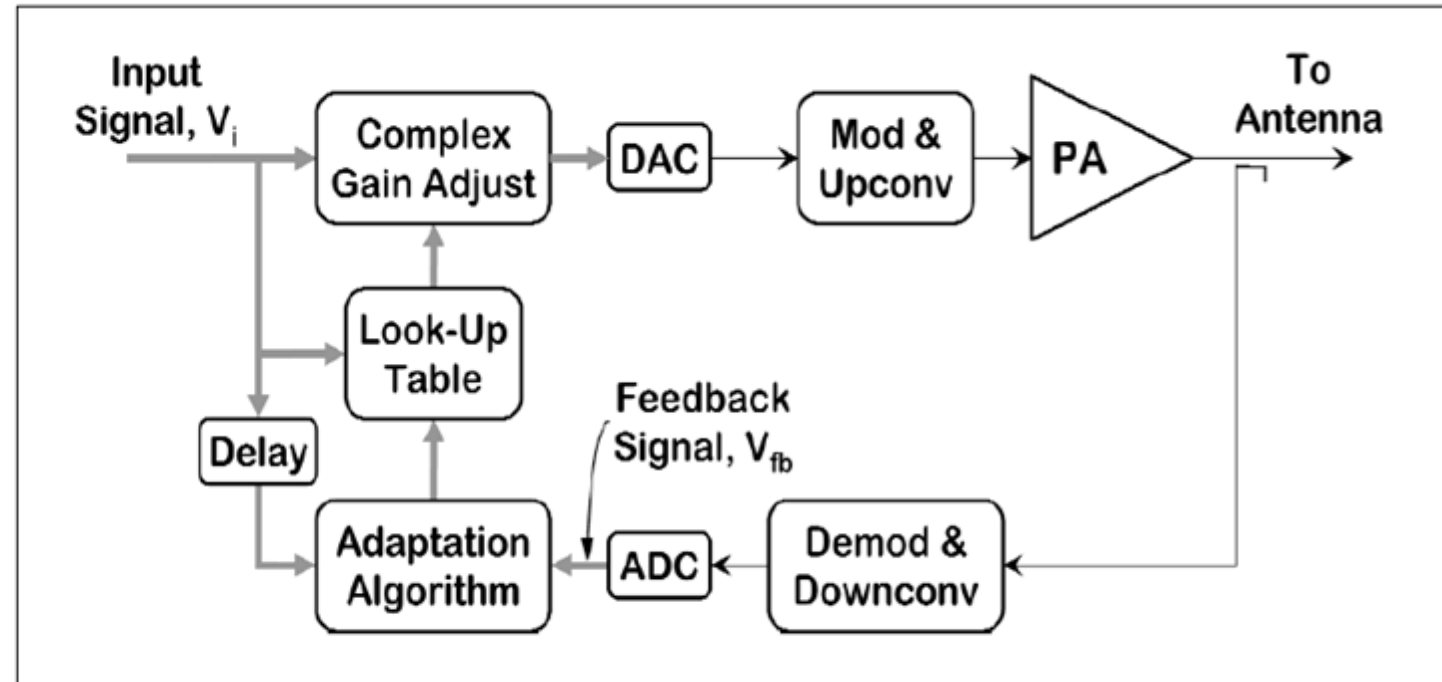
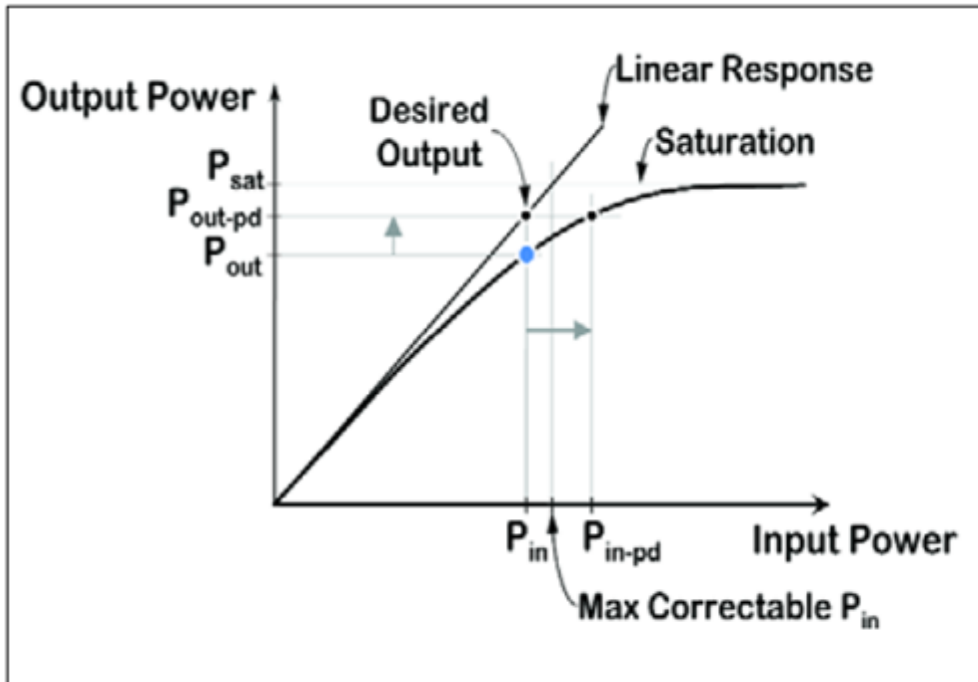
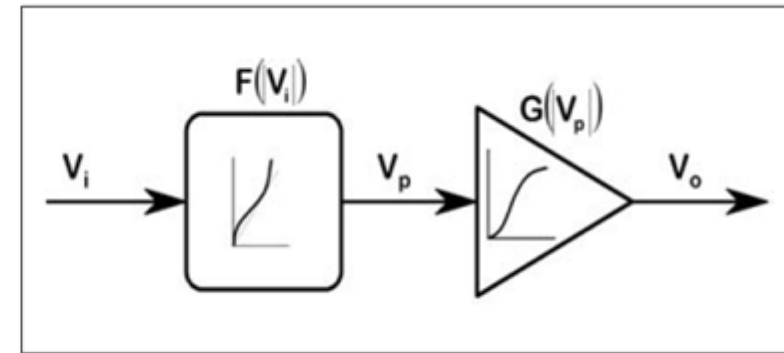
Power Amplifiers for ADRV9002

P/N	Freq Band	P_{SAT} /OP1dB (dBm)	Gain (dB)	OIP3 (dBm)	V_{DD}/I_{DQ} (V/A)
HMC1099	UHF (30-300 MHz)	40.5	18.5	49	28/0.1
ADPA1105	L-Band (1-2 GHz)	46	34.5	N/A	50/0.4
HMC1114	S-Band (2-4 GHz)	43	34.5	42.5	28/0.15
HMC1121	C-Band (4-8 GHz)	36.5	28	44	7/2.2
ADPA1107	C-Band (4-8 GHz)	45	30.5	N/A	28/0.35
HMC637A	Wideband	28 (OP1dB)	15.5	44	12/0.4
HMC8205B	Wideband	45.5	19	50	50/1.3
ADPA9002	Wideband	29 (OP1dB)	15	43	12V/385mA

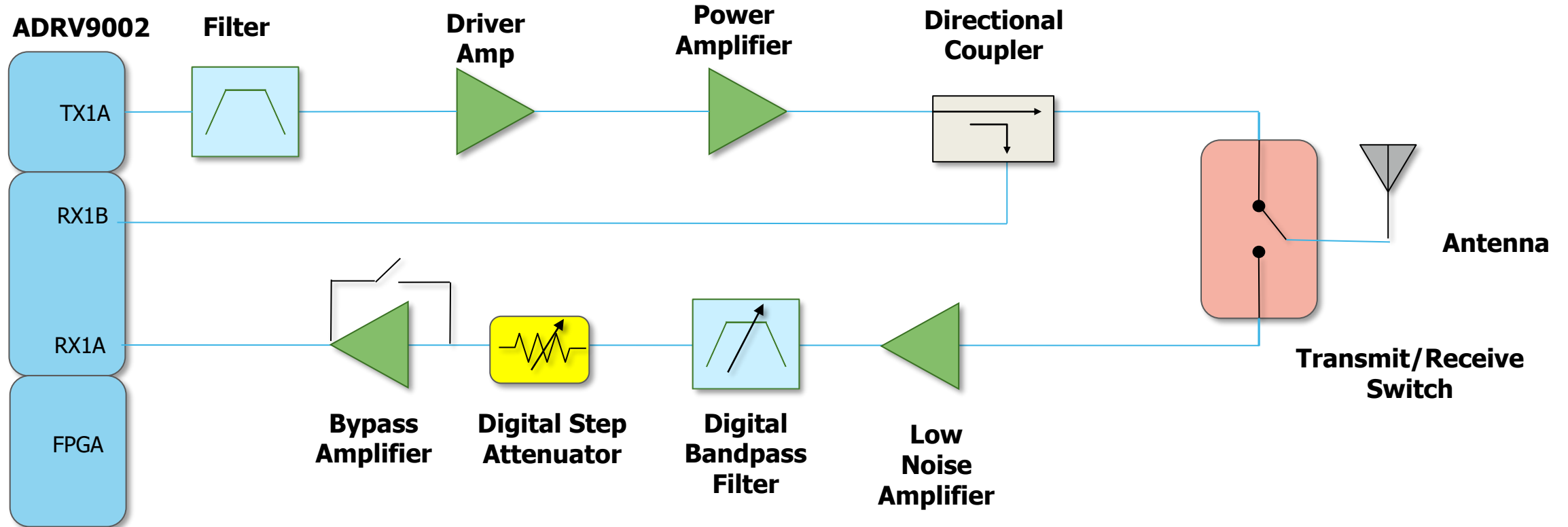
- Quiescent current (shown) will generally increase with RF Output Power

How Digital Predistortion Works

Phase and gain adjustments of the power amplifier's non-linear region are fed back and corrected in the baseband

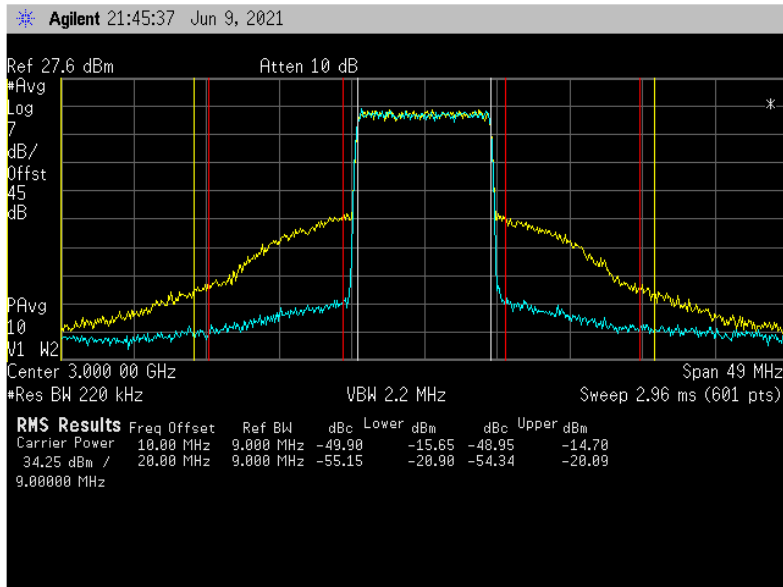


ADRV9002 Signal Chain with Digital Predistortion



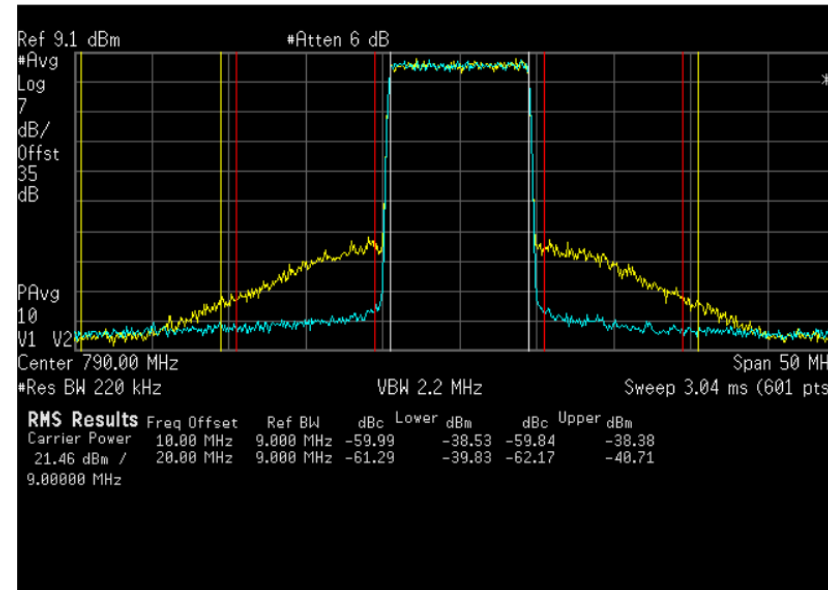
Digital Predistortion – ACPR Before and After DPD

ADI GaN PA – HMC1114 -10W



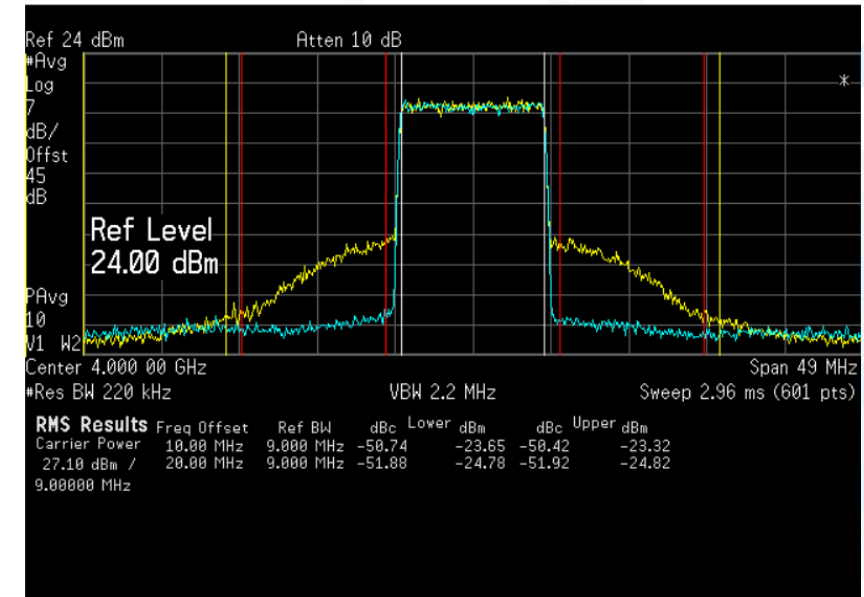
3 GHz

ADI GaAs PA – HMC637 -1W



790 MHz

Skyworks Si HBT PA – SKY66292-11
4 Watts



4 GHz

Approx. 19dB ACP improvement in all cases

9MHz Carrier BW (LTE), 15.36 MSPS

DPD Configuration using TES (Transceiver Evaluation Software)

Connect

Connection

Device Configuration **Device connected.**

Initialization

Rx Gain Control

Rx Overview

Tx Overview

TCP IP Connection

TCP IP Address 192 . 168 . 1 . 10

Port Number 55557

Setup Modulation

Configure Transmit Receive GPIO Gain Control Attenuation Control Power Savings and Monitor Mode TDD Enablement Delays Automated TDD

Connection

Device Configuration

Board Configuration

Clocks

Carriers

Radio

Advanced Features

Initial Calibrations

Rx Filters

Tx Filters

Rx Overview

Tx Overview

Device

Product ADRV9002 (2T2R) Duplex TDD Frequency Units Kiloherzt Megahertz

Setup LTE Channels Channel 1 Valid

Channel 1

SS1 Type LVDS

Number of Lanes 2-Lane

Data Rate Double

Channel 2

SS1 Type LVDS

Number of Lanes 2-Lane

Data Rate Double

Rx1

Signal Type I/Q

Dataport Sample Rate 1.92 MSPS

Rx RF Input Rx1A

RF Channel Bandwidth 1.008 MHz

Rx2

Signal Type Disabled

Dataport Sample Rate 1.92 MSPS

Rx RF Input Rx2A

RF Channel Bandwidth 1.008 MHz

Tx1

Signal Type I/Q

Dataport Sample Rate 1.92 MSPS

Tx2

Signal Type Disabled

Dataport Sample Rate 1.92 MSPS

Setup Carrier

File View Sample Code Connect Program Log File

Configure Transmit Receive GPIO Gain Control Attenuation Control Power Savings and Monitor Mode TDD Enablement Delays Automated TDD

Connection

Device Configuration

Board Configuration

Clocks

Carriers

Radio

Advanced Features

Initial Calibrations

Rx Filters

Tx Filters

Rx Overview

Tx Overview

Carrier Configuration Mode Defined Carrier Frequencies

PLL Retuning

Allow PLL retuning when switching between Tx and Rx

Rx1 (Driven by LO1)

Carrier Frequency 900 MHz

Rx2 (Off)

Carrier Frequency 900 MHz

Tx1 (Driven by LO1)

Carrier Frequency 900 MHz

Tx2 (Off)

Carrier Frequency 900 MHz

LO1 Source Internal

LO2 Source Internal

Internal LO1 (Driving Tx1, Rx1)

PLL1 Power Consumption Low Power

LO1 Optimization Best Power Consump

PLL1 Calibration Normal

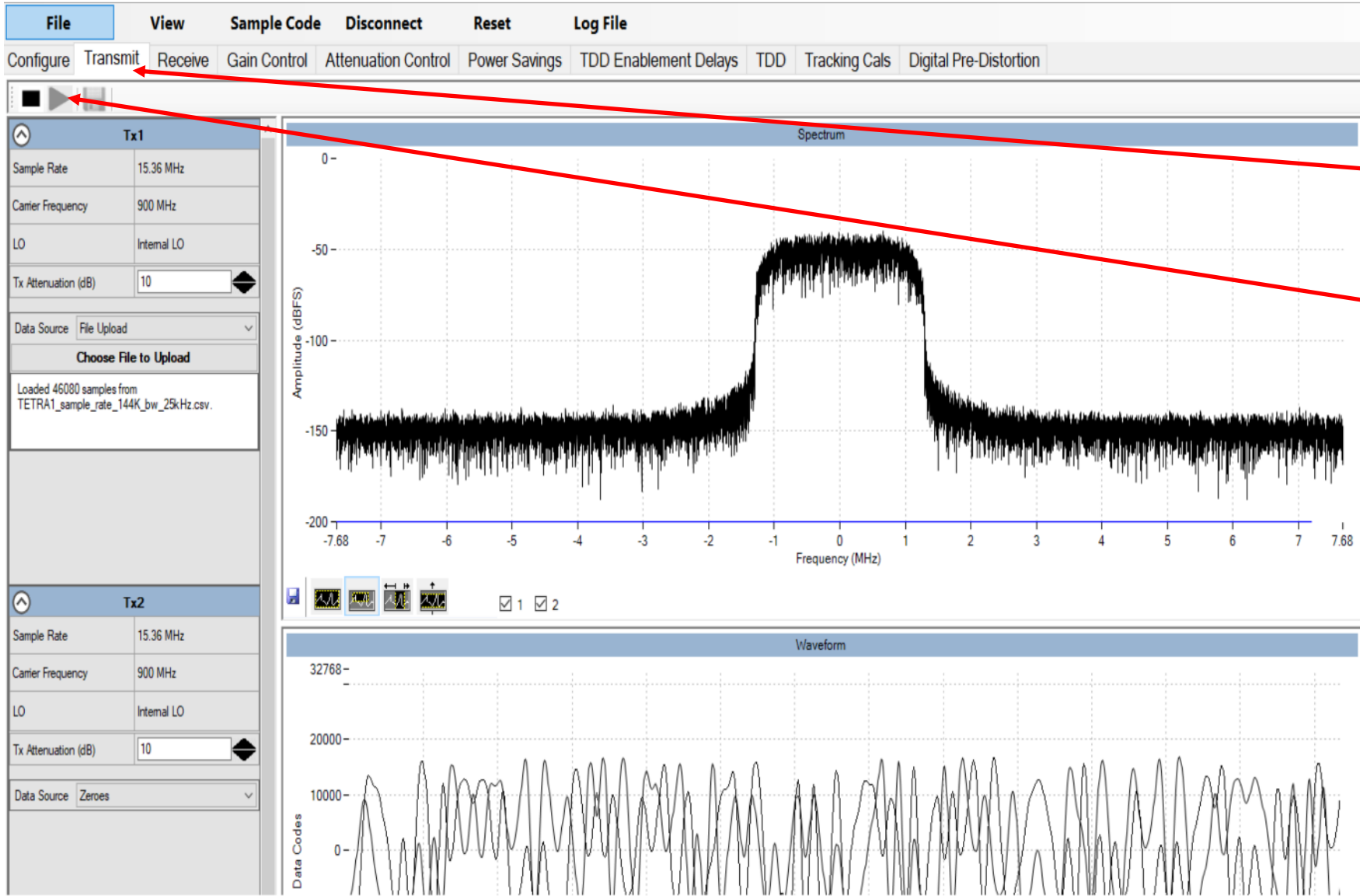
Internal LO2 (Off)

PLL2 Power Consumption Low Power

LO2 Optimization Best Power Consump

PLL2 Calibration Normal

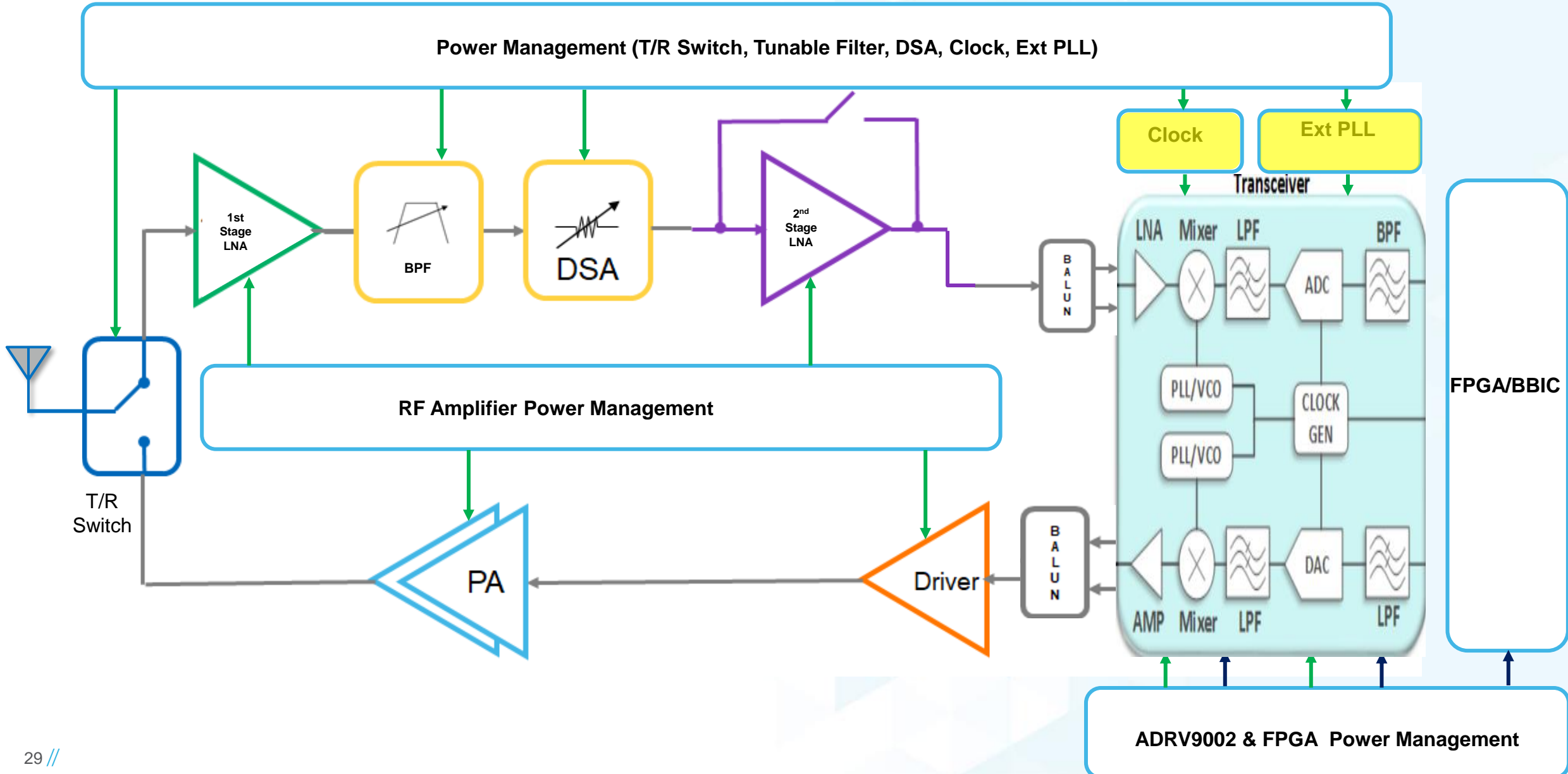
DPD Software Control with TES (cont.)



Select Transmit Tab

Press "Play" button

Clocking and External LO Generation



Clock and LO Generation

- ▶ ADRV9002's 3 different clock configurations

Mode	F_{REF}/F_{LO}	Recommend Clock and LO Sources
Internal LO without MCS	10 MHz to 1000 MHz (F_{REF})	CVCSO-914 (Crystek) CVCO55C (Crystek)
Internal LO with MCS	10 MHz to 1000 MHz (F_{REF})	LTC6952 JESD204B Clock IC w Crystek Osc HMC7044 JESD204B Clock IC w Crystek Osc
External LO without MCS	60 MHz to 12 GHz (F_{LO})	ADF4355-3 ADF4372 ADF4368

Multichip Synchronization

Overview

- ▶ Send 6 MCS pulses aligned to Reference Input
 - ADRV9002 specification > 2 reference clock cycles
 - Clock IC SYSREF min pulse width specification will often result in >> 2 reference clock cycles
- ▶ Leverage Existing JESD204B Clock ICs Single Pulse SYSREF Mode
- ▶ HMC7044/43 or LTC6952/53 Clock ICs
 - PLLs support External VCO/VCSO (LTC6952 or HMC7044)
 - Single Pulse SYSREF MODE
 - Multichip modes for arrays greater than 4 ADRV9002's

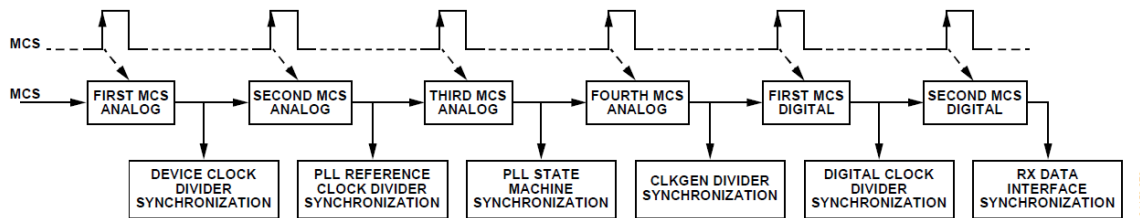
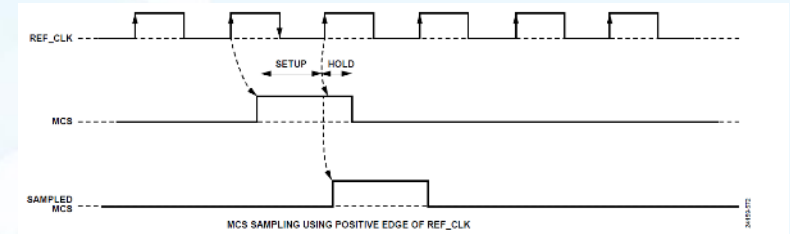
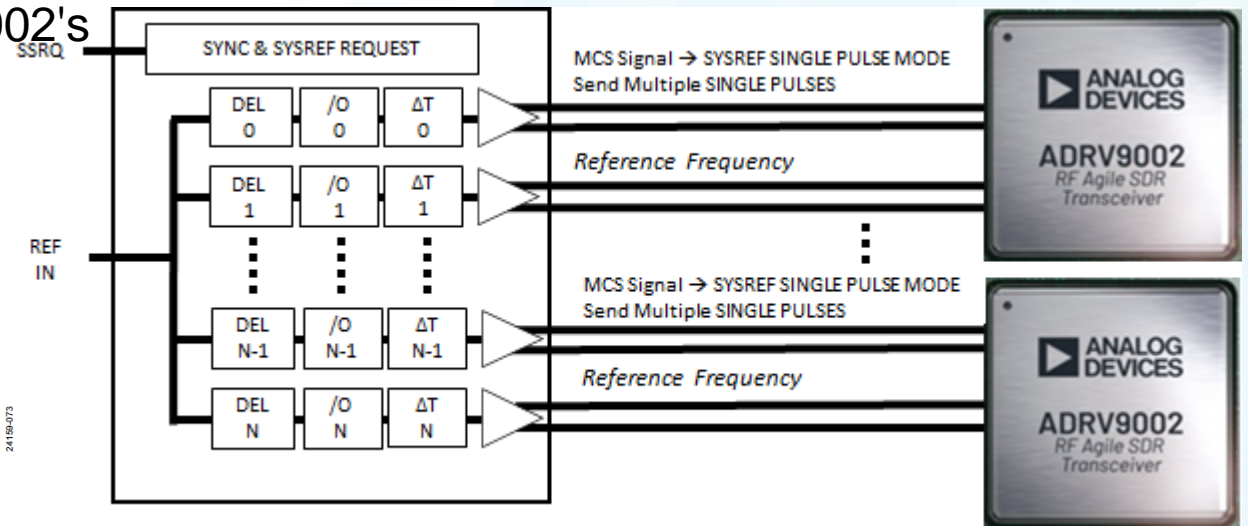
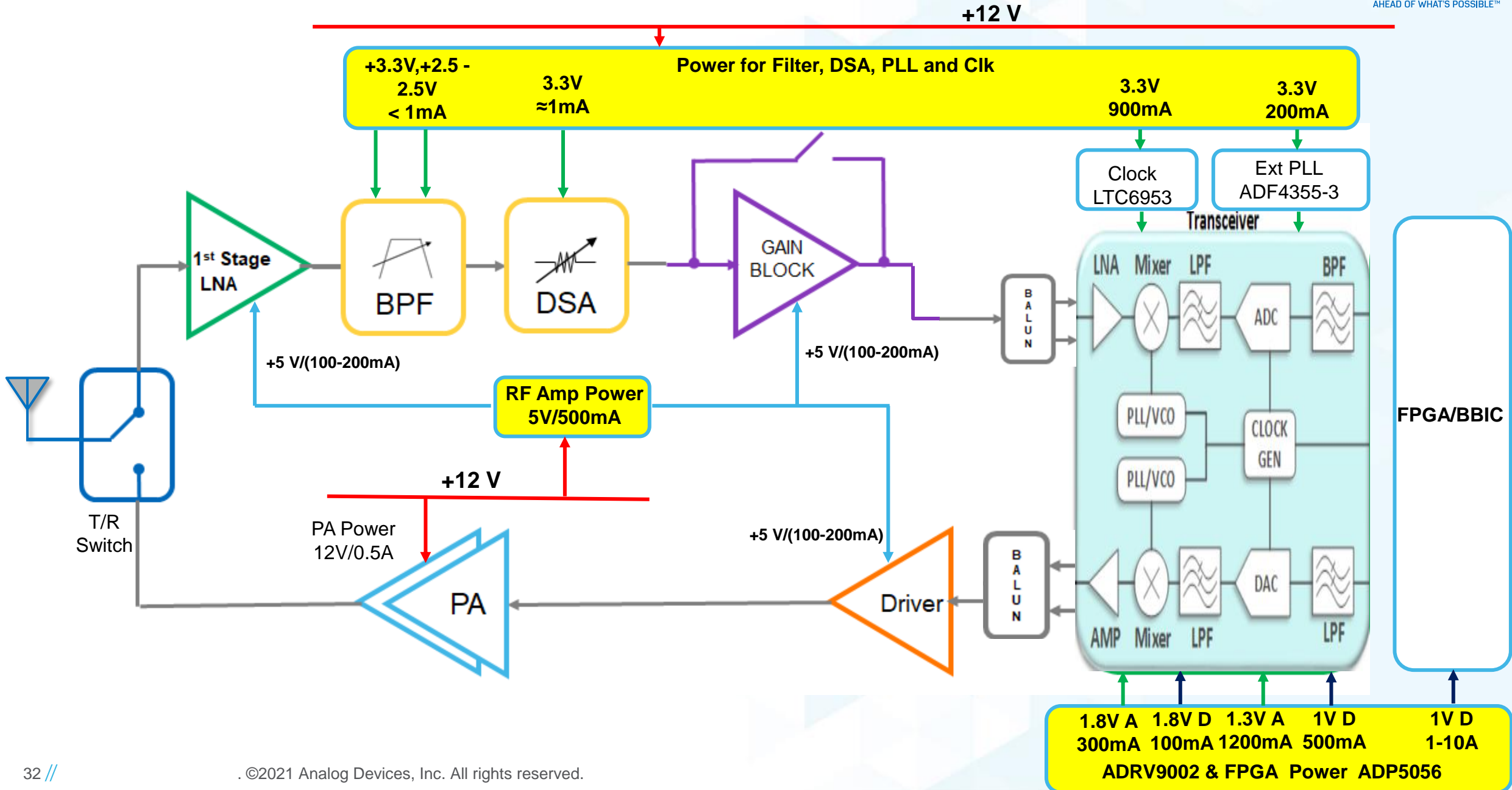


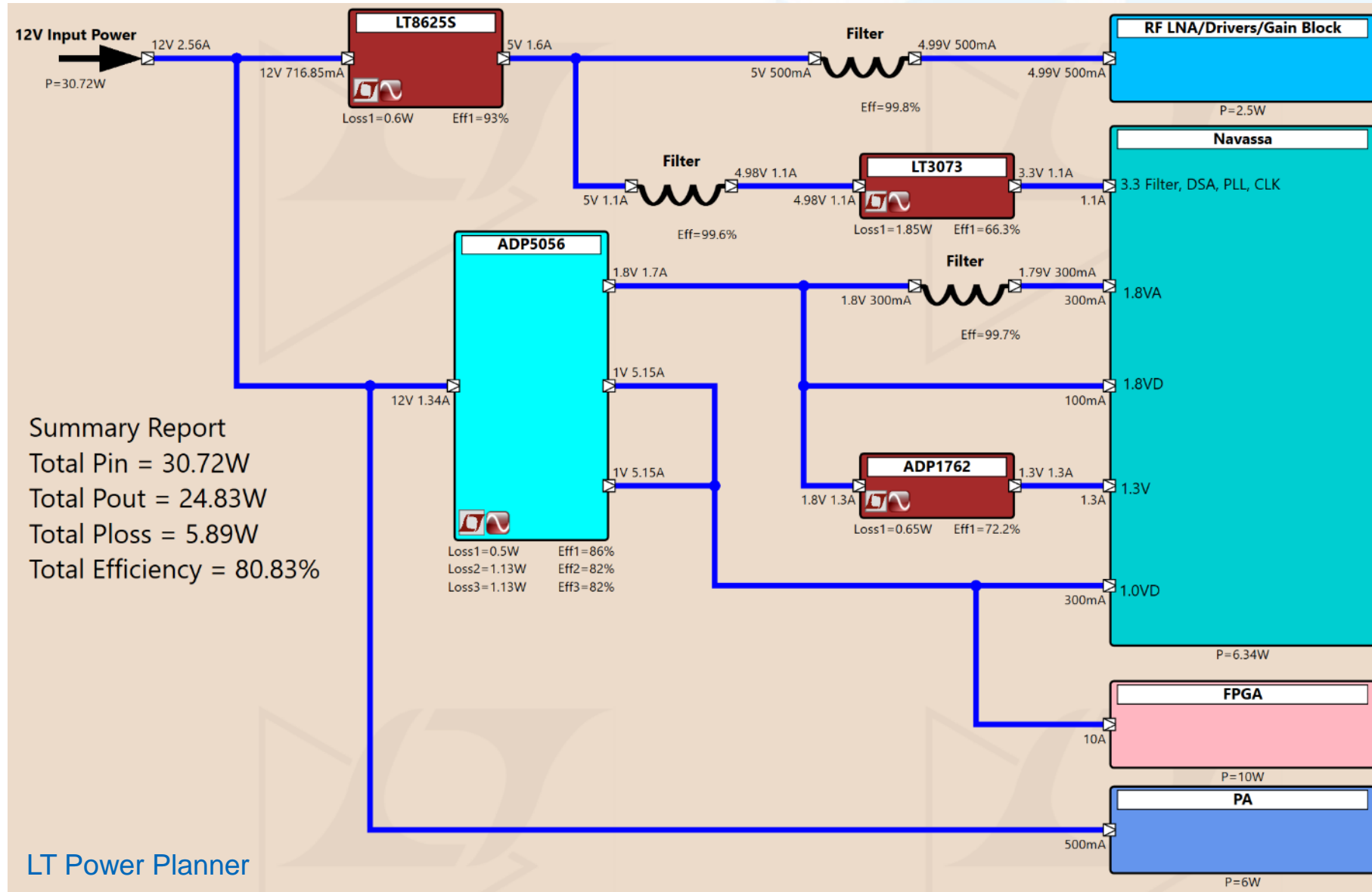
Figure 73 MCS pulses for analog and digital synchronization



Power Management

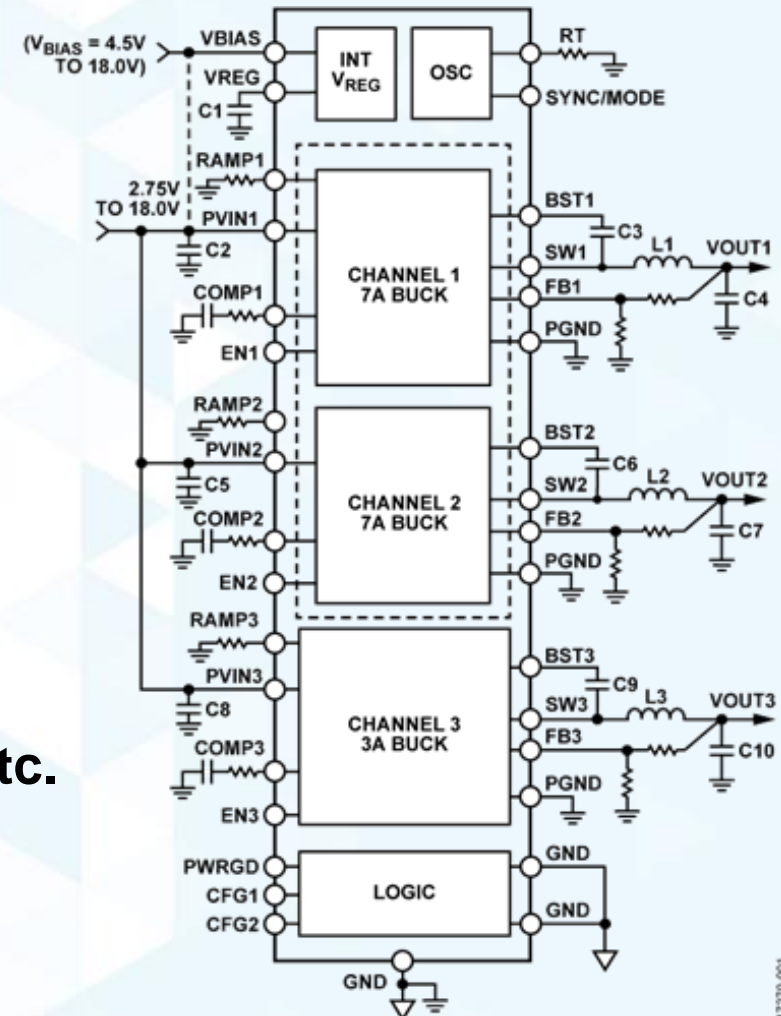


ADRV9002 RF Front End Power Solution



FEATURES

- Wide input voltage range: 2.75 V to 18 V
- Bias input voltage range: 4.5 V to 18 V
- Operation up to 150°C junction temperature
- $\pm 1\%$ Feedback voltage accuracy over temperature
- Ch1 and Ch2: 7A each, 14A in parallel operation
- Ch3: 3A
- 250 kHz to 2500 kHz adjustable switching frequency
- Simple 2 pin Rset configuration settings, seq, Ch setup, etc.



RF Amplifier Power Management

Ultra Low Noise Regulators

P/N	Description	Input Voltage	Vout Max	Output Current	Noise
LT8625S	18V/8A Step-Down Silent Switcher 3 with Ultralow Noise	2.7 V to 18 V	6V	8 A	4 μ VRMS

Active Bias Controllers

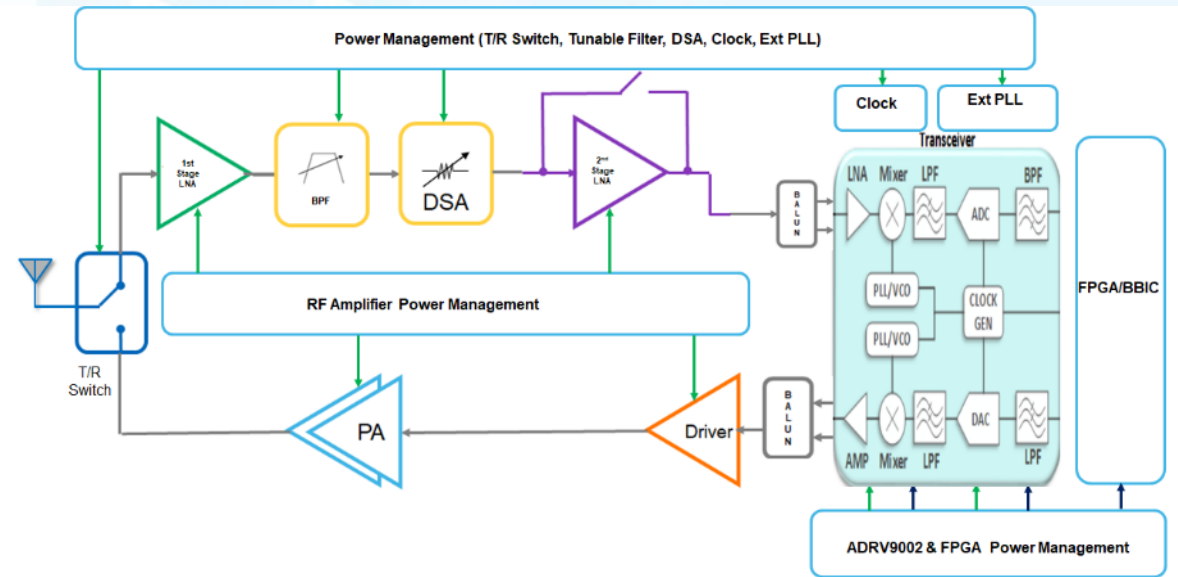
P/N	Output Drain Voltage	Max Drain Current	Gate Voltage
HMC980	5 V to 16.5 V	1600 mA	-2.46 V to +2.04V
HMC981	4 V to 12 V	200 mA	-2.5 V to +2.0 V
HMC920	3 V to 15 V	500 mA	-2.5 V to +2.0 V

Power Management (T/R Switch, Tunable Filter, DSA, Clock, Ext PLL)

P/N	Description	Input Voltage	Vout Max	Output Current	Noise
LT3042	Ultralow Noise RF Linear Regulator	1.8 V to 20 V	15 V	200 mA	0.8 μ VRMS
LT3045	Ultralow Noise RF Linear Regulator	1.8 V to 20 V	15 V	500 mA	0.8 μ VRMS

Summary and Wrap Up

- ▶ ADRV9001 SDR family offer 30 MHz to 6GHz RF range with configurable bandwidth from 12 KHz to 40 MHz in a 12mm x 12mm package
- ▶ ADI provides all the necessary front-end RF circuitry and power management to build a complete radio
- ▶ Built-In Observation Receiver and DPD algorithm can be used to improved ACLR by up to 18 dB
- ▶ Multiple Hardware and Software Resources Available



Resources

▶ Evaluation Boards

▶ ADRV9002 Transceiver Evaluation Software

- [Wideband RF Transceiver Evaluation Software | Analog Devices](#)

▶ Milcom Solutions on analog.com

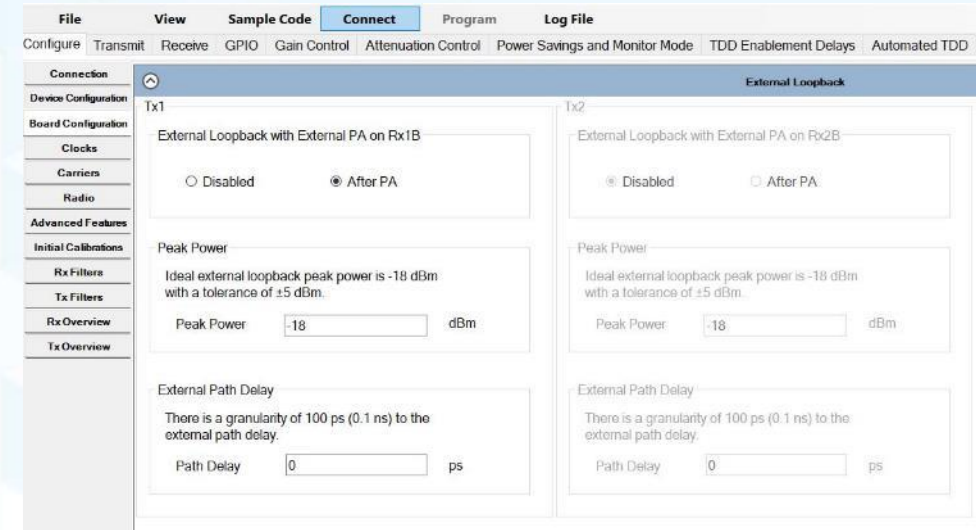
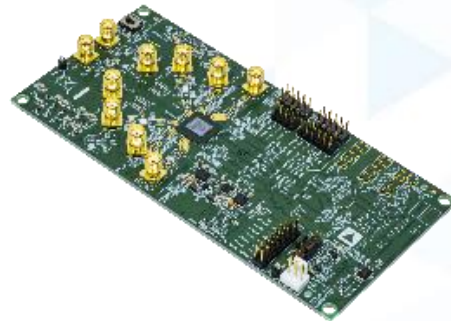
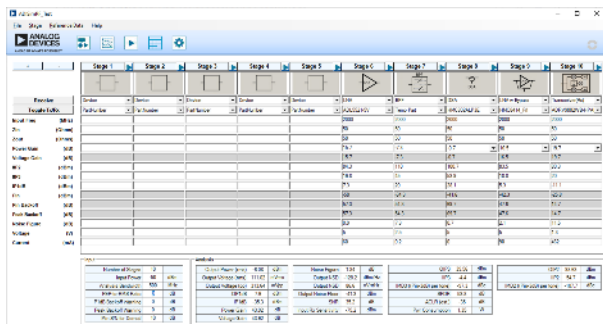
- [Military Communications | Analog Devices](#)

▶ LT Power CAD/LT Power Planner

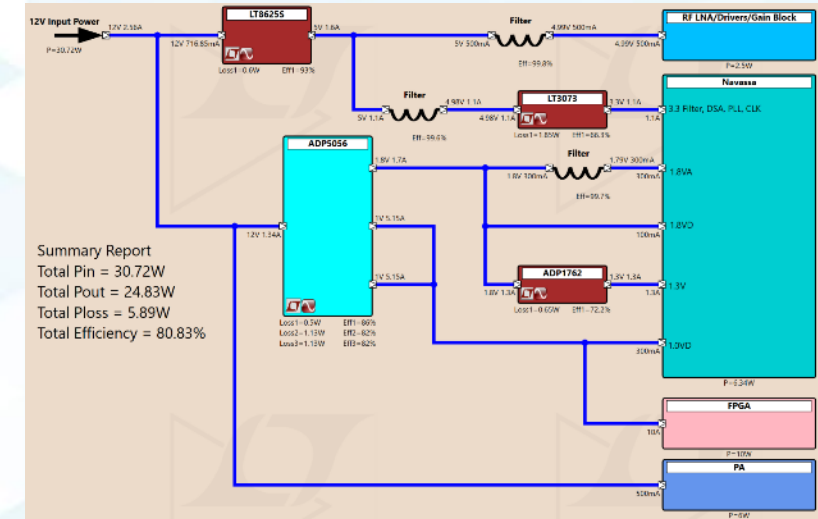
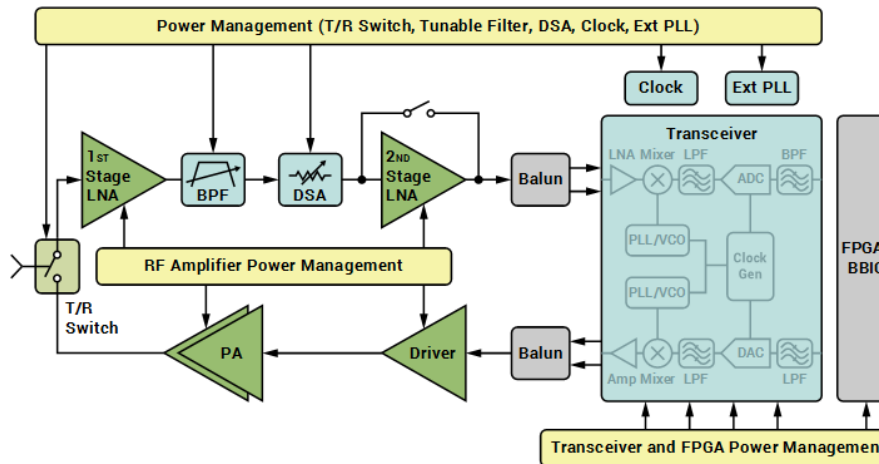
- [LTpowerCAD | Analog Devices](#)

▶ ADIsimRF

- [ADIsimRF | Analog Devices](#)

Block	Power In (W)	Power Out (W)	Loss (W)	Efficiency (%)
1st Stage LNA	0.000	0.000	0.000	0.000
BPF	0.000	0.000	0.000	0.000
DSA	0.000	0.000	0.000	0.000
2nd Stage LNA	0.000	0.000	0.000	0.000
Balun	0.000	0.000	0.000	0.000
Transceiver	0.000	0.000	0.000	0.000
FPGA/BBIC	0.000	0.000	0.000	0.000
PA	0.000	0.000	0.000	0.000
Driver	0.000	0.000	0.000	0.000
T/R Switch	0.000	0.000	0.000	0.000



Q & A



AHEAD OF WHAT'S POSSIBLE™

RF Front-End Design for the ADRV9002 Narrow/Wideband Transceiver

Oisin Watkins, Eamon Nash, Larry Prestia