또 하나의 SoC (System on chip)

System on MAX X

Webinar / 2014

MEASURABLE ADVANTAGE™

Agenda

- **Overview**
- **Architectural Details**
  - Core Fabric
    - Core Architecture
    - DSP
    - PLL
    - Clocking
    - Internal Memory
  - Power
    - Voltage Regulator
    - Power Savings
  - I/O
    - General Purpose I/O
    - LVDS
    - External Memory Interface (EMIF)
  - Internal Oscillator
  - User Flash Memory
  - Configuration
    - Instant-On
    - Design Security
    - SEU Mitigation
  - Analog Block
  - Design S/W and IP
- **Development tools**

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MAX 10 FPGAs – Overview

MEASURABLE ADVANTAGE™

Innovation Leader Across the Board

ALTERA®

MAX® Series	Cyclone® Series	Arria® Series	Stratix® Series	ENPIRION
PLDs Lowest Cost, Lowest Power	**FPGAs** Cost/Power Balance SoC & Transceivers	**FPGAs** Mid-range FPGAs SoC & Transceivers	**FPGAs** Optimized for High Bandwidth	**PowerSoCs** High-efficiency Power Management

RESOURCES

Embedded Soft and Hard Processors

Nios® II

ARM®

Design Software

QUARTUS® II

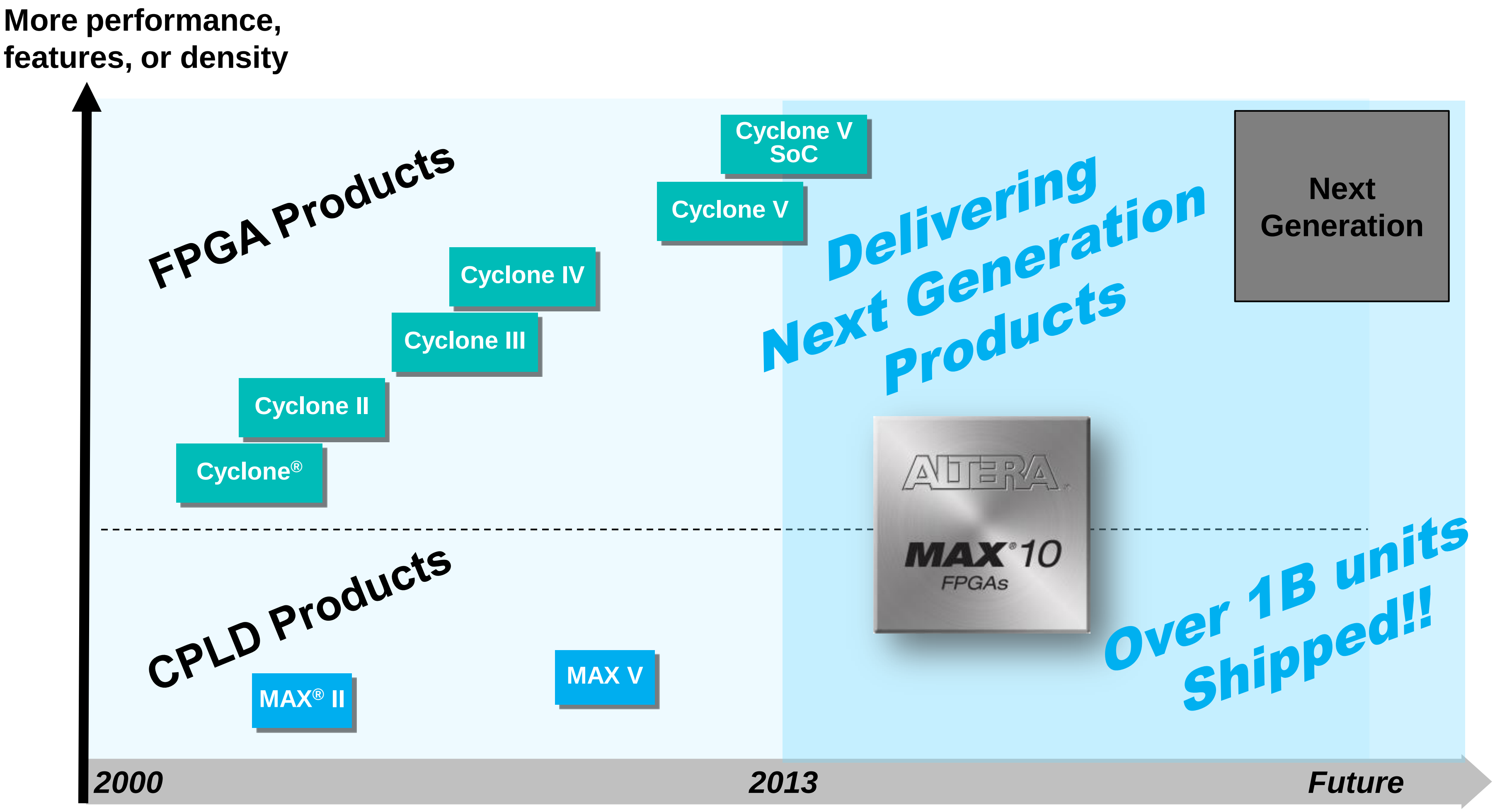
DSP Builder

Development Kits

Intellectual Property (IP)

- Industrial
- Computing
- Enterprise

Low Cost Families – Altera Continues Focus & Investment



More performance, features, or density

FPGA Products

Cyclone®

Cyclone II

Cyclone III

Cyclone IV

Cyclone V

Cyclone V SoC

Delivering Next Generation Products

Next Generation

CPLD Products

MAX® II

MAX V

ALTERA MAX® 10 FPGAs

Over 1B units Shipped!!

2000

2013

Future

■ In Design

▨ Product Planning

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MAX 10 FPGAs: Revolutionizing Non-Volatile Integration

- **FPGA Capabilities**
  - Up to 50,000 Logic Elements
  - Analog Block with ADC
  - Internal SRAM
  - PLLs
  - DSP Blocks
  - External Memory Interface (e.g. DDR3)
  - Dual Image Configuration
  - Nios II Embedded Soft Processor
  - LVDS, PCI, and 30+ other I/O Standards
  - Design Security
  - Sleep Mode
- **Non-volatile Features**
  - Instant-On
  - User Flash Memory
  - Voltage Regulator
  - Internal Oscillator

MAX 10 FPGA Customer Benefits

Lowers System Cost

Increase Board Reliability

Single-chip integration item	Customer Benefits
N-components → 1 component	Higher system reliability (less failure points)
	Reduced BOM/System Cost
Reduced PCB Footprint	Simpler PCB Design
	Fewer PCB layers → Lower PCB cost
Fewer Suppliers	Less vendors to manage
PLD have Longer Life-cycles	Avoids EOL vs. other technologies

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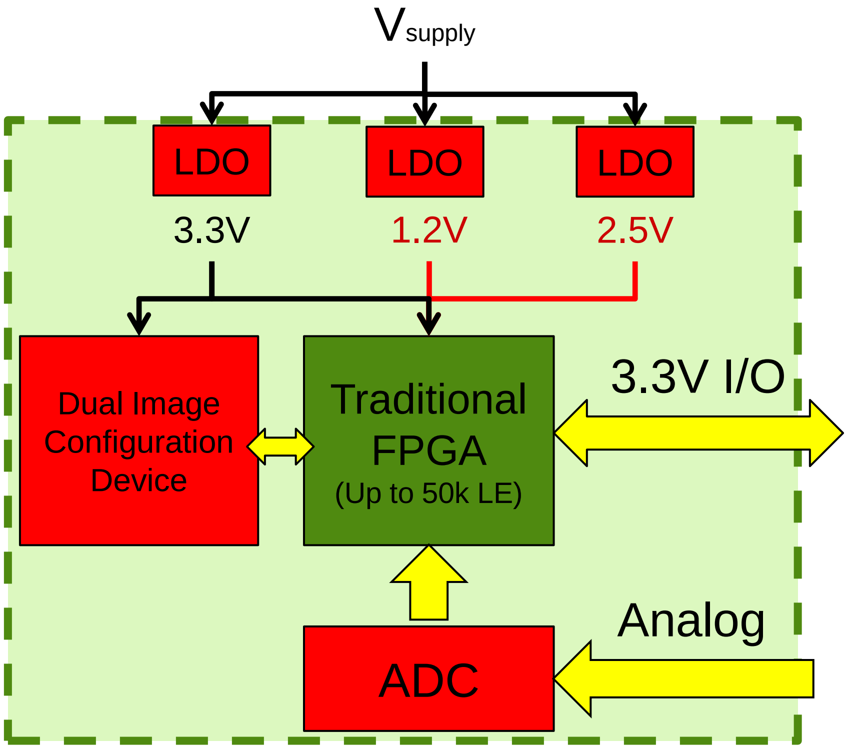
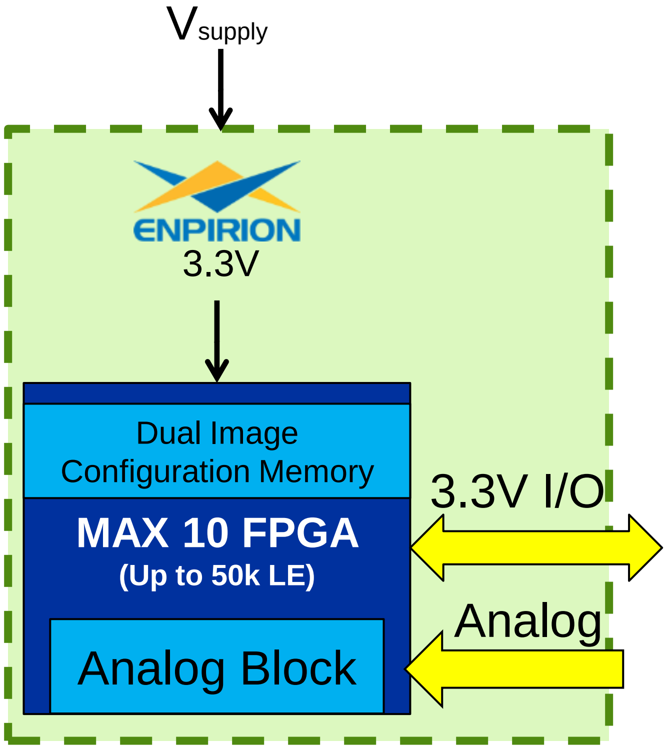
MAX 10 FPGAs Simplify FPGA Systems

Traditional FPGA



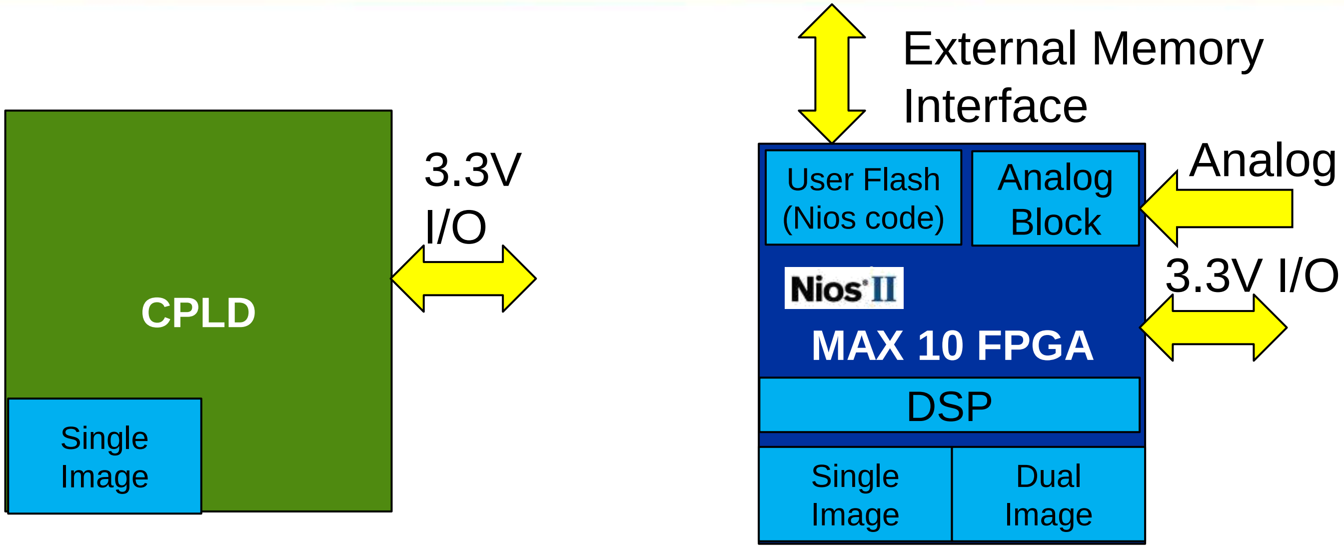
Standard Configuration Time

MAX 10 FPGAs



Instant-On Configuration

MAX 10 FPGAs Increase Capabilities of CPLD Systems



	CPLD	MAX 10 FPGAs
Logic Elements	240 – 8,000	2,000 to 50,000
Instant-On Images	Single	Dual
DSP	No	Yes
DDR3 SDRAM	No	Yes
Analog Block w/ADC	No	Yes
Embedded Soft Processor	No	Nios® II

MAX 10 Target Applications

Industrial Drives, Motor Control, I/O Modules

- Sense environmental conditions
  - Analog, temperature, motor, etc.
- Efficient real-time calculations
- Video and motion control processing

Communications, Compute & Storage

- Manage board bring-up
- Power sequencing
- I/O Expansion

Automotive Infotainment, ADAS, E-vehicle

- Instant-on configuration meets regulatory requirements
- High-quality video and image processing
- Small form factor through single-chip integration

… & many more applications

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MAX 10 – Higher Single Chip Integration

Feature	MAX V CPLDs	MAX 10 FPGAs
Process Technology	180 nm	55 nm
User Logic (max.)	2,000 LE’s	50,000 LE’s
On-chip Configuration	Single Image	Dual Image, AES
User I/O	271	Up to 500
User Flash Memory	8 Kb	Up to 512 Kb
On-chip hard IP blocks	-	Embedded RAM, DSP, ADC, PLL
Remote System Upgrade	No	Yes

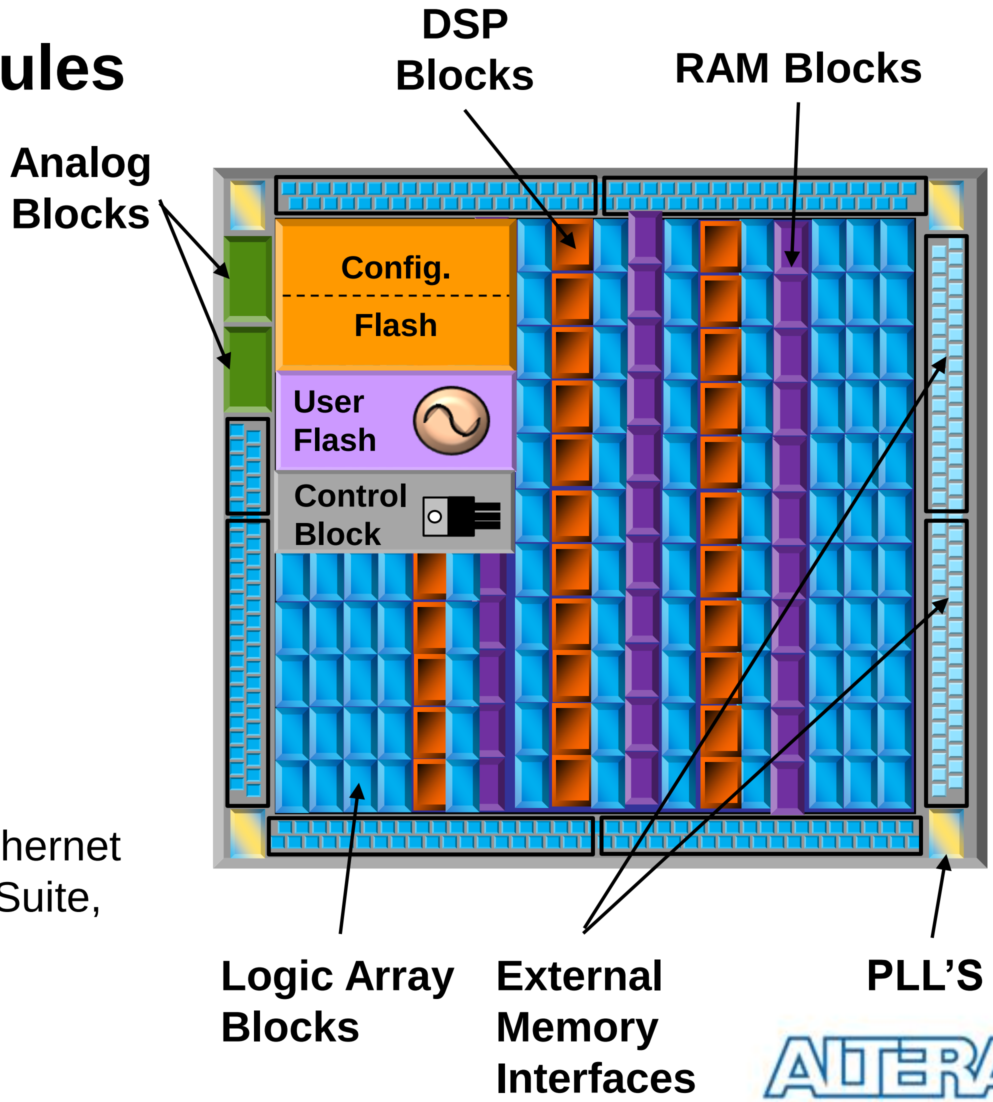
Lowering System Cost

&

Increasing Reliability

MAX 10 FPGA – Floor plan

- **Main Architecture Modules**
  - Logic array
  - On-chip RAM & FLASH
  - DSP blocks
  - Up to two analog blocks
  - Up to eight I/O banks
  - Up to four PLL's
  - Oscillator & Clocks
  - Soft IP functionality
    - Nios® II 32-bit processor, Ethernet MAC, PCIe MAC, Video IP Suite, etc.



MAX 10 FPGA – Family Plan

Device	LEs	Block Memory (Kb)	User Flash [1] (Kb)	18x18 Mults	PLLs	Internal Config.	ADC, TSD	External RAM I/F
10M02	2,000	108	96	16	1, 2	Single	-	Yes [2]
10M04	4,000	189	128	19	1, 2	Dual	1, 1	Yes [2]
10M08	8,000	378	256	24	1, 2	Dual	1, 1	Yes [2]
10M16	16,000	549	256	45	1, 4	Dual	1, 1	Yes [3]
10M25	25,000	756	256	61	1, 4	Dual	2, 1	Yes [3]
10M40	40,000	1,260	512	125	1, 4	Dual	2, 1	Yes [3]
10M50	50,000	1,638	512	144	1, 4	Dual	2, 1	Yes [3]

Notes:
1. ***Additional User Flash may be available, depending on configuration options.***
2. ***SRAM only.***
3. ***SDR SDRAM, SRAM, DDR3, DDR2, or LPDDR2.***
4. ***ADC blocks available on die but may not be available in low pin count packages.***

Preliminary and subject to change without notice.

MAX 10 FPGA – Feature Set Options

Feature Set	C: Compact	F: Flash	A: Analog
Single Image	Yes	Yes	Yes
Dual Image w/Remote System Upgrade	-	Yes	Yes
Analog Features Block	-	-	Yes
	“C”	**“F”**	**“A”**

Three Feature Set Variants

To Order From

Package Plan & Available I/O (all devices)

	Dual Power Supply: 1.2V/2.5V						Single Power Supply: 3.3V		
Device	36-WLCSP 3 x 3 mm^2 0.4 mm	81-WLCSP 4 x 4 mm^2 0.4 mm	256-FBGA 17 x 17 mm^2 1.0 mm	324-UBGA 15 x 15 mm^2 0.8 mm	484-FBGA 23 x 23 mm^2 1.0 mm	672-FBGA 27 x 27 mm^2 1.0 mm	144-EQFP 22 x 22 mm^2 0.5 mm	153-MBGA 8 x 8 mm^2 0.5 mm [1]	169-UBGA 11 x 11 mm^2 0.8 mm
10M02	C (27)	-	-	C (160)	-	-	C (101)	C (112)	C (130)
10M04	-	-	C/F/A (178)	C/F/A (246)	-	-	C/F/A (101)	C/F/A (112)	C/F/A (130)
10M08	-	C/F (56)	C/F/A (178)	C/F/A (246)	C/F/A (250)	-	C/F/A (101)	C/F/A (112)	C/F/A (130)
10M16	-	-	C/F/A (178)	C/F/A (246)	C/F/A (320)	-	C/F/A (101)	-	C/F/A (130)
10M25	-	-	C/F/A (178)	-	C/F/A (360)	C/F/A (380)	C/F/A (101)	-	-
10M40	-	-	C/F/A (178)	-	C/F/A (360)	C/F/A (500)	C/F/A (101)	-	-
10M50	-	-	C/F/A (178)	-	C/F/A (360)	C/F/A (500)	C/F/A (101)	-	-

Notes:

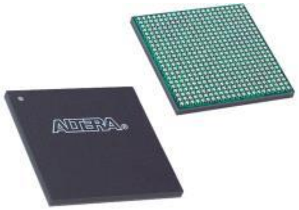
1 - "Easy PCB" utilizes 0.8mm PCB design rules

2 - A subset of p/n's will be available in Automotive grade.

Preliminary and subject to change without notice.

Bare Die

WLCSP



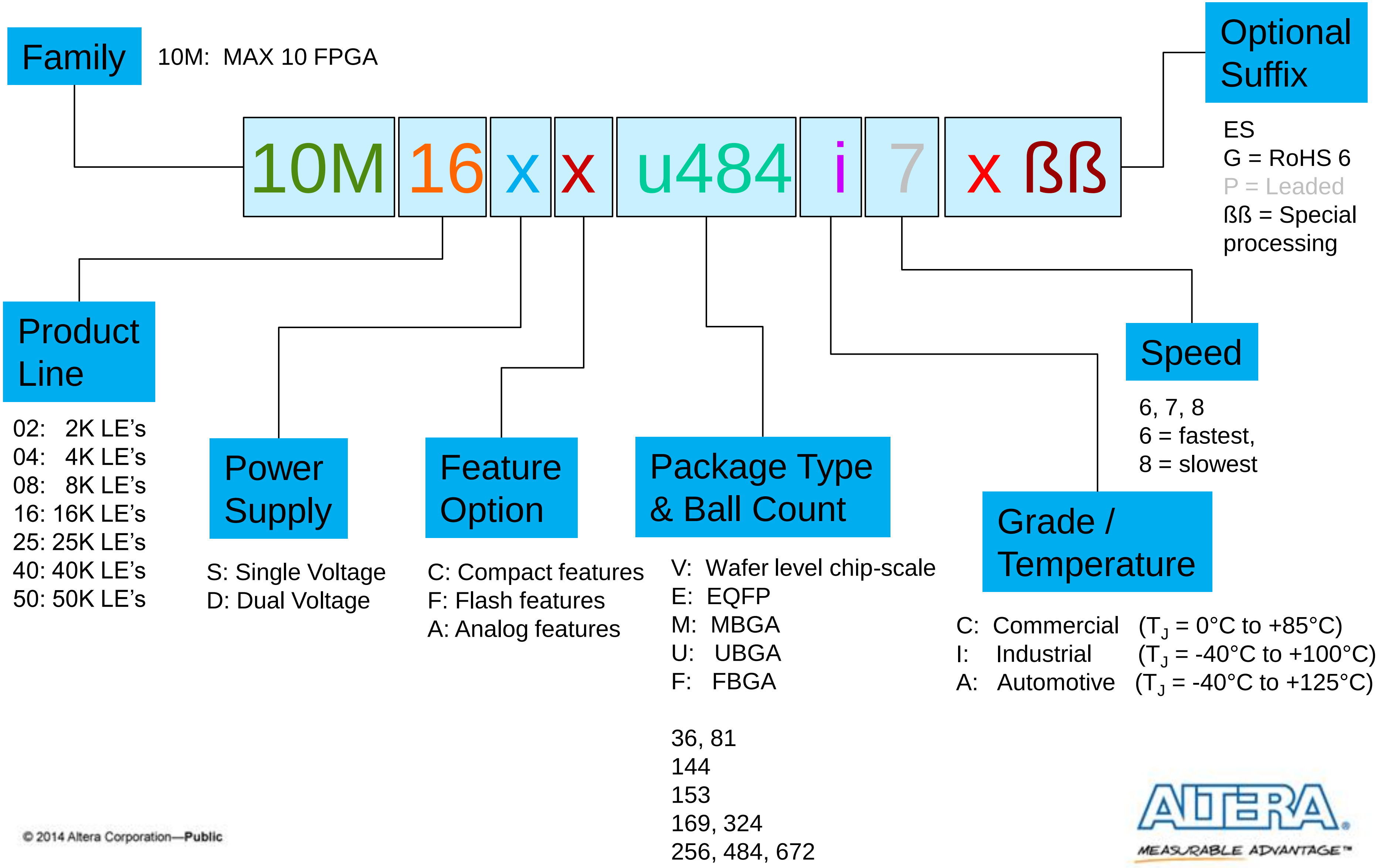
xBGA

M = 0.5mm ball spacing
U = 0.8mm ball spacing
F = 1.0mm ball spacing

EQFP

C: Compact features
F: Flash features
A: Analog features

MAX 10 FPGA - Ordering Information



10M 16 x x u484 i 7 x ßß

Family

10M: MAX 10 FPGA

Product Line

02: 2K LE’s
04: 4K LE’s
08: 8K LE’s
16: 16K LE’s
25: 25K LE’s
40: 40K LE’s
50: 50K LE’s

Power Supply

S: Single Voltage
D: Dual Voltage

Feature Option

C: Compact features
F: Flash features
A: Analog features

Package Type & Ball Count

V: Wafer level chip-scale
E: EQFP
M: MBGA
U: UBGA
F: FBGA

36, 81
144
153
169, 324
256, 484, 672

Grade / Temperature

C: Commercial (T_J = 0°C to +85°C)
I: Industrial (T_J = -40°C to +100°C)
A: Automotive (T_J = -40°C to +125°C)

Speed

6, 7, 8
6 = fastest,
8 = slowest

Optional Suffix

ES
G = RoHS 6
P = Leaded
ßß = Special processing

MAX 10 FPGA I/O Standard Support

I/O Standard	Variant	Toggle Rate (MHz)	Max Strength	Load	Application
Single-Ended	LVTTL/LVCMOS 3.3V	250	2 mA	10 pF	General purpose
	LVTTL/LVCMOS 3.0V	250	16 mA	10 pF	General purpose
	LVTTL/LVCMOS 2.5V	250	16 mA	10 pF	General purpose
	LVTTL/LVCMOS 1.8V	250	12 mA	10 pF	General purpose
	LVTTL/LVCMOS 1.5V	250	8 mA	10 pF	General purpose
	LVTTL/LVCMOS 1.2V	200	8 mA	10 pF	General purpose
	PCI	250	-	10 pF	General purpose
	Schmitt Trigger (RX only)	200	-	-	General purpose
External Memory Interfaces **(& Voltage Referenced I/O)**	SSTL2 Class I	250	12 mA/50 Ω	7 pF	DDR1
	SSTL2 Class II	250	16 mA/25 Ω	7 pF	DDR1
	SSTL18 Class I	300	12 mA/50 Ω	7 pF	DDR2
	SSTL18 Class II	300	16 mA/25 Ω	7 pF	DDR2
	SSTL15 Class I	300	12 mA/50 Ω	7 pF	DDR3
	SSTL15 Class II	300	16 mA/25 Ω	7 pF	DDR3
	SSTL15	300	34 Ω	7 pF	DDR3
	SSTL135	300	34 Ω	7 pF	DDR3L
	HSUL12	200	34 Ω	7 pF	LPDDR2
	HSTL18 Class I	300	12 mA/50 Ω	7 pF	DDR2+/QDR2+/RLDRAM2
	HSTL18 Class II	300	16 mA/25 Ω	7 pF	DDR2+/QDR2+/RLDRAM2
	HSTL15 Class I	300	12 mA/50 Ω	7 pF	DDR2+/QDR2/QDR2+/RLDRAM2
	HSTL15 Class II	300	16 mA/25 Ω	7 pF	DDR2+/QDR2/QDR2+/RLDRAM2
	HSTL12 Cass I	200	12 mA/50 Ω	7 pF	General purpose
	HSTL12 Class II	200	14 mA/25 Ω	7 pF	General purpose
LVDS	Dedicated LVDS (RX/TX)	830/800 Mbps	-	6 pF	
	Dedicated Mini-LVDS (TX)	380 Mbps	-	6 pF	
	Dedicated RSDS (TX)	340 Mbps	-	6 pF	
	Dedicated PPDS (TX)	420 Mbps	-	6 pF	
	External Resistor LVDS (TX)	600 Mbps	-	6 pF	
	External Resistor Mini-LVDS (TX)	380 Mbps	-	6 pF	
	External Resistor RSDS (1R) (TX)	170 Mbps	-	6 pF	
	External Resistor RSDS (3R) (TX)	342 Mbps	-	6 pF	
	External Resistor PPDS (TX)	420 Mbps	-	6 pF	
	LVPECL (RX only)	830 Mbps		6 pF	
	BLVDS (RX/TX)	830/475 Mbps	16 mA	6 pF	

MAX 10 FPGAs – Architectural Details

MAX 10 FPGA – Architectural Sections

- **Core Fabric**
  - Core Architecture
  - DSP
  - PLL
  - Clocking
  - Internal Memory
- **Power**
  - Voltage Regulator
  - Power Savings
- **I/O**
  - General Purpose I/O
  - LVDS
  - External Memory Interface (EMIF)
- **Internal Oscillator**
- **User Flash Memory**
- **Configuration**
  - Instant-On
  - Design Security
  - SEU Mitigation
- **Analog Block**
- **Design S/W and IP**

MAX10 FPGA – Core Architecture

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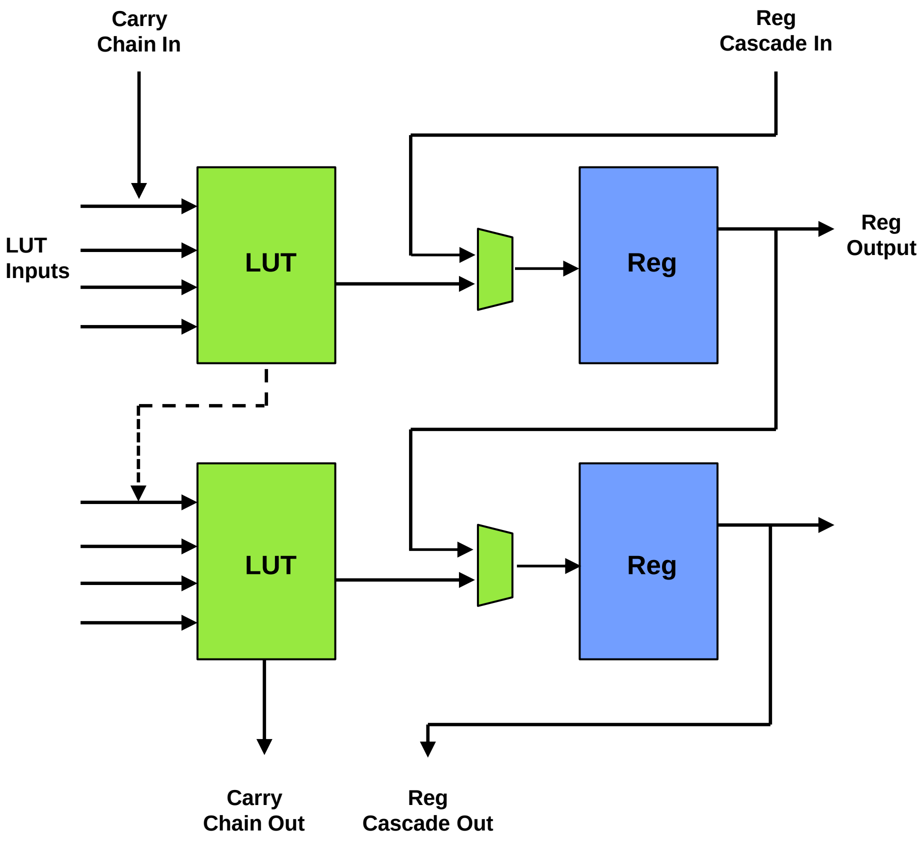
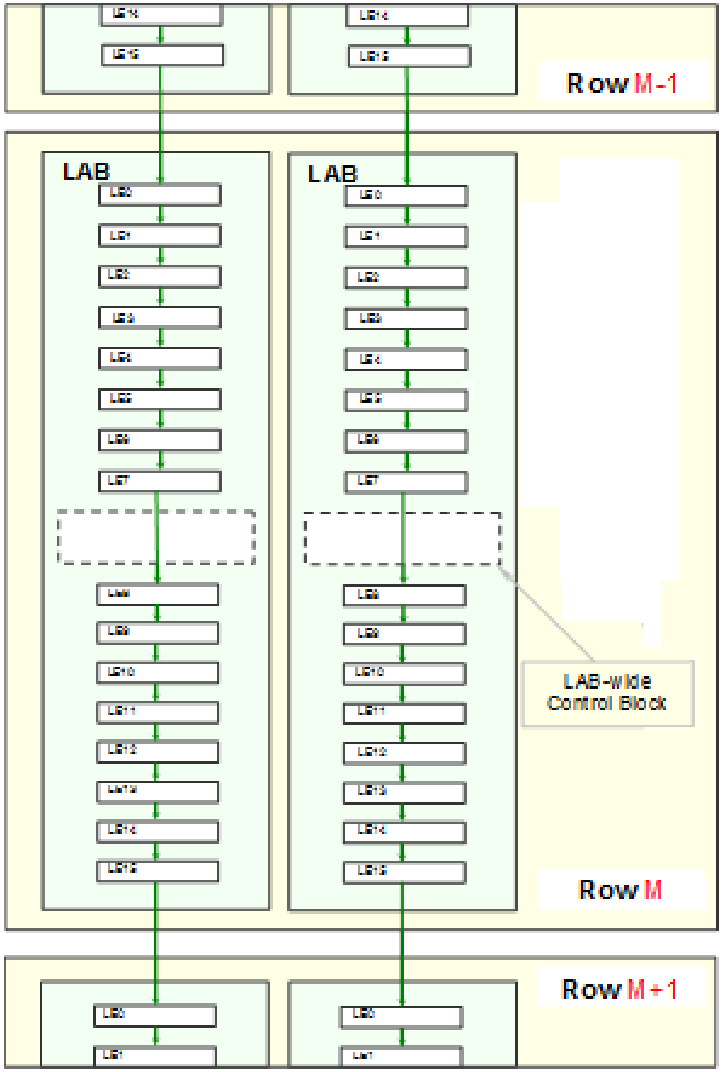
MAX 10 FPGA – Logic Element (LE) and Interconnect

- **LE = 4-input Look Up Table (LUT) + Register**

- **Two dedicated paths between LEs:**
  - Carry chain
    - Chain runs the entire length of a LAB Block Column
  - Register cascade
    - Cascade chain can start & finish at any LE
    - Multiple chains supported
    - Register cascade between LAB blocks is not supported



MAX 10 FPGA – Logic Array Block (LAB) Structure

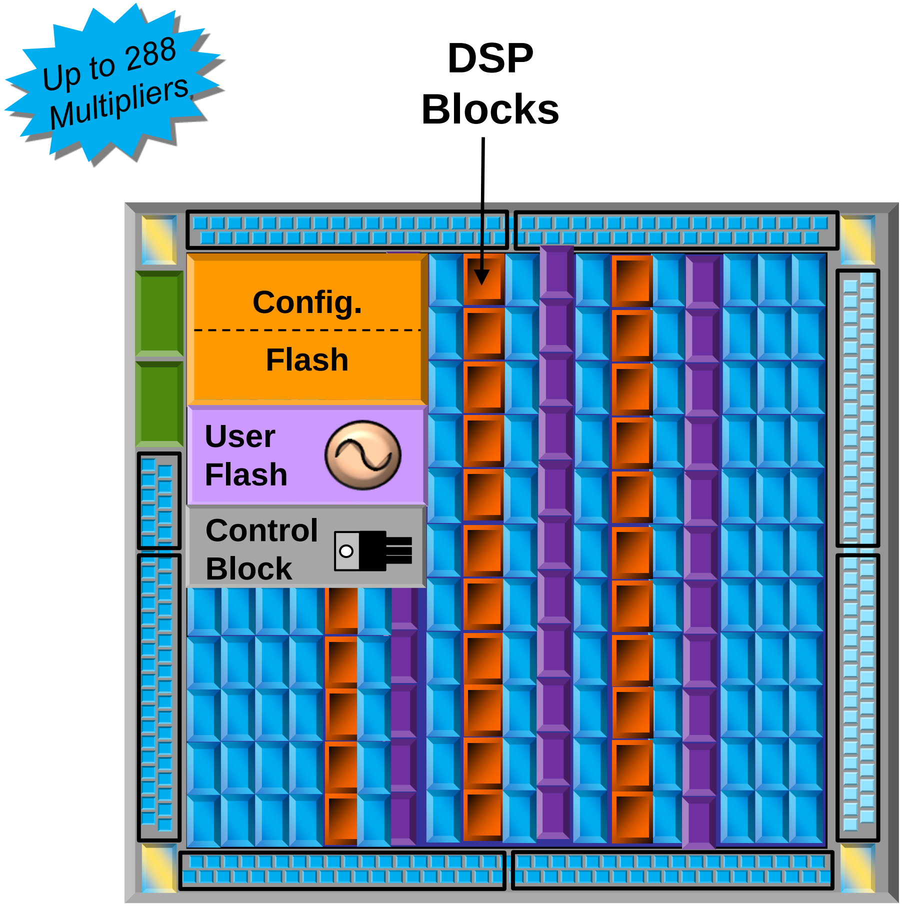


- **Logic Element**
  - Look Up Table + Register + Output Logic
- **Logic Array Block**
  - 16 Logic Elements
  - Control Block (middle of LAB)
  - Lab-wide routing (not shown)

☞ *Click to return to Architectural Sections*

MAX10 FPGA – DSP

MAX 10 FPGAs – Basic DSP Architecture

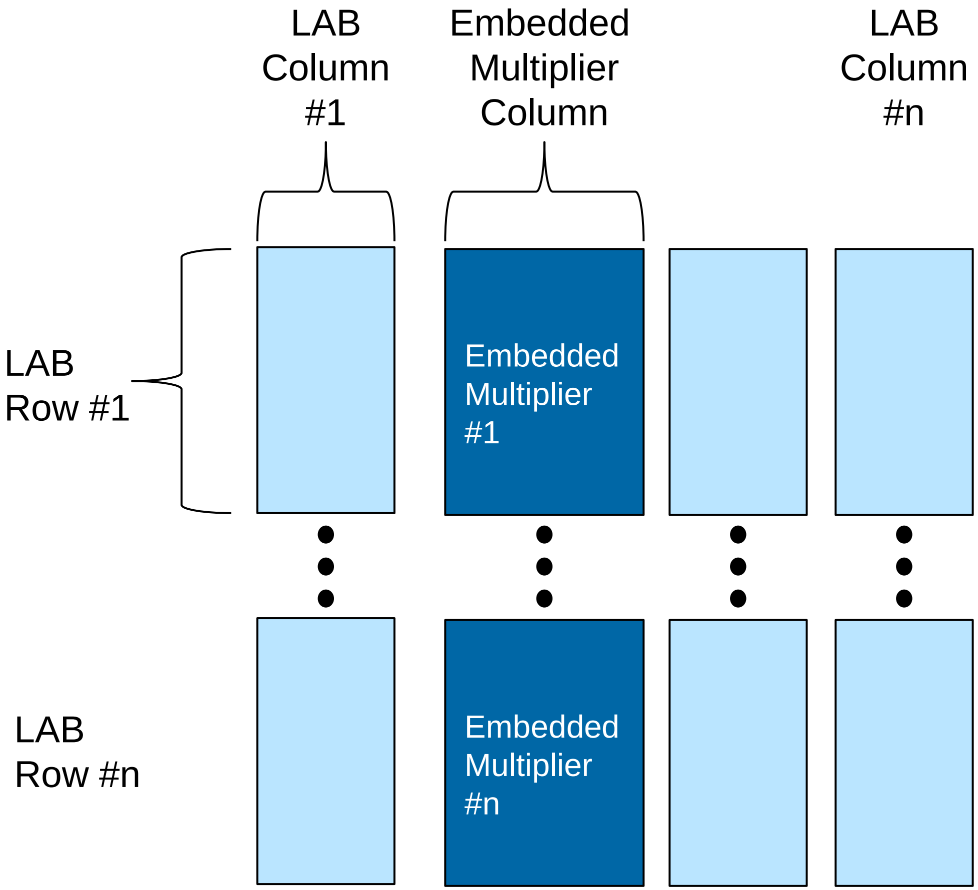


- Only non-volatile, low-cost FPGA with dedicated hard multipliers

- Supports Up To:
  - 144 18x18 multipliers or,
  - 288 9x9 multipliers

- Maximum multiplier performance of 234 MHz

MAX 10 FPGAs – DSP Block Organization



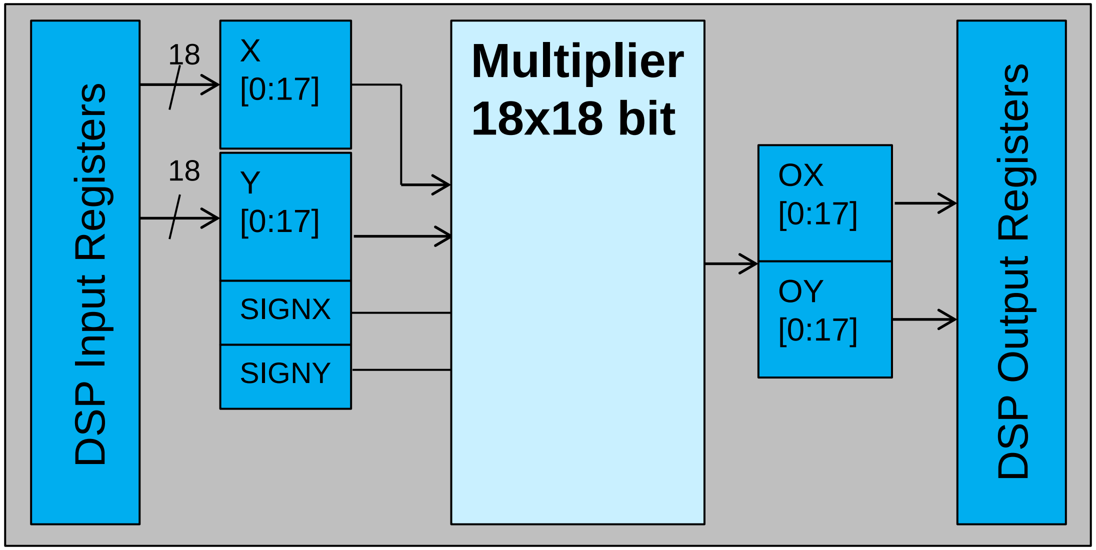
- **Implemented as column elements in between LAB columns**
- **Multiplications greater than 18-bits are supported via cascade chaining of DSP blocks**
  - Supports wide multiplication
- **Automatically supported in Quartus® II software**

MAX 10 FPGAs – DSP Block Architecture

- **41 inputs (max.)**
  - 36 data inputs
  - 5 control signal inputs

- **36 outputs (max.)**

- **Two modes of operation:**



Modes	# Data Inputs	# Data Outputs
1 individual 18bx18b multiplier	36	36
2 individual 9bx9b multipliers	36	36

MAX 10 FPGAs – DSP Performance

MAX 10 FPGA Supply Variant	Speed Grade		
	-6	-7	-8
MAX 10D - Dual Supply	234 MHz	212 MHz	180 MHz
MAX 10S - Single Supply	198 MHz	183 MHz	160 MHz

Note: performance numbers per speed grade all assume registered inputs and outputs

☞ [Click to return to Architectural Sections]

MAX10 FPGA – Phase Locked Loops (PLLs)

MAX 10 FPGAs – Full Featured PLLs

- **Up to four full-featured PLLs**
  - Five programmable outputs per PLL
  - Dynamically change both frequency and phase
  - Up to 10 global clocks and 2 external clocks outputs from 1 clock source
- **Flexibility**
  - Support multiple or unknown input frequencies using dynamic reconfiguration
  - PLL counter cascading for finer clock synthesis resolution
  - Single PLL supply device option
- **External interface support**
  - x16 DDR3 interfaces using a single PLL
  - Support for LVDS interfaces up to 830 Mbps

☞ [*Click to return to Architectural Sections*]

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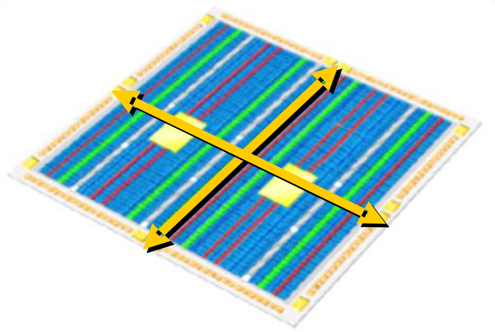
MAX10 FPGA – Clocks

MAX 10 FPGAs – Low Power Clocking Architecture

- **Low power…when needed**
  - Dynamic enable/disable for power control/sleep
  - Unused networks automatically powered down

- **High performance**
  - Up to 450MHz
- **Abundant, flexible clocking resources**
  - Up to 20 global clock networks with dynamic user clock selection
  - Oscillator for Self-running applications - sleep controller, watch-dogs, etc.



Up to 20 networks per device

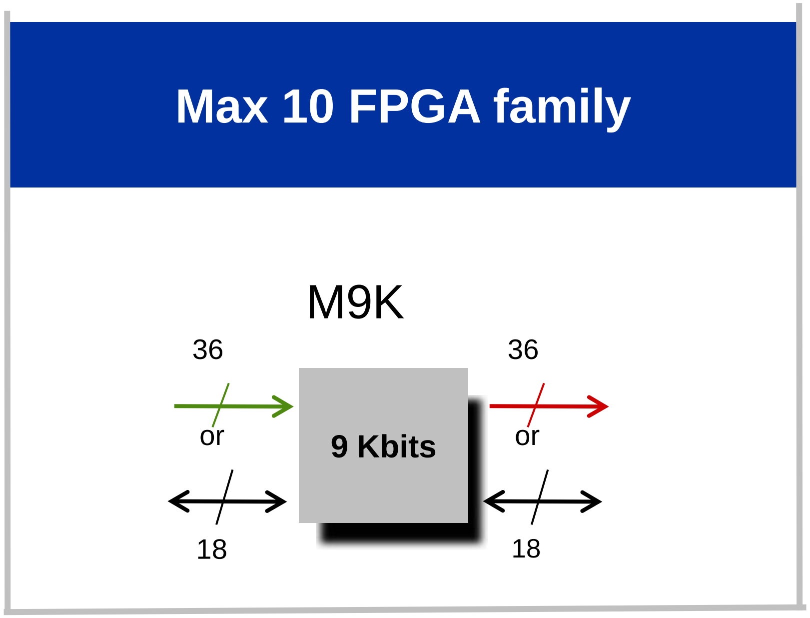
Robust clocking resources to support system integration

☞ *[Click to return to Architectural Sections]*

Max 10 FPGA – Internal Memory

Max 10 FPGAs – M9K Embedded RAM Blocks

Feature	M9K	Benefit
Block Size	9 Kbits	Optimizes Memory
Performance	Up to 315 MHz	Hi speed Performance
Dual-Port Read During Write Behavior	New Data or Old Data	Flexibility and Ease of Use
Parity Bit	Yes	Usability for High Reliability Apps
Clock Enables	4	Increased Flexibility and Reduced Power
Read and Write Enables	4	Increased Flexibility and Reduced Power



Max 10 FPGAs – M9K Block Key features

- **9,216 RAM bits including parity bits**
  - Variable port width configurations of x1, x2, x4, x8, x9, x16, x18, x32 and x36
  - Synchronous only operation operating up to 315 MHz
  - Parity support by storing one extra bit per byte in x9, x18 and x36 modes.
- **Data options**
  - Byte enable support for data input masking during write
  - Address stall for efficiency in cache-miss applications
  - Same-port read-during-write to read out new data
  - Same-port read-during-write to read out old data
- **Port options**
  - Single-port mode and simple dual-port mode supported for all port widths
  - True dual-port operation in x1, x2, x4, x8 x9, x16 and x18 modes
  - Pack mode in which 9k MEAB is split into two 4.5k single port RAMs
  - Mixed-port same-clock read-during-write to read out old data.
- **Control options**
  - total of 4 clock enable controls.
  - Separate read enable and write enable for each port.
  - Asynchronous clear for output latches
  - Asynchronous clear for address registers.
- **ROM mode with preload supported for all port widths***

**** Feature available depending on configuration option used.***

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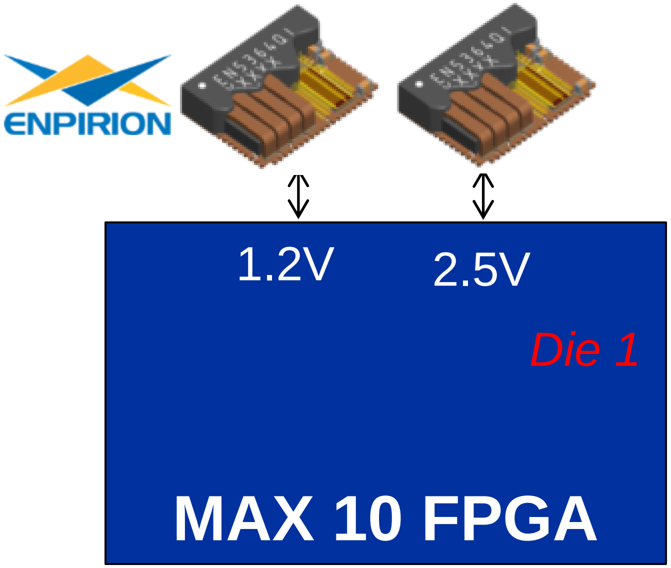
Max 10 FPGA – Voltage Regulator

MAX 10 FPGA – Optional Integrated Linear Regulator

Option 1 – Dual Supply



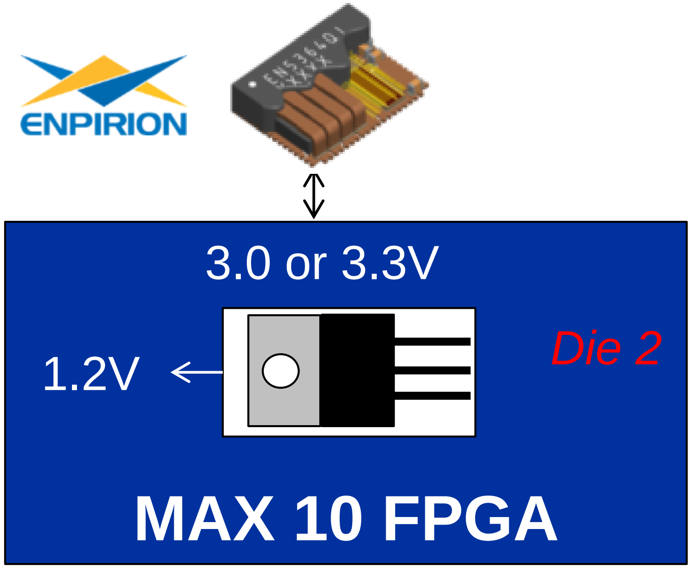
1.2V

2.5V

Die 1

MAX 10 FPGA

Option 2 – Single Supply



3.0 or 3.3V

1.2V ←

Die 2

MAX 10 FPGA

- **Higher Performance**
- **More Features**
- **Higher Power Efficiency**

- **Simple, compact PCB**
- **Lower BOM cost**

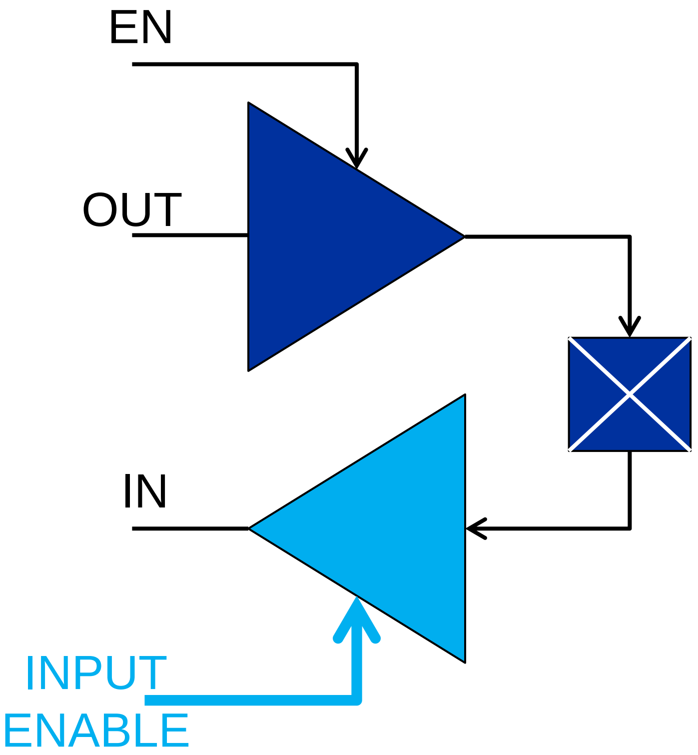
☞ *Click to return to Architectural Sections*

Max 10 FPGA – Power Savings

Max 10 FPGA – Dynamic Input Buffer Disable

- **Power down high performance input buffers**
- **No FPGA reconfiguration needed**
- **Automatic and/or User Control**

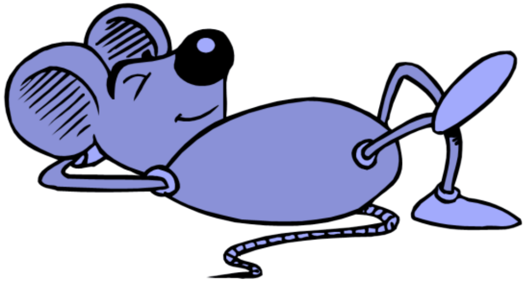
I/O Type	**Control Source**
External Memory Interface	Memory Controller (during IDLE and WRITE)
LVDS	User Control

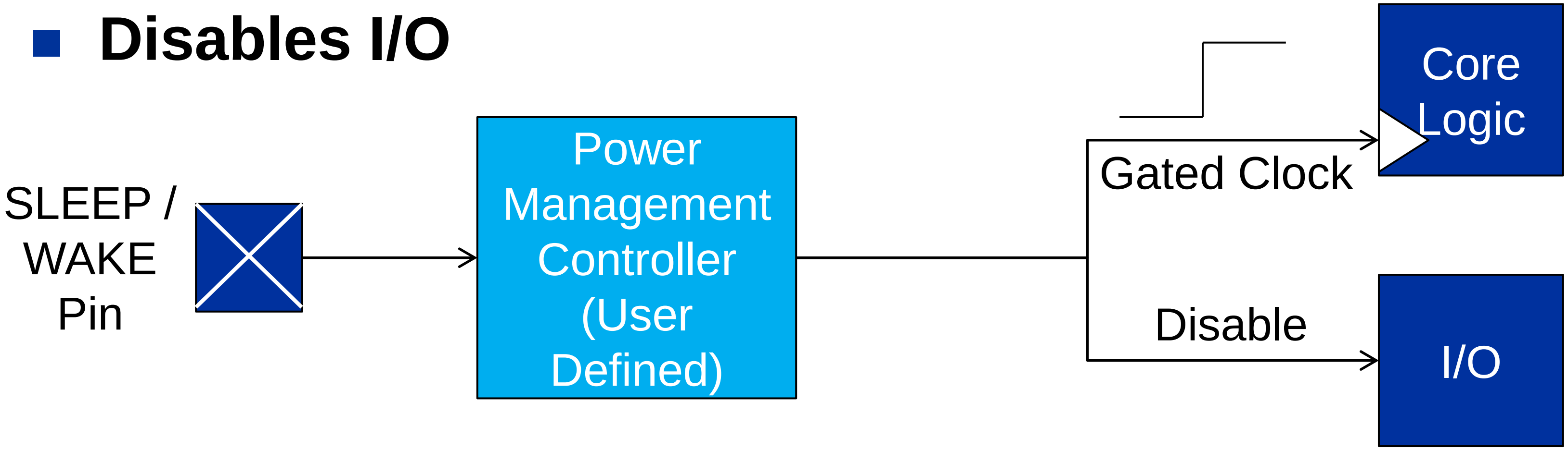


Saves Operating and Standby Power

Max 10 FPGA – Sleep Mode Capability & Ref. Design

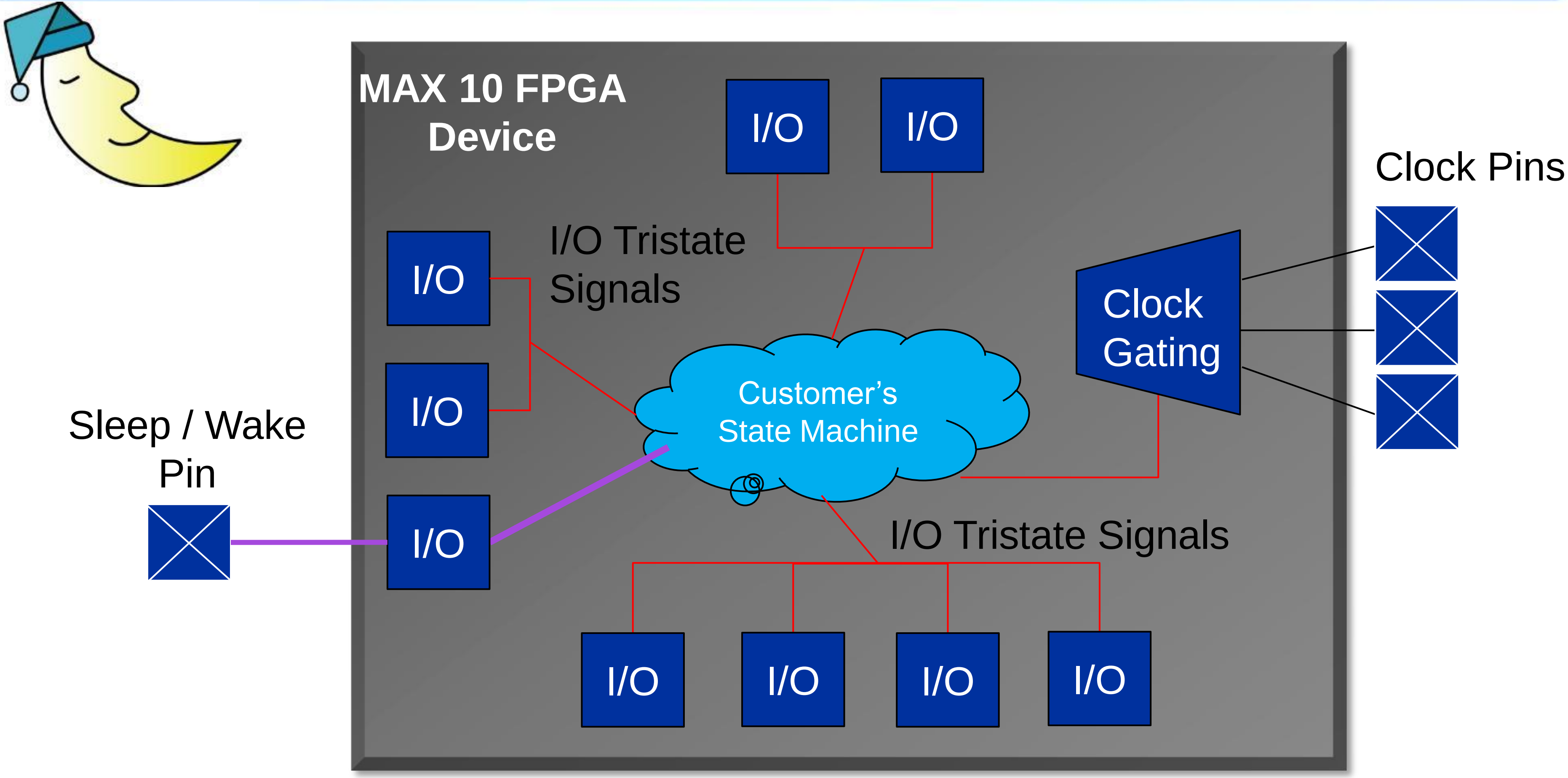
- **Low power mode without losing state**
- **External control via single pin**
- **Wake-up from sleep in < 1 ms**
- **Gates clocks to internal logic**
- **Disables I/O**





Reference Design Available

MAX 10 FPGA – “Sleep” Mode



5%-95% Dynamic Power Reduction

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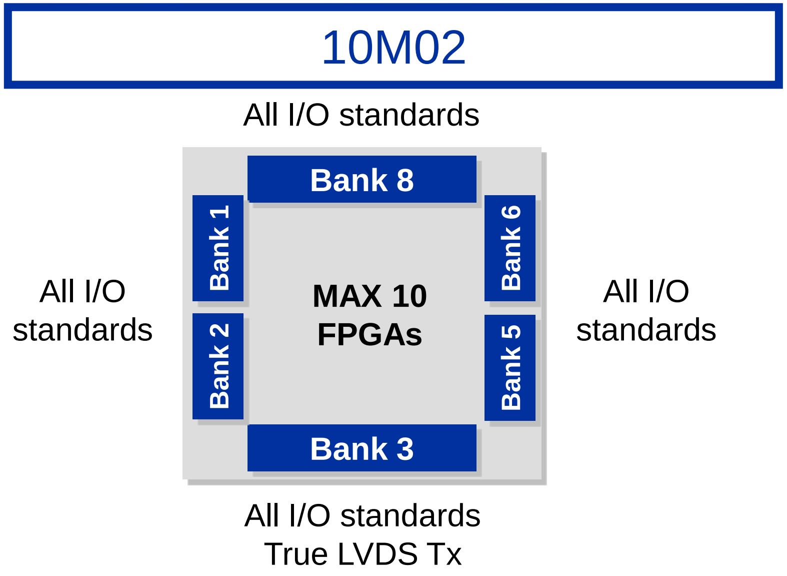
MAX 10 FPGAs – General Purpose I/O (GPIO)

MAX 10 FPGAs – I/O Features & Benefits

I/O features	Benefit
Multiple interfaces, standards, and features supported	■ Easily bridge between different devices having different voltage levels or protocols ■ Flexible I/O placements for easier PCB design and to reduce board area
Large number of I/O banks	■ Better granularity to mix and match different I/O requirements
Abundant I/O element registers	■ Increase external memory interface performance ■ Improve Tco performance
Dedicated differential output buffers	■ Eliminate external resistors for LVDS, RSDS, and mini-LVDS transmission ■ LVDS interfaces up to 830 Mbps
Selectable series OCT (some with calibration)	■ On-chip termination reduces external passive cost & calibration eliminates variations due to PVT
Adjustable slew rates	■ Improve signal integrity by slowing down edge rates on non-performance-critical I/O pins

MAX 10 FPGAs – I/O Bank Details

- **Interface to 3.3, 2.5, 1.8, 1.5, and 1.2V logic levels**
- **3.3V PCI 32-bit, 33 MHz compatible**
  - PCI clamp diode on all pins
- **Output enable per pin**
- **Noise control features**
  - Schmitt Triggers
  - Three step slew rate
  - Programmable output drive strength
- **Emulated-LVDS I/O on all banks**
  - True LVDS I/O, bottom banks only
- **On-chip series termination & Hot-Socket Compliant**

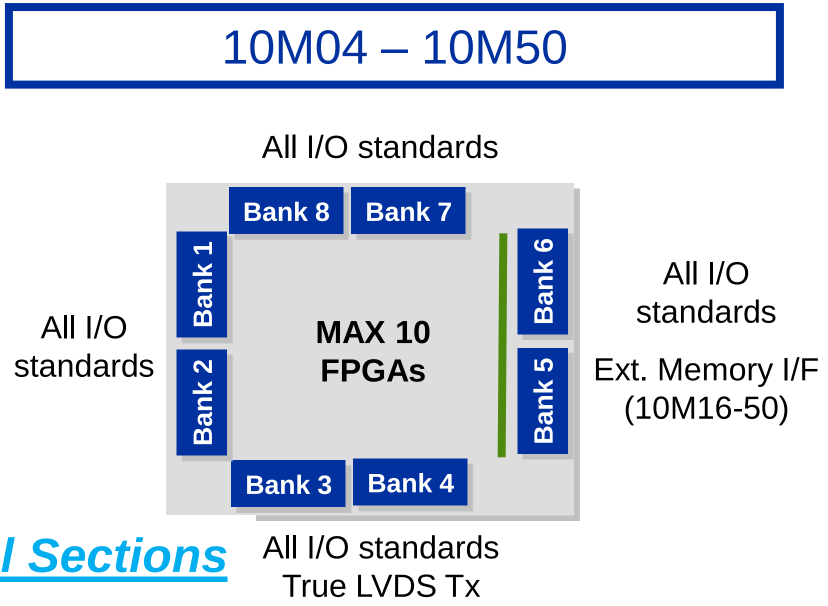

10M02

All I/O standards

All I/O standards

All I/O standards

All I/O standards
True LVDS Tx


10M04 – 10M50

All I/O standards

All I/O standards

All I/O standards

Ext. Memory I/F (10M16-50)

All I/O standards
True LVDS Tx

Click to return to Architectural Sections

MAX 10 FPGAs – LVDS I/O

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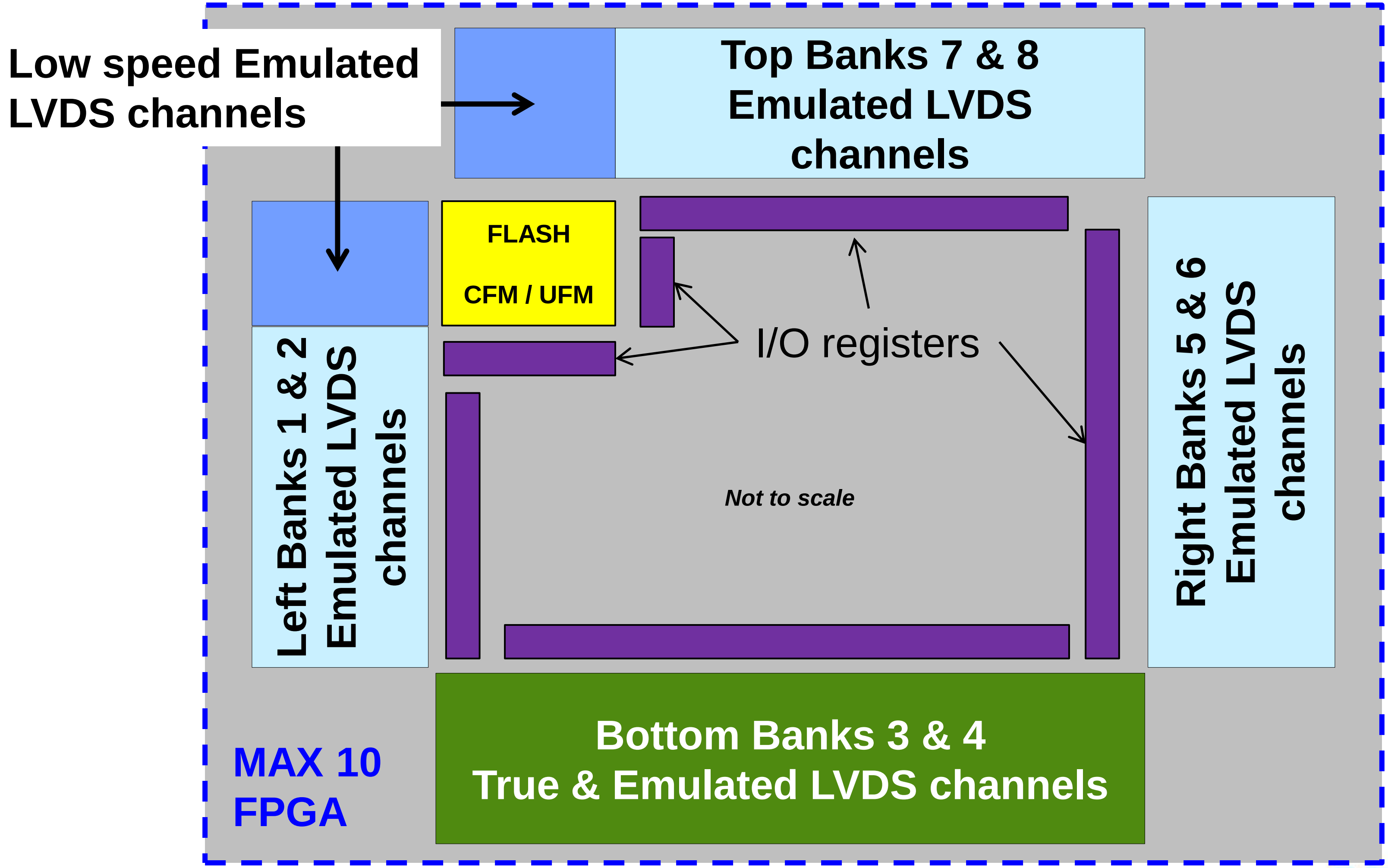
MAX 10 FPGA – LVDS on Every I/O

LVDS Type	Description	Performance	
		Single-Supply Voltage	Dual-Supply Voltage
True	Full differential matched channel Rx / Tx (Banks 3, 4)	Up to 400 Mbps	Up to 830 Mbps
Emulated	Requires external 3-resistors at Tx (Banks 2, 5, 6, 7)	Up to 285 Mbps	Up to 600 Mbps
Low speed Emulated	Requires external 3-resistors at Tx (Banks 1a, 1b, 8)	Up to 200 Mbps	Up to 380 Mbps

Performance & Termination is Location/Bank Dependent

MAX 10 FPGA – LVDS I/O Floorplan



Low speed Emulated LVDS channels

Top Banks 7 & 8 Emulated LVDS channels

FLASH

CFM / UFM

I/O registers

Left Banks 1 & 2 Emulated LVDS channels

Right Banks 5 & 6 Emulated LVDS channels

Not to scale

Bottom Banks 3 & 4
True & Emulated LVDS channels

MAX 10 FPGA

MAX 10 FPGA – LVDS Performance by Speed Grade (Dual-Supply Voltage)

LVDS Type	I/O Signal Name	Data Direction	Performance (Mbps)				
			-i6	-c7	-i7	-a7	-c8
True	LVDS	Rx (input toggle rate)	830	720	720	620	640
		Tx (output toggle rate)	800	720	720	620	640
Emulated	LVDS_E_3R	Rx (input toggle rate)	600	600	600	535	550
		Tx (output toggle rate)	600	600	600	535	550
Low speed Emulated	LVDS_E_3R (flash region)	Rx (input toggle rate)	380	300	300	290	300
		Tx (output toggle rate)	380	300	300	290	300

MAX 10 FPGA – LVDS Performance by Speed Grade (Single-Supply Voltage)

LVDS Type	I/O Signal Name	Data Direction	Performance (Mbps)				
			-i6	-c7	-i7	-a7	-c8
True	LVDS	Rx (input toggle rate)	380	290	290	195	200
		Tx (output toggle rate)	380	290	290	195	200
Emulated	LVDS_E_3R	Rx (input toggle rate)	285	285	285	195	200
		Tx (output toggle rate)	285	285	285	195	200
Low speed Emulated	LVDS_E_3R (flash region)	Rx (input toggle rate)	200	200	200	200	200
		Tx (output toggle rate)	200	200	200	200	200

MAX 10 FPGA – # of LVDS I/O Channels

Location	Top Banks (emulated)		Bottom Banks (true-LVDS)		Left Banks (emulated)		Right Banks (emulated)	
Device	Rx	Tx	Rx	Tx	Rx	Tx	Rx	Tx
10M02	15	15	17	8	22	22	26	26
10M04	30	30	30	15	30	30	36	36
10M08	30	30	30	15	30	30	36	36
10M16	38	38	40	20	38	38	44	44
10M25	46	46	48	24	42	42	54	54
10M40	56	56	60	30	62	62	72	72
10M50	56	56	60	30	62	62	72	72

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MAX 10 FPGA – External Memory Interface (EMIF)

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MAX 10 FPGA – EMIF Overview

Industry's Lowest Cost & Long-Life Memories

Device / Protocol	Configuration	Max Total DRAM Bandwidth (Gbps)	Max I/O Data Rate (MHz)	MAX 10 FPGA
SRAM	Up to x36	-	100	All
DDR3 / 3L	Up to 1 x16 (ECC option)	9.6	300	10M16 or larger densities (1)
DDR2	Up to 1 x16 (ECC option)	6.4	200	
LPDDR2	Up to 1 x16 (no ECC)	6.4	200	

4th generation Low-Cost I/F architecture

	MAX 10 FPGA	Higher-End Altera FPGAs
Objective	Low cost	Performance & flexibility
PHY	Soft IP: UniPHY – Proven solution Silicon features: Easy timing closure	UniPHY – NIOS-based solution for multiple protocols & high performance
Controller	Soft IP – no wasted device resources if design doesn't need EMIF	Soft/Hard- High speed, low latency, and high through-put

Note 1: EMIF only available on dual-supply voltage device/package options.

EMIF – Wide Range of Options in Low-Cost Families

Device	**Altera Controller + PHY**				**Partner Controller + PHY**
	DDR3 (MHz)	DDR2 (MHz)	LPDDR2 (MHz)	DDR (MHz)	Various
Cyclone® III	-	200	-	167	✓
Cyclone III LS	-	167	-	150	✓
Cyclone IV GX	-	200	-	167	✓
Cyclone IV E	-	167	-	133	✓
Cyclone V (HMC)	400	400	333	-	✓
MAX 10 FPGA	300	200	200	-	✓

Notes:

1. ***HMC = Hard Memory controller (part of die silicon). All other solutions use soft IP cores.***
2. ***Performance targets are for the fastest speed grade, not available in all speed grades.***
3. ***Memory solution partners include:***
    - ***Northwest Logic***
    - ***Microtronix***
    - ***CAST***

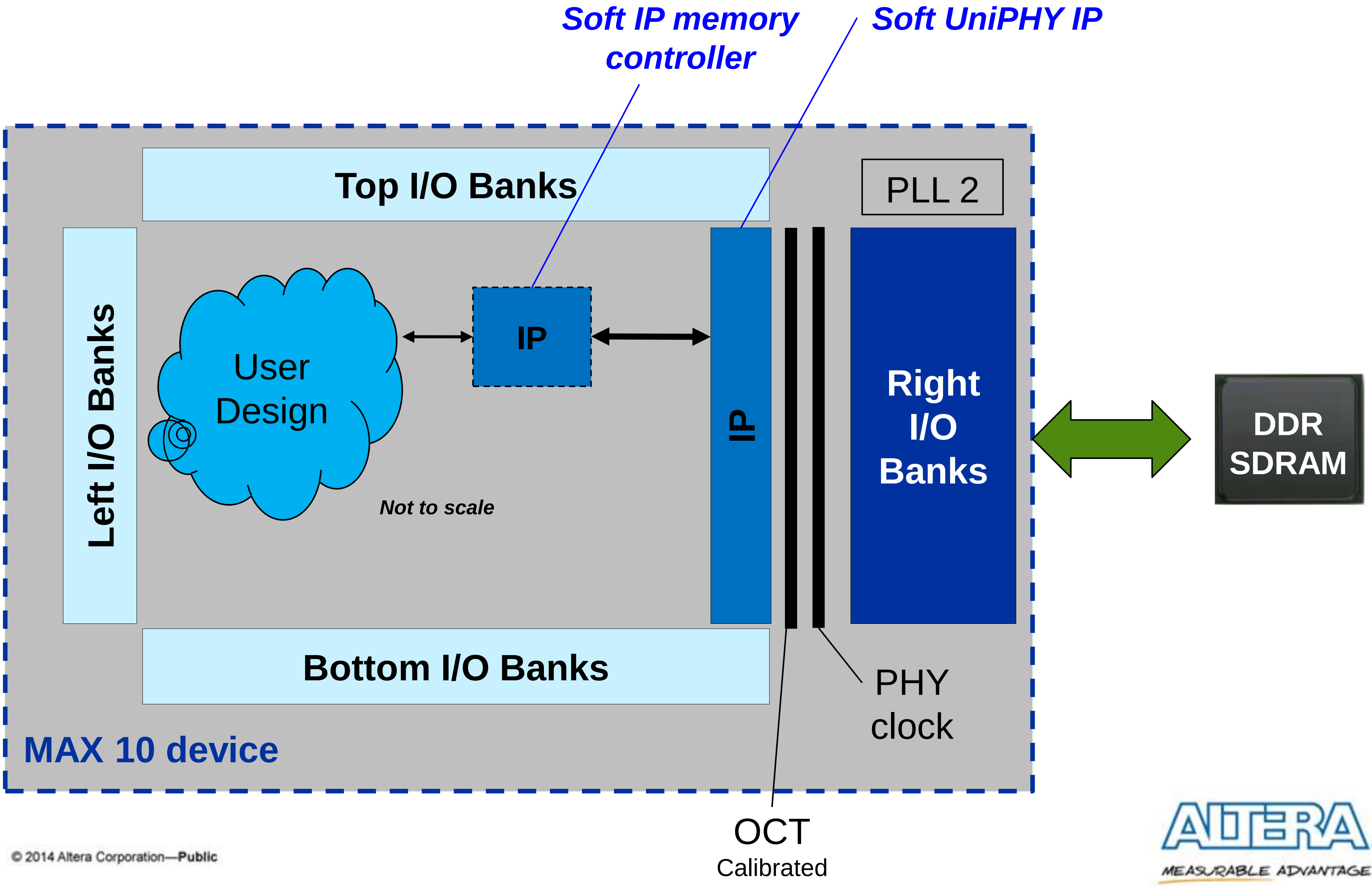
MAX 10 FPGA – EMIF Support by Speed Grade

Memory Standards	**-i6 Speed** (2)	**-c7 Speed**	**-i7 Speed**	**-a7 Speed**	**-c8 Speed**
	1 Rank / CS	1 Rank / CS	1 Rank / CS	1 Rank / CS	1 Rank / CS
DDR3 / 3L	300 MHz	TBD (3)	-	TBD (3)	-
DDR2	200 MHz	167 MHz	167 MHz	TBD (3)	-
LPDDR2	200 MHz	TBD (3)	-	-	-

Note:

1. ***EMIF is only supported on the right side I/O banks (10M16 – 10M50 device densities) for dual-supply voltage package options.***
2. ***Industrial -6 speed grade is 'hidden' in Quartus (visible but greyed out). File SR to request review & approval to unlock p/n.***
3. ***Pending device characterization.***

MAX 10 FPGA – EMIF Solution Floorplan



MAX 10 FPGA – EMIF Maximum Width Support by Package

Device	U324	F256	F484	F672
10M16	x8, x16 LPDDR2	x8 (no ECC), x16 LPDDR2	x8, x16 LPDDR2	-
10M25	-		x8, x16	x8, x16
10M40	-			
10M50	-			

Note: Only available in dual-supply package options and I/O Banks 5 & 6.

MAX 10 FPGA – EMIF # DQ Groups Available by Package

Device	Package	U324	F256	F484 (2)	F672
10M16	Bank 5, 6	1, 1	1, 1	1, 1	-
10M25	Bank 5, 6	-	1, 1	2, 1	2, 1
10M40	Bank 5, 6	-	1, 1	2, 2 (3)	2, 2 (3)
10M50	Bank 5, 6	-	1, 1	2, 2 (3)	2, 2 (3)

Notes:

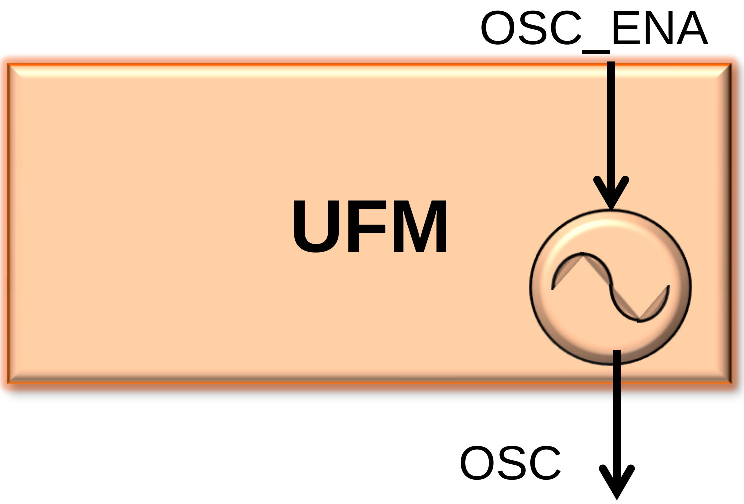
1. ***One DQ group = 12 pins total (DQS, DQS#, DM, 9x DQ)***
2. ***Only two x8 DQ groups support vertical pin-out migration from 10M16 → 10M50.***
3. ***Only one x8 DQ group from this bank can support vertical pin-out migration between the 10M25 → 10M50.***

☞ *Click to return to Architectural Sections*

MAX 10 FPGA – Internal Oscillator

MAX 10 FPGA – Internal Oscillator Clock Source

- **Uninterruptable clock source**
- **Great for self-running circuits:**
  - Watchdog Timer
  - Sleep mode controller
- **Ring oscillator based**
  - 3.75 to 7.5 MHz die variable range, nominally 6.25 MHz
- **Located inside the UFM; accessible by the core fabric**



	Internal Oscillator Frequency
Minimum	3.75 MHz
Typical	6.25 MHz
Maximum	7.5 MHz

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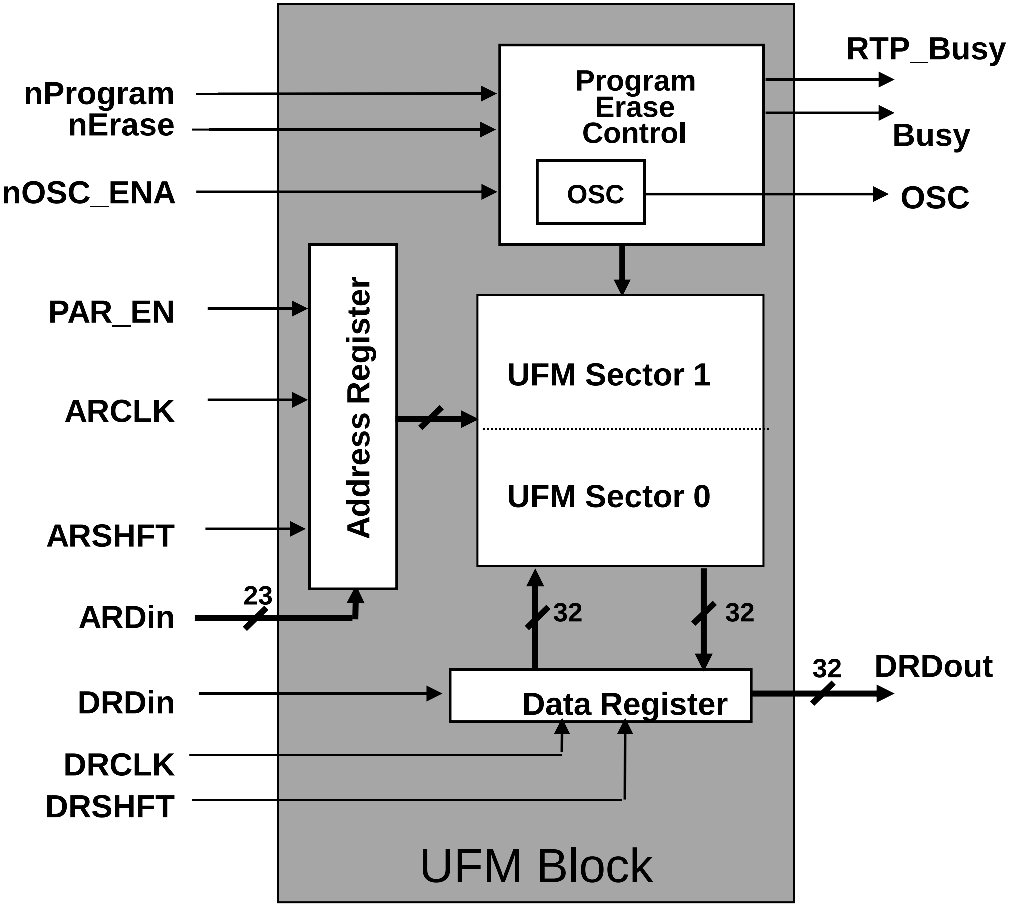
MAX 10 FPGA – User Flash Memory (UFM)

MAX 10 FPGA - UFM Block Overview

- **User Flash Memory Block**
  - Up to 512 Kbits on largest device
- **Supports native 32-bit parallel interface**
  - Enhancement over MAX II/V UFM
  - Up to 320 Mbps read bandwidth
- **SPI and I²C soft interfaces supported in Quartus® II s/w**
- **Page and Sector erase support**
- **Integrated UFM oscillator available to core**



MAX 10 FPGA – Size of UFM

Device	Page Size (bits)	Pages / Sector	# of Sectors	Total UFM Size (bits)
10M02	16,384	3	2	98,304
10M04	16,384	8	1	131,072
10M08	16,384	8	2	262,144
10M16	32,768	4	2	262,144
10M25	32,768	4	2	262,144
10M40	65,536	4	2	524,288
10M50	65,536	4	2	524,288

Use-Models Include Scratch-Pad Memory for Nios II Processor Code

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MAX 10 FPGA – Device Configuration

MAX 10 FPGA – Configuration Flash Memory (CFM)

- **Instant On Configuration**
- **Single or Dual Images**
- **Less Board Space**
- **Smaller Bill of Materials**
  - Reduces assembly costs
  - Simplified inventory management
- **Increased Security**
  - No exposed external interface

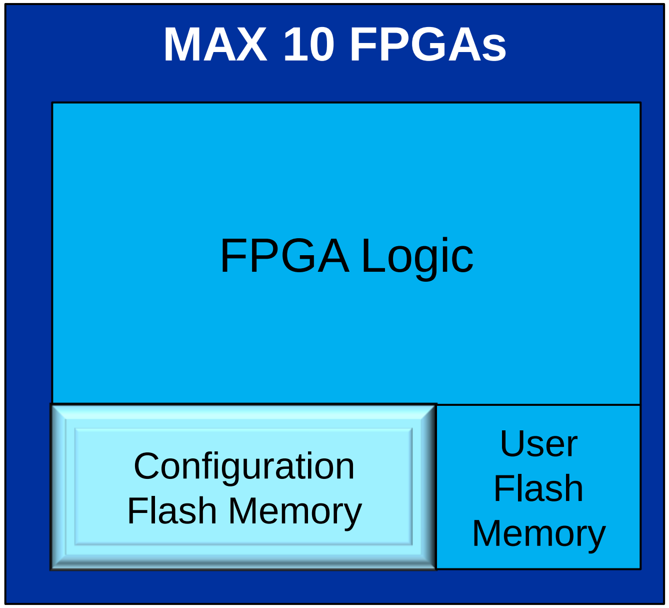
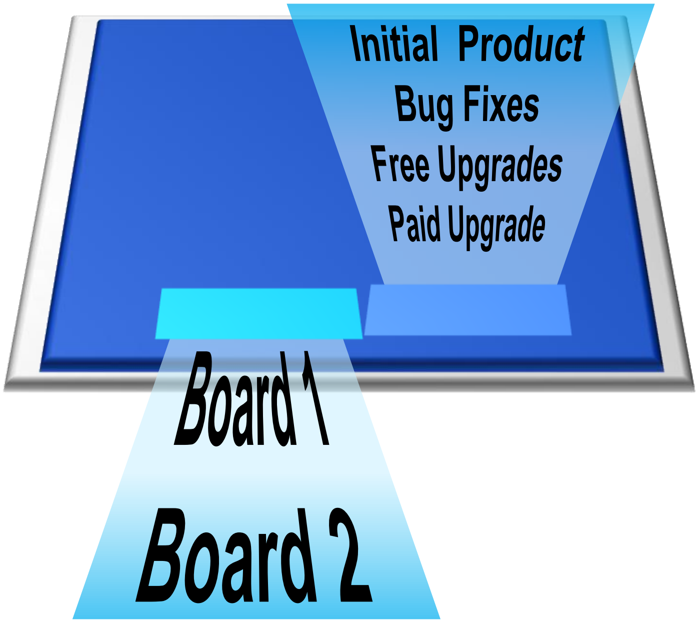


Figure Not to Scale

Many Benefits to Integrated Configuration Flash

MAX 10 FPGA – Dual Image Configuration Benefits

Capability	Use
Remote System Upgrade w/Fail-Safe Upgrade	Ship System Sooner
	Free Upgrades for Older Systems
	Paid Upgrades
Dual Personas	Reduce logic density by time multiplexing algorithms
	Reduce supply chain by combining multiple SKU’s into one pre-programmed device



Infinite Possibilities with Dual Image Configuration

MAX 10 FPGA – Dual Persona Configuration

- **BOOT_SEL input pin selects one of two images from Configuration Flash Memory (CFM)**

Use Case	Example
Two Images on the Same Board	Instantly switch between two image processing algorithms.
One Image Per Board, on Two Boards	Consolidate two different sockets into a single BOM line item.

Dual Personas.

Endless Possibilities.

MAX 10 FPGA – Minimum Configuration Time (ms)

Product Line	Uncompressed, Unencrypted
10M50	3
10M40	3
10M25	2
10M16	2
10M08	1
10M04	1
10M02	1

Configures in Milliseconds

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MAX 10 FPGA – Configuration Flash Programming Methods

	Programming Method	Use Model
From JTAG	In System Programming (ISP)	Program configuration flash memory, right from the system board. User Flash Memory can also be programmed via ISP.
	Real Time ISP	Updates take effect at user defined time, or at next power cycle.
From FPGA User Mode	Remote System Upgrade (RSU)	Erase, Write, and Verify configuration flash memory from inside a user mode FPGA design.

Multiple Ways to Program Configuration Flash Memory

☞ *Click to return to Architectural Sections*

MAX 10 FPGA - Design Security

MAX 10 FPGA - Design Security – Deny the Counterfeiters!

- **Single chip solution with up to 2 secure images**
- **Advanced Encryption Standard (128-bit AES) protection**
  - Non-volatile key for internal configuration
- **JTAG port security protection**
  - Read disable or Read/Write disable (OTP)
  - Prevents reverse engineering
- **Embedded unique identification (ID)**
  - 64 bit unique ID for traceability

Comprehensive Monolithic Design Protection

☞ [Click to return to Architectural Sections]

MAX 10 FPGA – Single Event Upset (SEU) Mitigation

MAX 10 FPGA - SEU Circuitry Features & Benefits

Function	Feature	MAX 10 FPGAs	Benefits
Detect	**Configuration RAM (CRAM) CRC**	✓ Embedded in silicon	Checking continuously in the background
	Error Detection Time	✓ Device density dependent	Fast
	User RAM SEU Detection	✓ Soft IP	Knowledge of data corruption
Fix	**User RAM Correction**	✓ Soft IP for M9K	ECC option

**** CRC = Cyclic Redundancy Check circuitry***

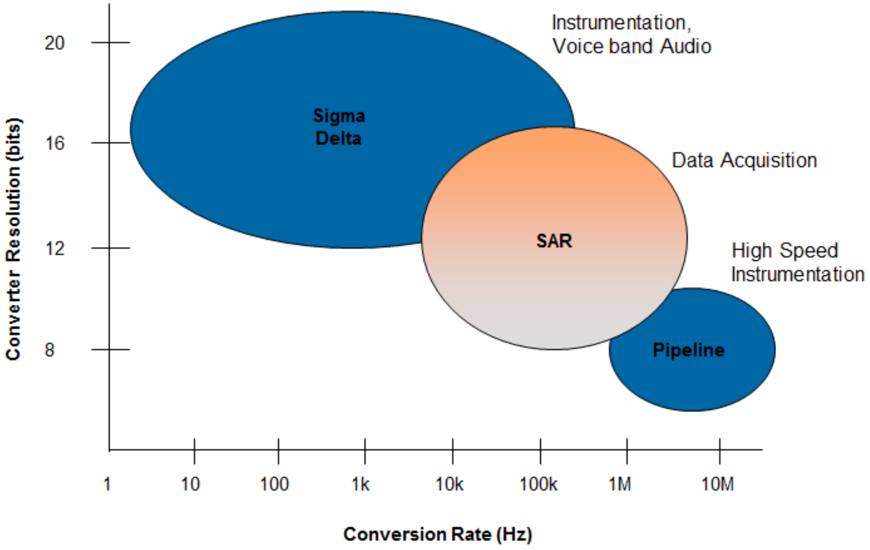
SEU Detection Capability

☞ *Click to return to Architectural Sections*

MAX 10 FPGA – Analog Block

An Overview of ADC Architectures

- **Three Main Types of ADC**
  - Sigma Delta
  - Successive Approximation Register (SAR)
  - Pipeline

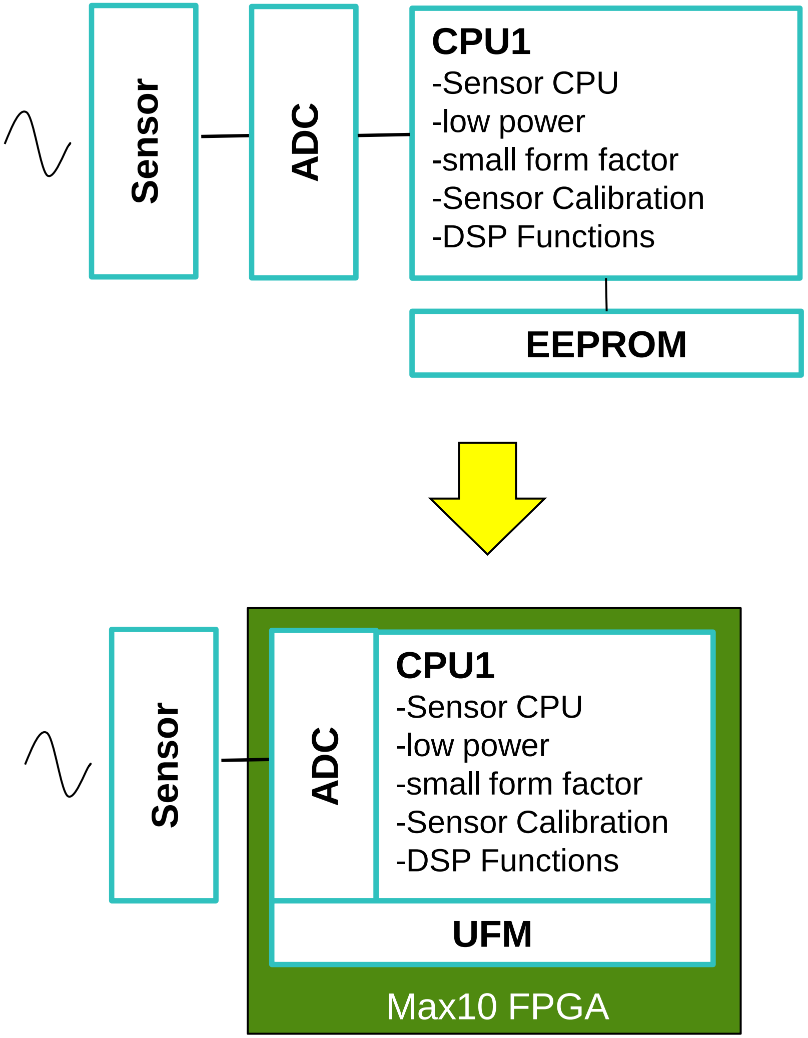


- **The selection of the right architecture is a very crucial decision**

- **ADC's are generally characterised in three ways**
  - Bandwidth or Conversion Rate
  - Resolution
  - Input Voltage Range

MAX 10 FPGA - Advantages of Hard IP Integration

- **The real world is analog**
  - Integration of analog blocks allows direct mixed signal support
  - Reduce components at front end

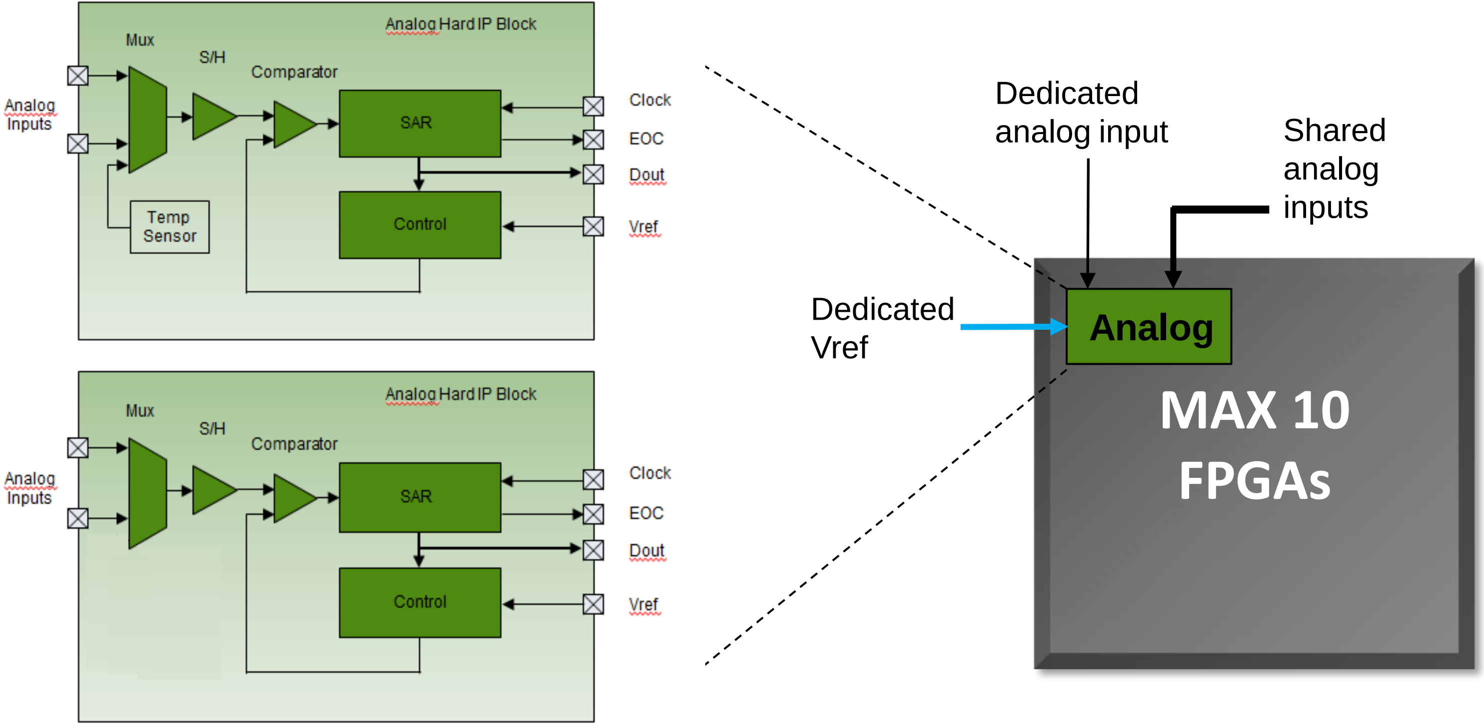


- **Benefits of Integration**
  - Reduced device I/O count
  - GUI based configuration
  - Flexible sample sequence
  - Faster data output
  - Simultaneous Sampling

- **$$$ + space savings!**

MAX 10 FPGA - Analog Hard IP Block

- Up to two, 12-bit SAR ADCs
  - 1 Msps (each ADC)
  - 18 Analog inputs (Max.)
  - 1 Temperature Sensing Diode
- Two dedicated inputs
- Selectable Voltage Prescalers
- Selectable for temperature and Voltage measurements



MAX 10 FPGA - ADC Channel Count vs. Package

- **ADC Channel GPIO count per device / package option**
  - Additional Dedicated Analog input per ADC block
  - Additional Temperature Sensing Diode only available on ADC1
  - Only 8 channels are able to migrate from 10M04 to 10M50 for ADC1

Package Details	Type	36-WLCSP	81-WLCSP	144-EQFP	153-MBGA	169-UBGA	256-FBGA	324-UBGA	484-FBGA	672-FBGA
	Voltage	Dual	Dual	Single	Single	Single	Dual	Dual	Dual	Dual
MAX 10 FPGA	10M04	-	-	8+0 ↑	8+0 ↑	8+0 ↑	16+0 ↑	16+0 ↑	16+0 ↑	-
	10M08	-	-	8+0	8+0 ↓	8+0	16+0	16+0	16+0	-
	10M16	-	-	8+0	-	8+0 ↓	16+0	16+0 ↓	16+0	-
	10M25	-	-	8+0	-	-	8+8	-	8+8	8+8 ↑
	10M40	-	-	8+0	-	-	8+8	-	8+8	8+8
	10M50	-	-	8+0 ↓	-	-	8+8 ↓	-	8+8 ↓	8+8 ↓

Note: ADC Channel Count = ADC1 + ADC2

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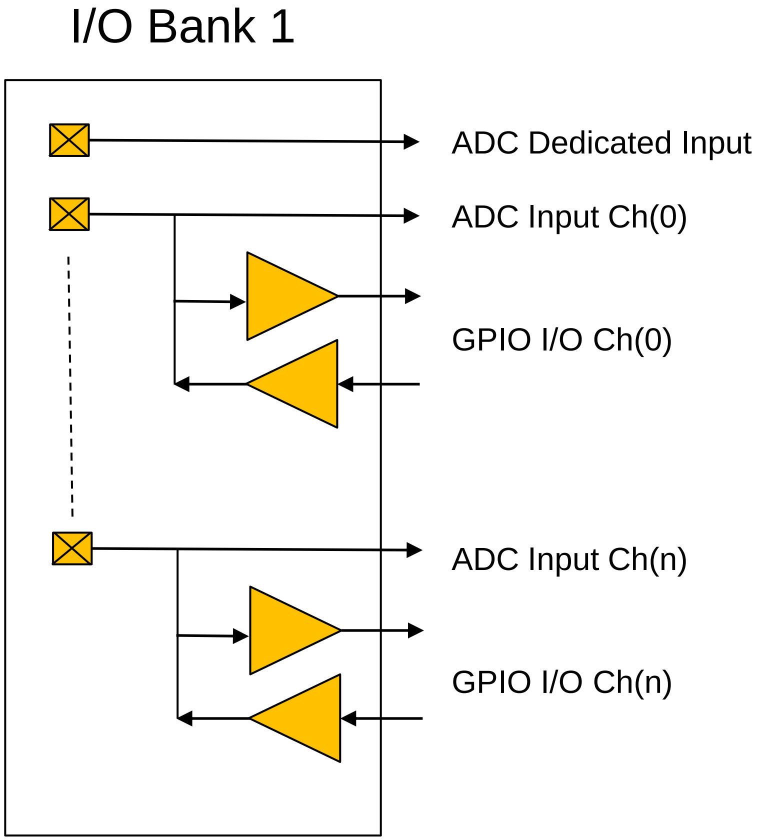
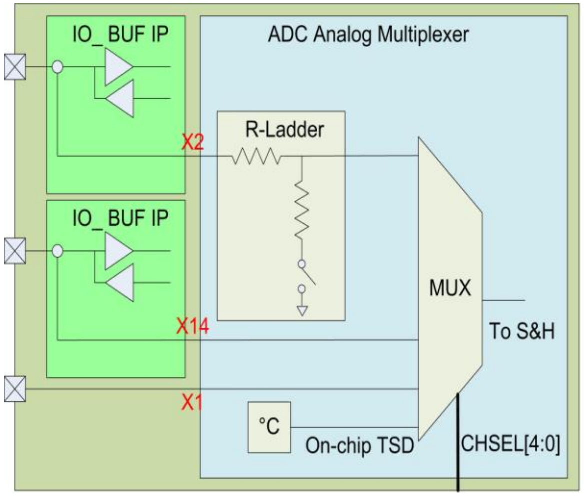
MAX 10 FPGA - Analog Inputs

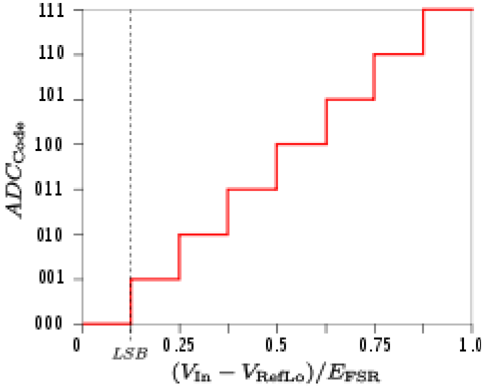
- **I/O Bank1 used for analog inputs or GPIO**
- **17 or 18 analog inputs total**
  - 1 dedicated per ADC
  - 16 Shared pad with GPIO
    - Includes single prescaler channel
  - 1 temp. sensing diode (ADC1 only)
- **All GPIO buffers in Bank1 are tri-stated if ADC is used.**



MAX 10 FPGA - ADC Input Prescalar

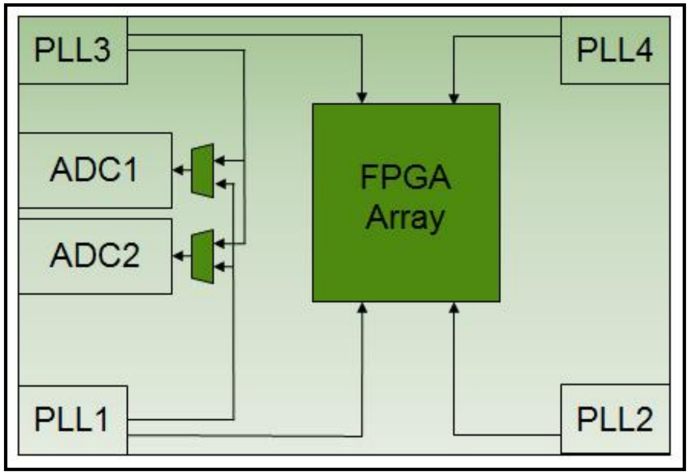
- **Each MAX10 device will have two Prescalers**
  - Prescaler (aka R-Ladder) divides the Analog input by half.
  - Increases maximum Analog input voltage to 3.0-V on Dual Voltage devices & 3.6V in single supply mode.
  - Effects the ADC output code, reduced voltage produces different output code value
  - Available on two channels only
  - Enabled separately for each channel in the Megawizard





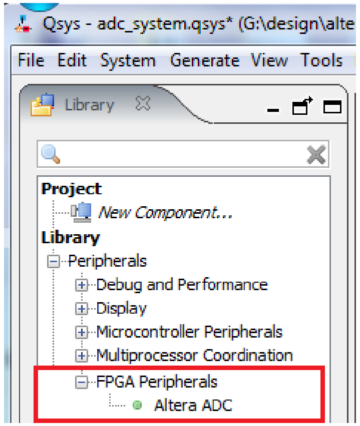
MAX 10 FPGA - Altera_adc Clocking

- **ADC's support clocks from two PLLs**
  - Top-left and bottom-left
- **PLL will not be generated as part of the Magawizard**
  - Customer will need to connect it.
  - Restricted to PLL1 or PLL3
- **Internal Clock Divide Block**
  - Voltage – Divide 1, 2, 10, 20, 40, 80
  - Temperature – Divide 10, 20



MAX 10 FPGA - Altera_adc Megawizard

- **New Analog ADC Megawizard will be located in the Peripherals library**

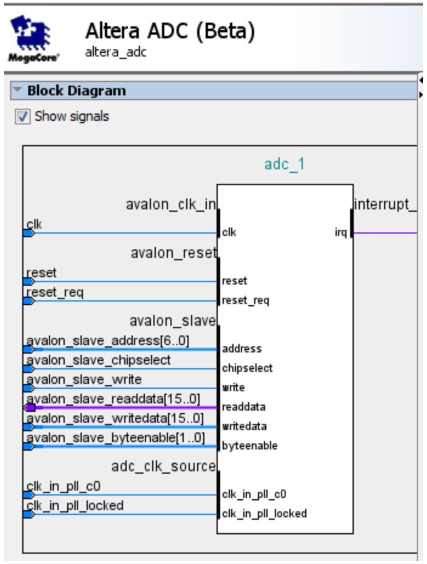


Project
- *New Component...*

Library
- Peripherals
  - Debug and Performance
  - Display
  - Microcontroller Peripherals
  - Multiprocessor Coordination
  - FPGA Peripherals
    - Altera ADC

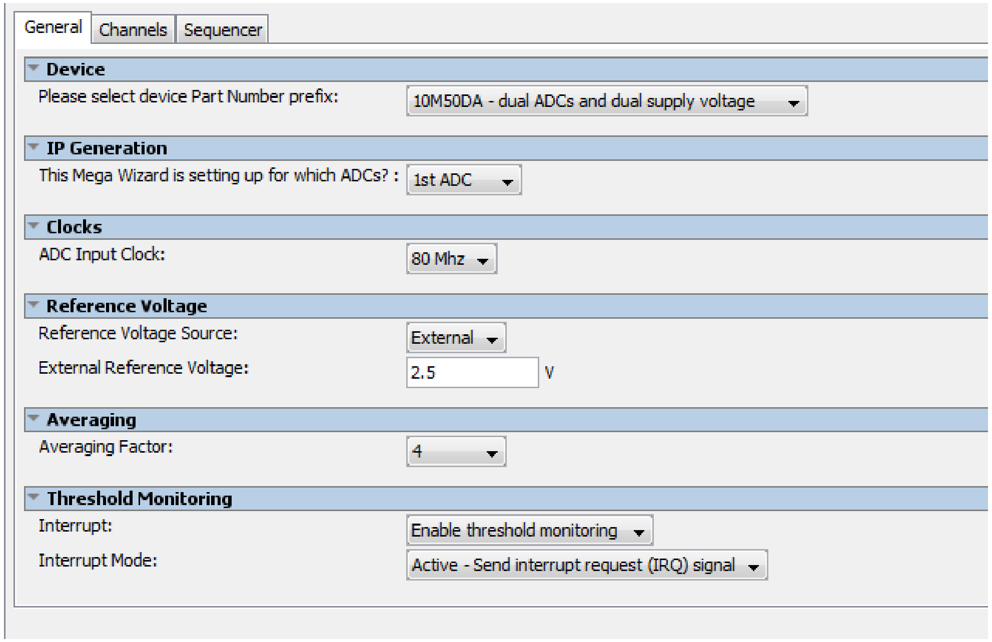
Proposed location of the new altrea_adc soft IP

- **Megawizard Support Schedule**
  - Single ADC → ACDS rev. 14.0
  - Dual ADC → future release (Beta)



MAX 10 FPGA - Altera_adc Megawizard (Tab 1)

- **General Tab**
  - Device
    - ADC's are package dependant
  - ADC (Single or Dual)
    - Include TSD
  - Input Clock frequency
  - Reference Voltage selection
  - Global Averaging Factor
    - Setting 4, 8,16 or 32
  - Threshold Monitoring
  - Interrupt Mode



Device

Please select device Part Number prefix: 10M50DA - dual ADCs and dual supply voltage

IP Generation

This Mega Wizard is setting up for which ADCs? : 1st ADC

Clocks

ADC Input Clock: 80 Mhz

Reference Voltage

Reference Voltage Source: External

External Reference Voltage: 2.5 V

Averaging

Averaging Factor: 4

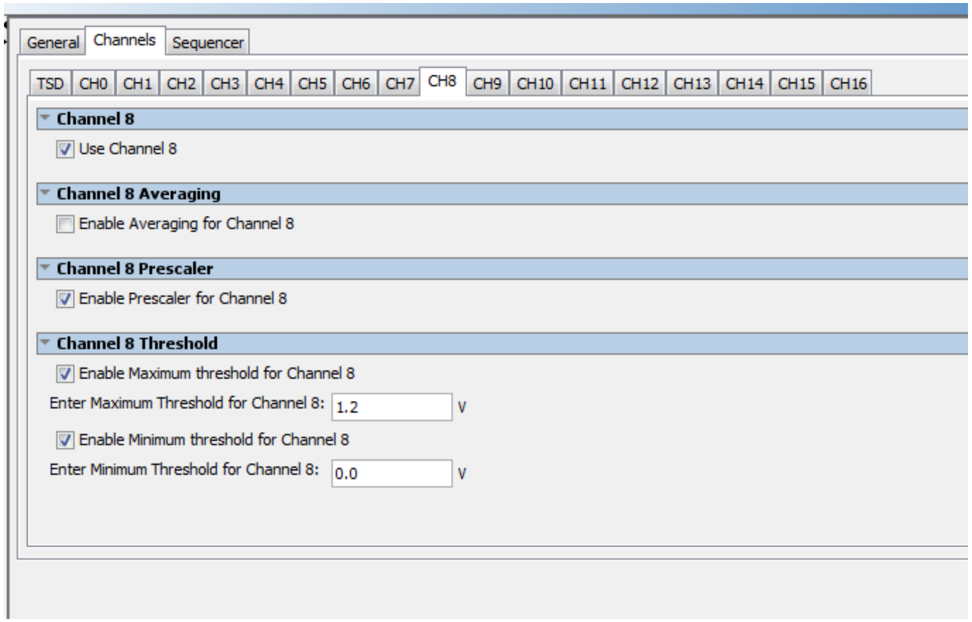
Threshold Monitoring

Interrupt: Enable threshold monitoring

Interrupt Mode: Active - Send interrupt request (IRQ) signal

MAX 10 FPGA - Altera_adc Megawizard (Tab 2)

- **Channel Tab**
  - Individual Channel Set up
    - Enable PreScalers
    - Enable Averaging
    - Set Min / Max Threshold Flag Value
      - Beta @ ACDS 14.0
    - Specify Desired Sample Frequency (future feature)



Channel 8

☑ Use Channel 8

Channel 8 Averaging

☐ Enable Averaging for Channel 8

Channel 8 Prescaler

☑ Enable Prescaler for Channel 8

Channel 8 Threshold

☑ Enable Maximum threshold for Channel 8

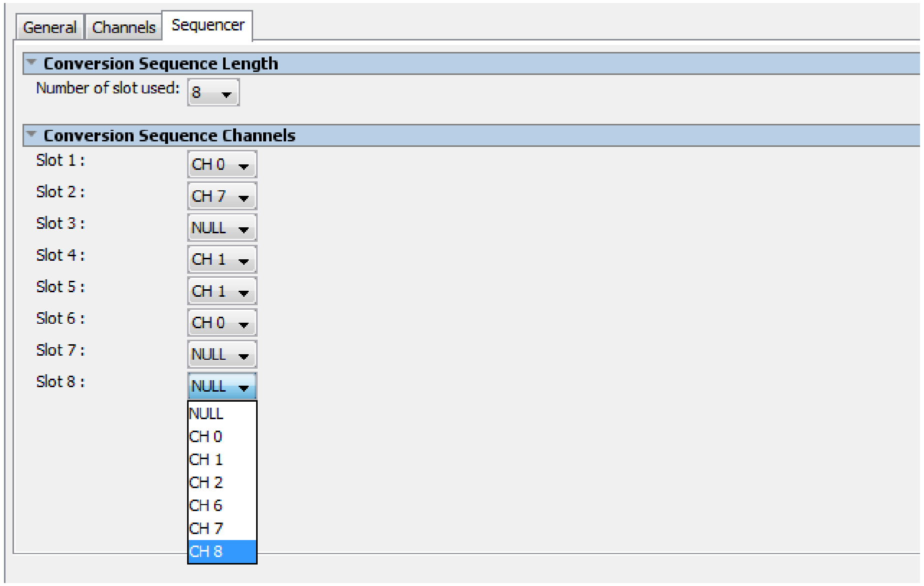
Enter Maximum Threshold for Channel 8: 1.2 V

☑ Enable Minimum threshold for Channel 8

Enter Minimum Threshold for Channel 8: 0.0 V

MAX 10 FPGA - Altera_adc Megawizard (Tab 3)

- **Soft Sequencer enables tighter control of ADC**
  - User defined start register
- **Sequencer Tab**
  - Configurable Sample Sequence
  - User defines sequence length and the channel order
    - Max 64 sequence length
  - Runtime update supported via Avalon MM interface
    - Halt FSM – Load New Sequence – Start FSM



Conversion Sequence Length

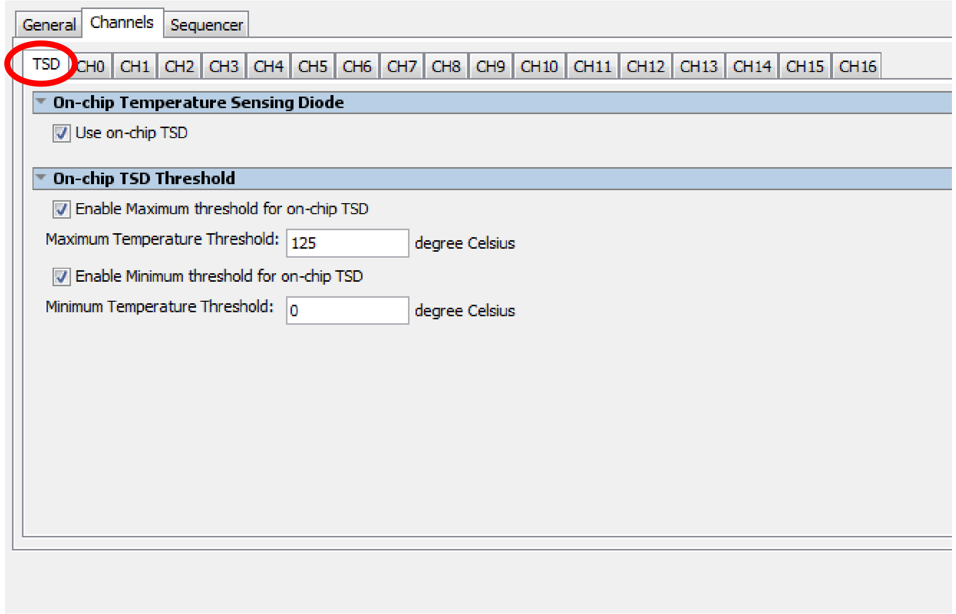
Number of slot used: 8

Conversion Sequence Channels

Slot 1 : CH 0
Slot 2 : CH 7
Slot 3 : NULL
Slot 4 : CH 1
Slot 5 : CH 1
Slot 6 : CH 0
Slot 7 : NULL
Slot 8 : NULL

MAX 10 FPGA - Internal Temperature Sensing Diode

- **Operating Range**
  - -40°C to +125°C
- **Conversion Speed**
  - 50Ksps
  - 8 clock cycles required for offset cancellation when switching between voltage & temperature mode
- **Threshold Detection IRQ**
  - Default values set in Megawizard
  - Reconfigurable via Avalon MM
- **Available in ADC1 only**



On-chip Temperature Sensing Diode

☑ Use on-chip TSD

On-chip TSD Threshold

☑ Enable Maximum threshold for on-chip TSD

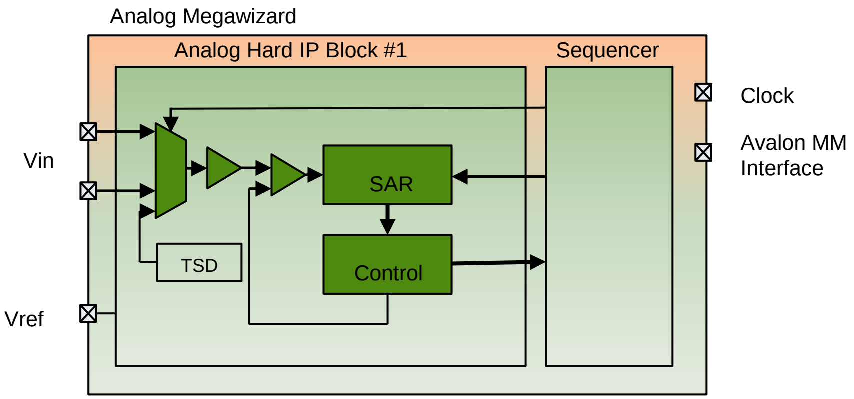
Maximum Temperature Threshold: 125 degree Celsius

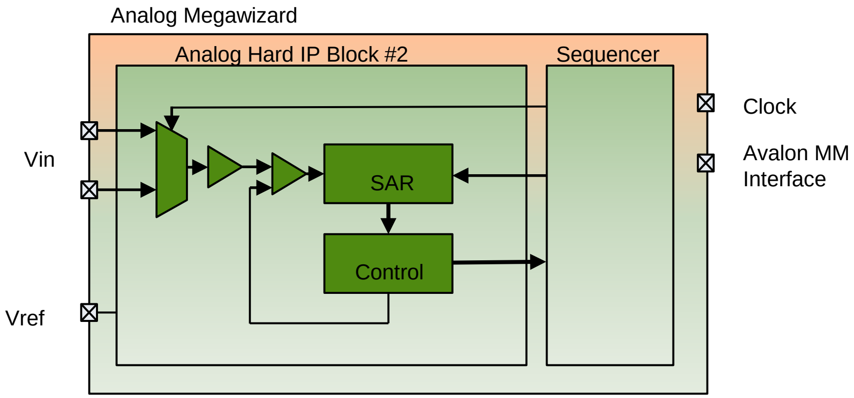
☑ Enable Minimum threshold for on-chip TSD

Minimum Temperature Threshold: 0 degree Celsius

MAX 10 FPGA - ADC Scenario # 1

- **With Quartus ACDS rev. 14.0**
  - Both ADC’s operate independently
  - Separate Sequencers
  - Vref Individually selectable





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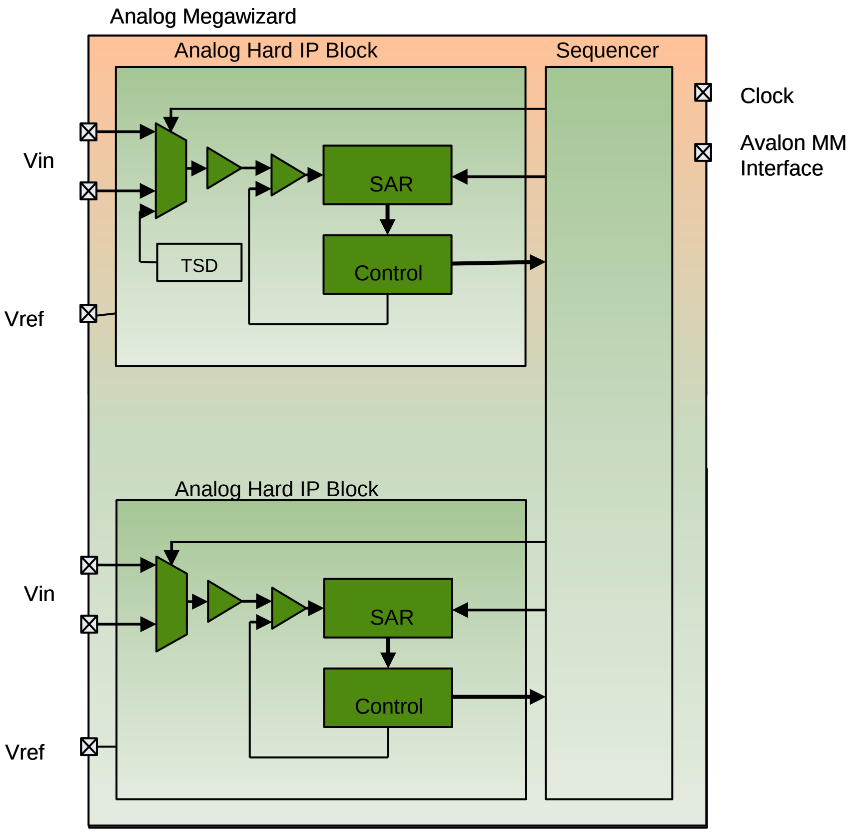
MAX 10 FPGA - ADC Scenario #2

- **With future release of Megawizard**
  - Dual Mode Operation
  - Both ADC's operate together under a Single Sequencer
  - Allows Simultaneous Sampling of analog input channels
  - Individual ADC Vref Selection
  - Common sample rate clk



[Click to return to Architectural Sections](#)

Design Software & IP

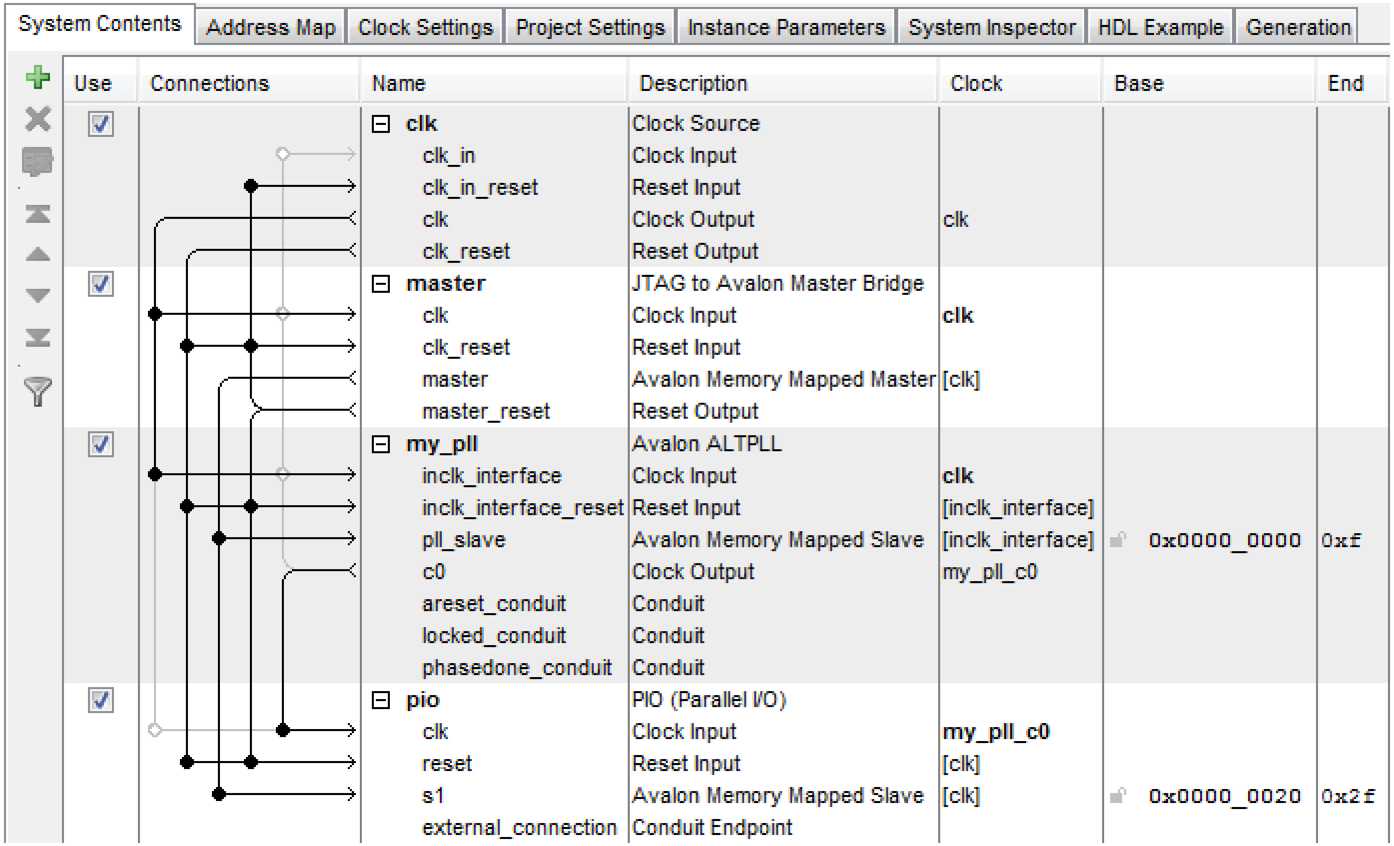
Software and IP Support

- **Quartus® II software**
  - Number one design software in performance and productivity
  - MAX 10 FPGA compilation & EPE support
    - Contact Altera for the latest support schedule
- **Includes Qsys system integration and DSP Builder for increased productivity**
  - DSP Builder + Advanced Block-set
- **Abundant IP & reference designs**

Quartus II Web Edition Software
No Cost License

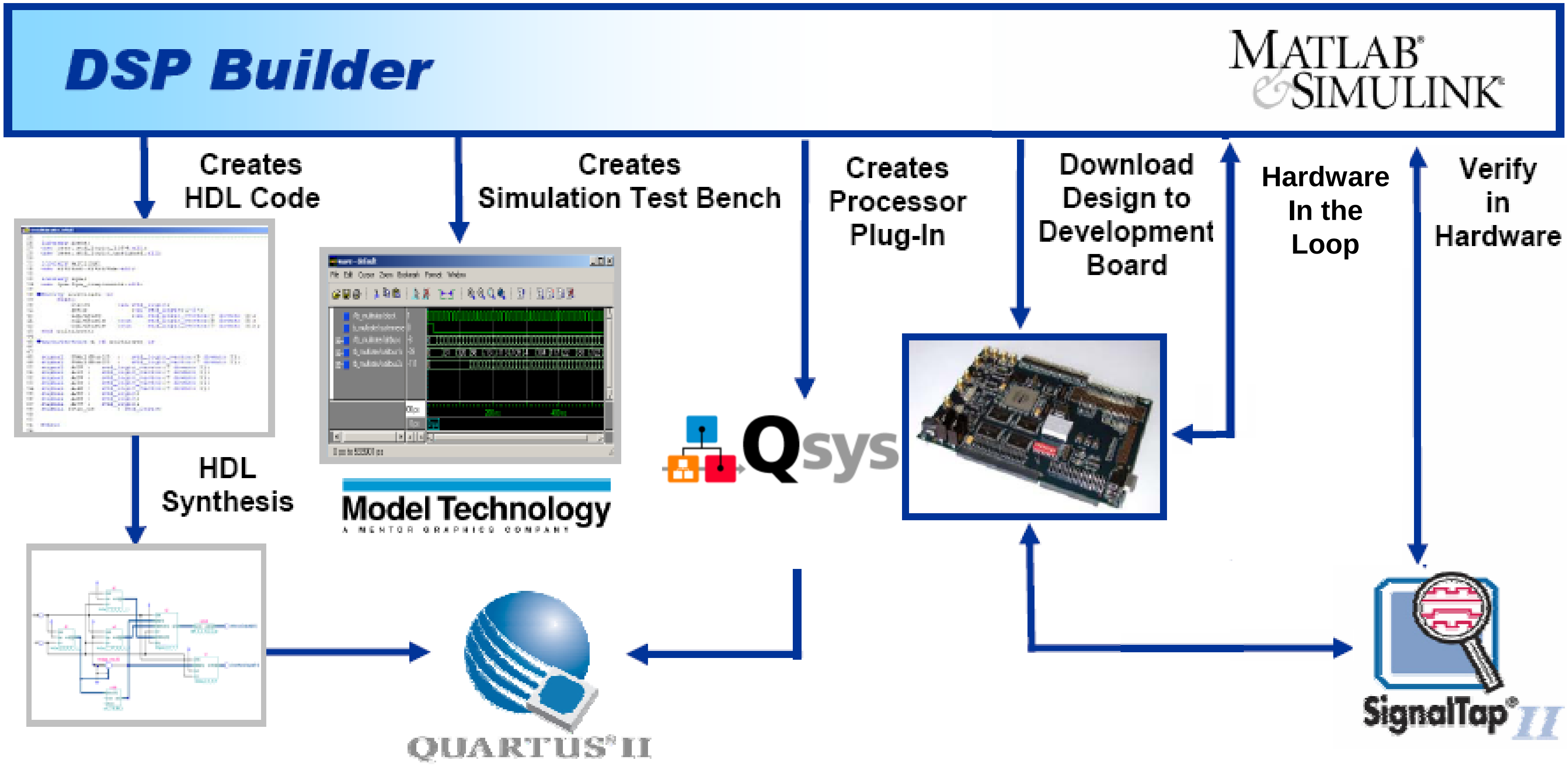
Qsys – Improving Designers *‘Productivity’*

“Drag & Drop” GUI



Use	Connections	Name	Description	Clock	Base	End
☑		⊟ **clk**	Clock Source			
		clk_in	Clock Input			
		clk_in_reset	Reset Input			
		clk	Clock Output	clk		
		clk_reset	Reset Output			
☑		⊟ **master**	JTAG to Avalon Master Bridge			
		clk	Clock Input	**clk**		
		clk_reset	Reset Input			
		master	Avalon Memory Mapped Master	[clk]		
		master_reset	Reset Output			
☑		⊟ **my_pll**	Avalon ALTPLL			
		inclk_interface	Clock Input	**clk**		
		inclk_interface_reset	Reset Input	[inclk_interface]		
		pll_slave	Avalon Memory Mapped Slave	[inclk_interface]	0x0000_0000	0xf
		c0	Clock Output	my_pll_c0		
		areset_conduit	Conduit			
		locked_conduit	Conduit			
		phasedone_conduit	Conduit			
☑		⊟ **pio**	PIO (Parallel I/O)			
		clk	Clock Input	**my_pll_c0**		
		reset	Reset Input	[clk]		
		s1	Avalon Memory Mapped Slave	[clk]	0x0000_0020	0x2f
		external_connection	Conduit Endpoint			

DSP Builder Flow – Support for MAX 10 FPGA



DSP Builder

MATLAB & SIMULINK

Creates HDL Code

Creates Simulation Test Bench

Creates Processor Plug-In

Download Design to Development Board

Hardware In the Loop

Verify in Hardware

HDL Synthesis

Seamless Integration with Qsys + DSP Builder (including folding)

'Most Requested' Customer IP (Alphabetically Listed)

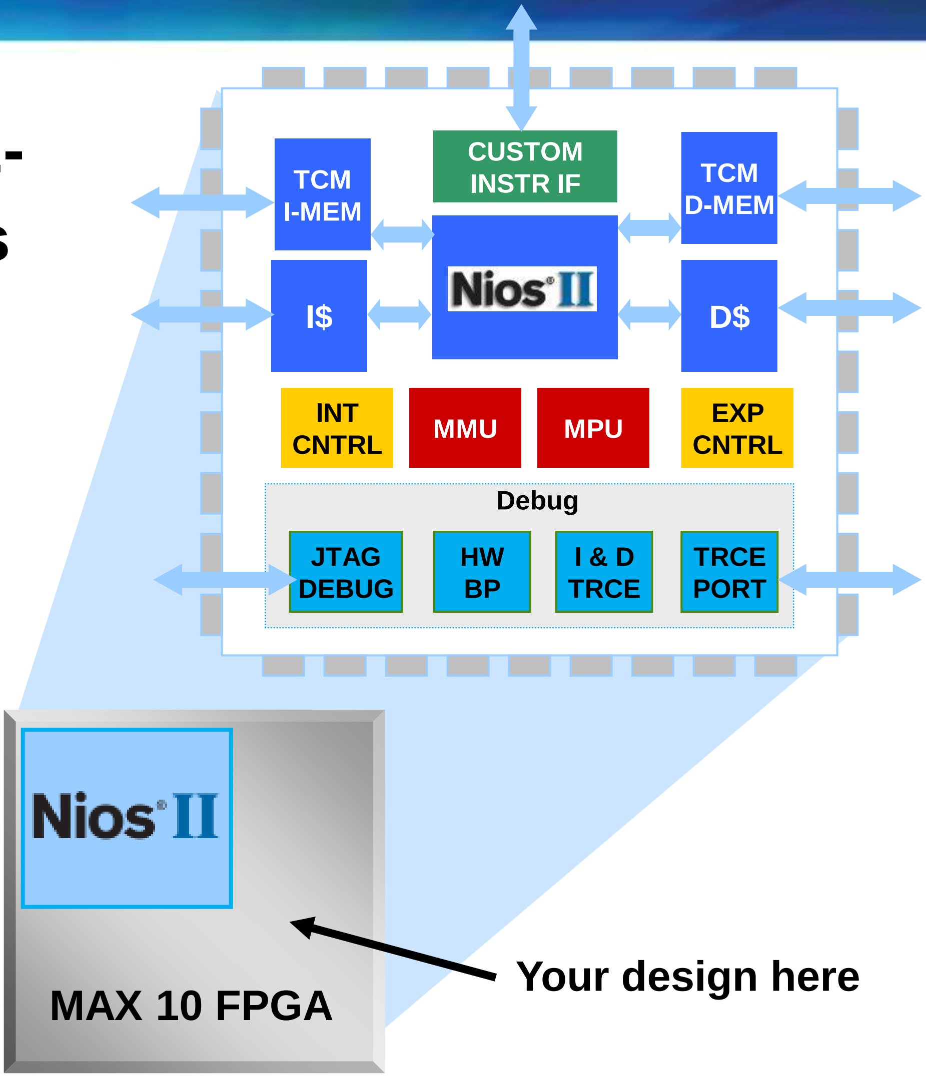
IP core	Altera	Partner
CAN	-	✓
Ethernet	✓	✓
FlexRay	-	✓
FPDLink	-	✓
MIPI	-	✓
MOST	-	✓
Nios® II 32-bit processor	✓	-
PCI 32/64-bit	-	✓
USB 2.0	-	✓
Video Image Processing (VIP) Suite	✓	-

What IP do you need?

MEASURABLE ADVANTAGE™

Nios® II Processor Overview

- **Family of configurable 32-bit embedded processors**
- **Soft IP core, royalty free license**
- **Over 32,000 licensees world wide**

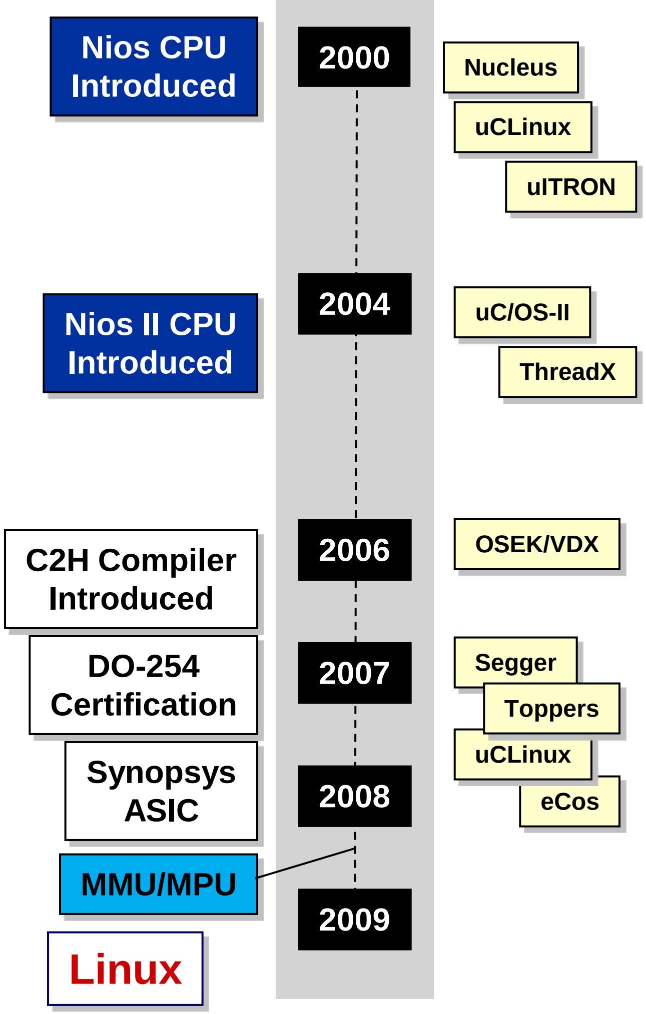


Your design here

http://www.altera.com/devices/processor/nios2/ni2-index.html

Nios® II Processor Adoption

- **Industry's #1 Soft Core CPU** – Gartner Dataquest
- **Used by each of Altera's top 20 OEMs**
- **Vibrant Nios Forum community (over 16,000)**
- **Used by developers in all Altera markets**



Nios CPU Introduced

2000

Nucleus

uCLinux

uITRON

Nios II CPU Introduced

2004

uC/OS-II

ThreadX

C2H Compiler Introduced

2006

OSEK/VDX

DO-254 Certification

2007

Segger

Toppers

uCLinux

Synopsys ASIC

2008

eCos

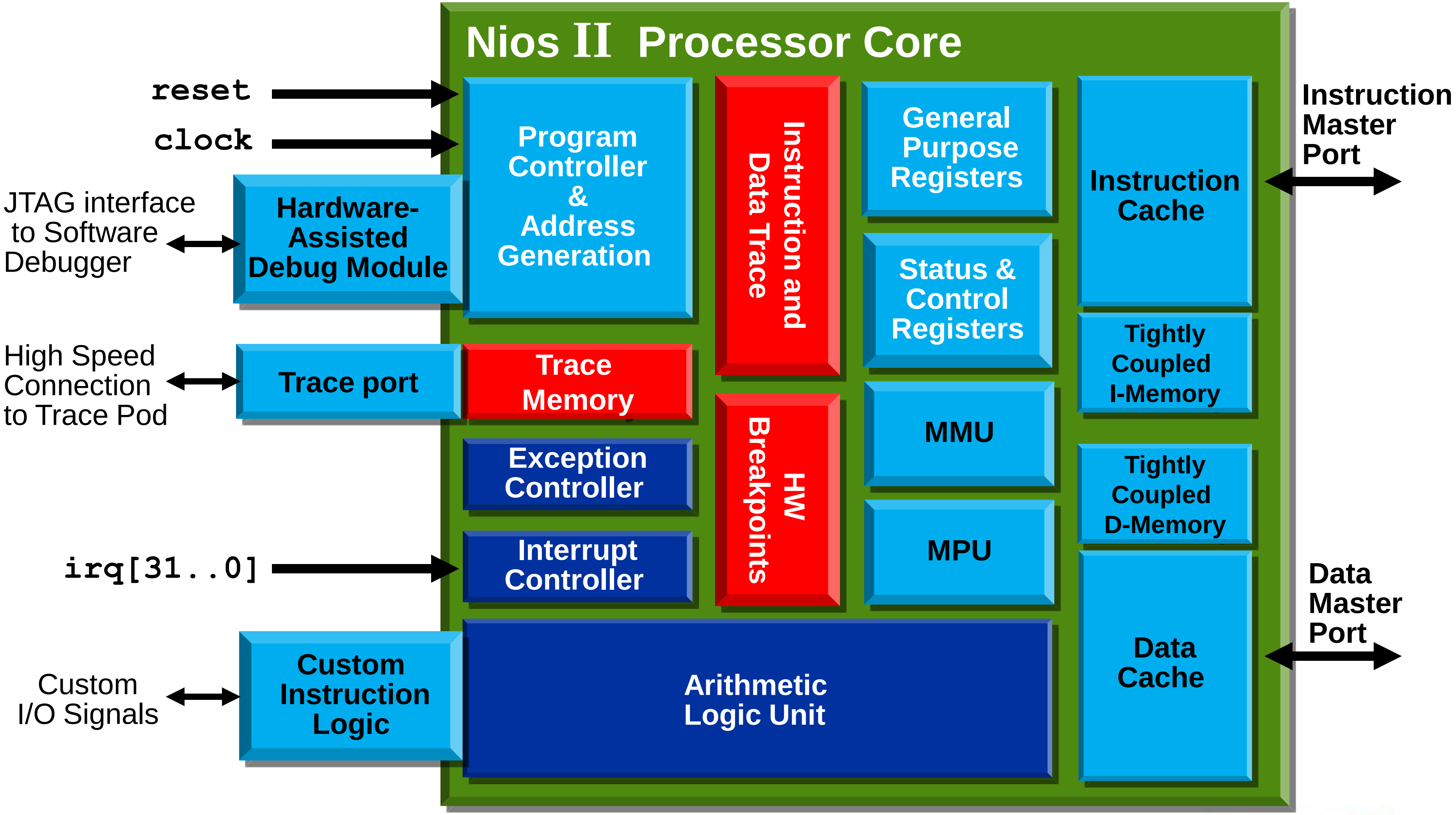
MMU/MPU

2009

Linux

Nios® II Processor Options

http://www.altera.com/devices/processor/nios2/ni2-index.html



Nios II Processor Core

reset

clock

JTAG interface to Software Debugger

Hardware-Assisted Debug Module

High Speed Connection to Trace Pod

Trace port

irq[31..0]

Custom I/O Signals

Custom Instruction Logic

Program Controller & Address Generation

Trace Memory

Exception Controller

Interrupt Controller

Instruction and Data Trace

HW Breakpoints

General Purpose Registers

Status & Control Registers

MMU

MPU

Arithmetic Logic Unit

Instruction Cache

Tightly Coupled I-Memory

Tightly Coupled D-Memory

Data Cache

Instruction Master Port

Data Master Port

A = Optional

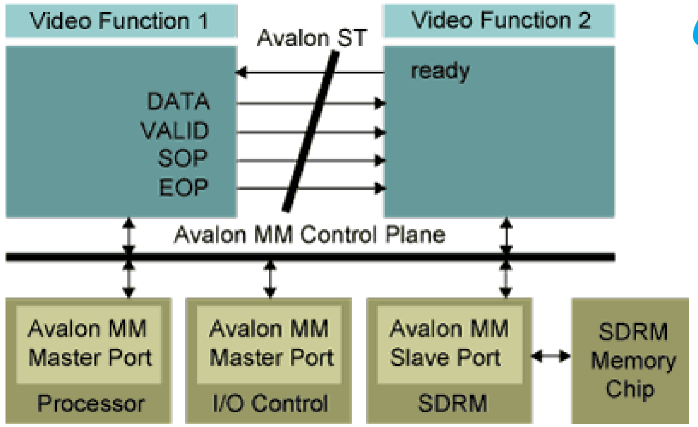
A = Fixed

🟦 = Configurable

🟥 = Debug Options

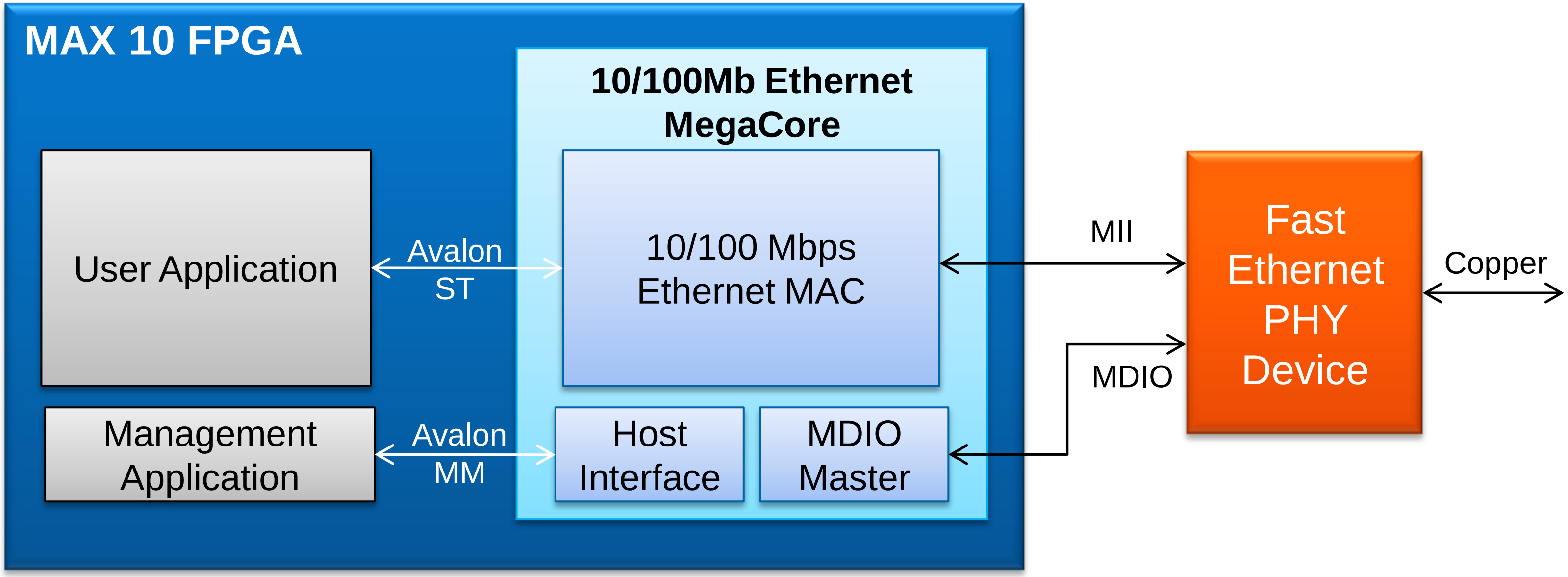
Video Image Processing (VIP) Suite

- **BT 656 ↓ Avalon ST video**
- Scaler
- Scaler II
- Deinterlacer
- Deinterlacer II
- Chroma resampler
- Color plane sequencer
- Frame buffer
- Image clipper
- Gamma correction
- Alpha blending mixer
- 2D FIR filter
- 2D median filter
- Color space converter
- Test pattern generator
- Switch
- Control Sync
- Frame Reader
- **Avalon ST video ↓ BT 656**



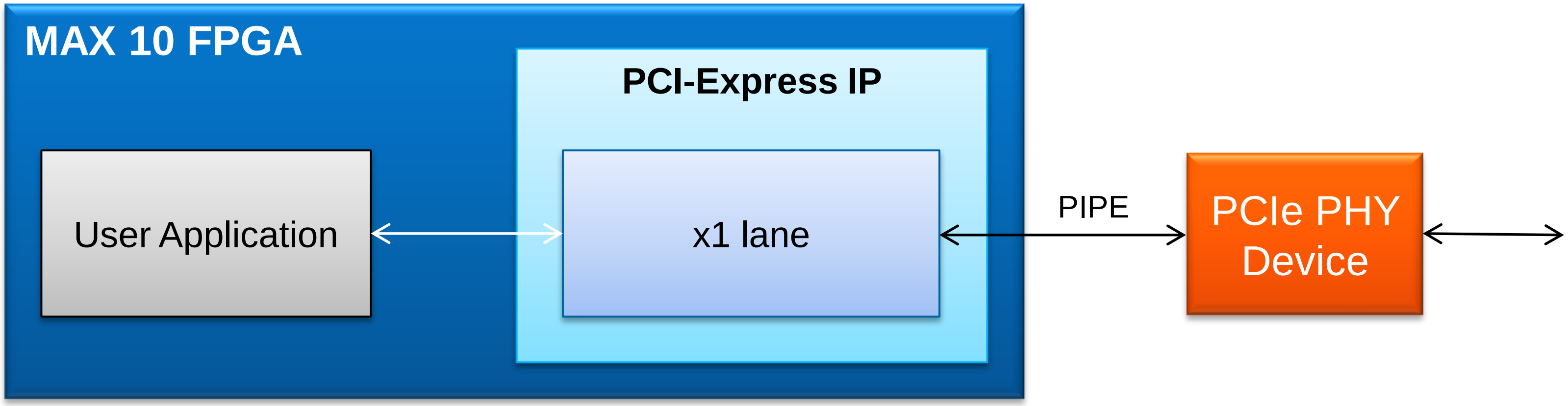
Open Interface Protocol

Ethernet Network Connectivity



- **10/100Mb Ethernet**
  - Media Independent Interface (MII)
  - Avalon Streaming 8-bit client side interface
  - IEEE 1588 precise time protocol for clock synchronization

PCI-Express Connectivity


MAX 10 FPGA

PCI-Express IP

User Application

x1 lane

PIPE

PCIe PHY Device

- **PCI-Express IP**
  - IP from Partner
  - Ref. design and h/w demo needs lead customer
    - port from Cyclone II (see picture)

☞ Click to return to Architectural Sections

Development tools

MAX® 10 FPGA Kits Portfolio Summary

Altera Kits	FPGA	Purpose	~Price	FGI Target
MAX 10 FPGA Development Kit	10M50	High density development with DDR3 and ADC evaluation	**$199**	**Q1 2015**
MAX 10 FPGA Evaluation Kits	10M02 WLCSP	Ultra low cost logic, power, and I/O evaluation with several density and package options	**$29**	**Q1 2015**
	10M02		**$49**	**Q1 2015**
	10M08		**$49.95**	**Sept 2014**
	10M50		**$69**	**Q1 2015**
NEEK 10 (Nios® Embedded Evaluation Kit)	10M50	Nios II evaluation with multi-touch display and extended peripherals	**$299**	**Q2 2015**
Stratix® 10 Development Kits	Various	Update System Controller from MAX V to MAX 10	**N/A**	**-**
Partner Solutions				
Various 3rd parties	10M08 – 10M50	Evaluation, development, or demo boards + ref. designs	**As low as $30**	**Sept 2014 – 1H 2015**

A Rich Extensive Portfolio!

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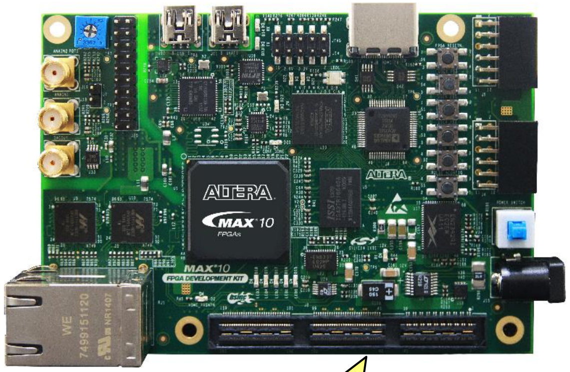
Altera MAX® 10 FPGA Kits Portfolio Plan

~$29 - $69

MAX 10 FPGA Evaluation Kits

- Ultra Low Cost Eval
- Logic, I/O, power eval
- Arduino
- 4 package/density options to choose



~$199

MAX 10 FPGA Development Kit

- High Density Development
- Ref Design Platform
- 300 MHz DDR3
- ADC Evaluation (SMAs)
- HDMI TX, HSMC

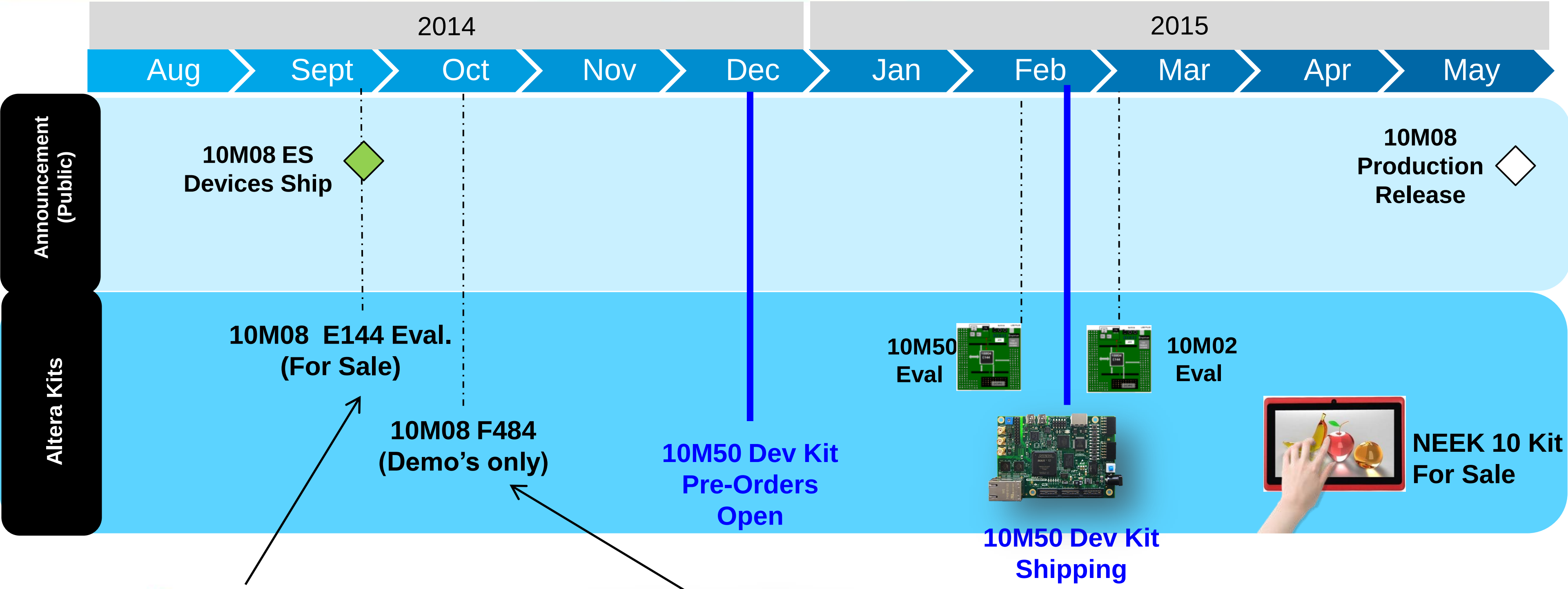
~$299

Altera NEEK 10 Kit

- MAX 10 NEEK Evolution
- Daughter to MAX 10 Dev Kit
- Large multi-touch screen
- Sensors, accelerometers, wireless
- Port CIII NEEK Applications

All Kits Feature Enpirion Power Solutions

Altera’s MAX® 10 FPGA Kit Portfolio Rollout



10M08 ES Devices Ship

10M08 Production Release

10M08 E144 Eval. (For Sale)

10M08 F484 (Demo’s only)

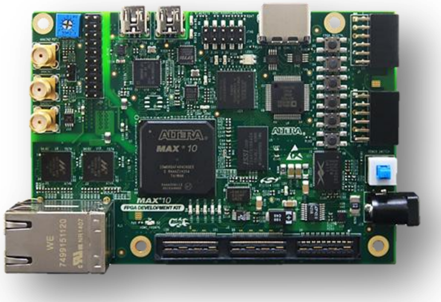
10M50 Dev Kit Pre-Orders Open

10M50 Eval

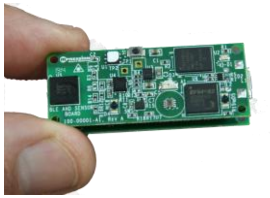
10M02 Eval

10M50 Dev Kit Shipping

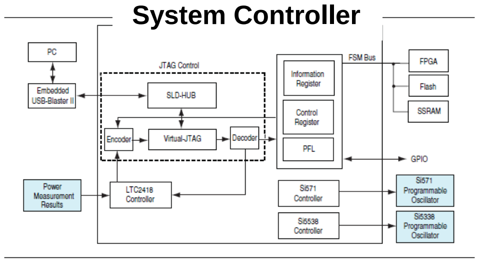
NEEK 10 Kit For Sale



Partner Solutions & Other Generation 10 Usage



Kit, IP, DSN Partners



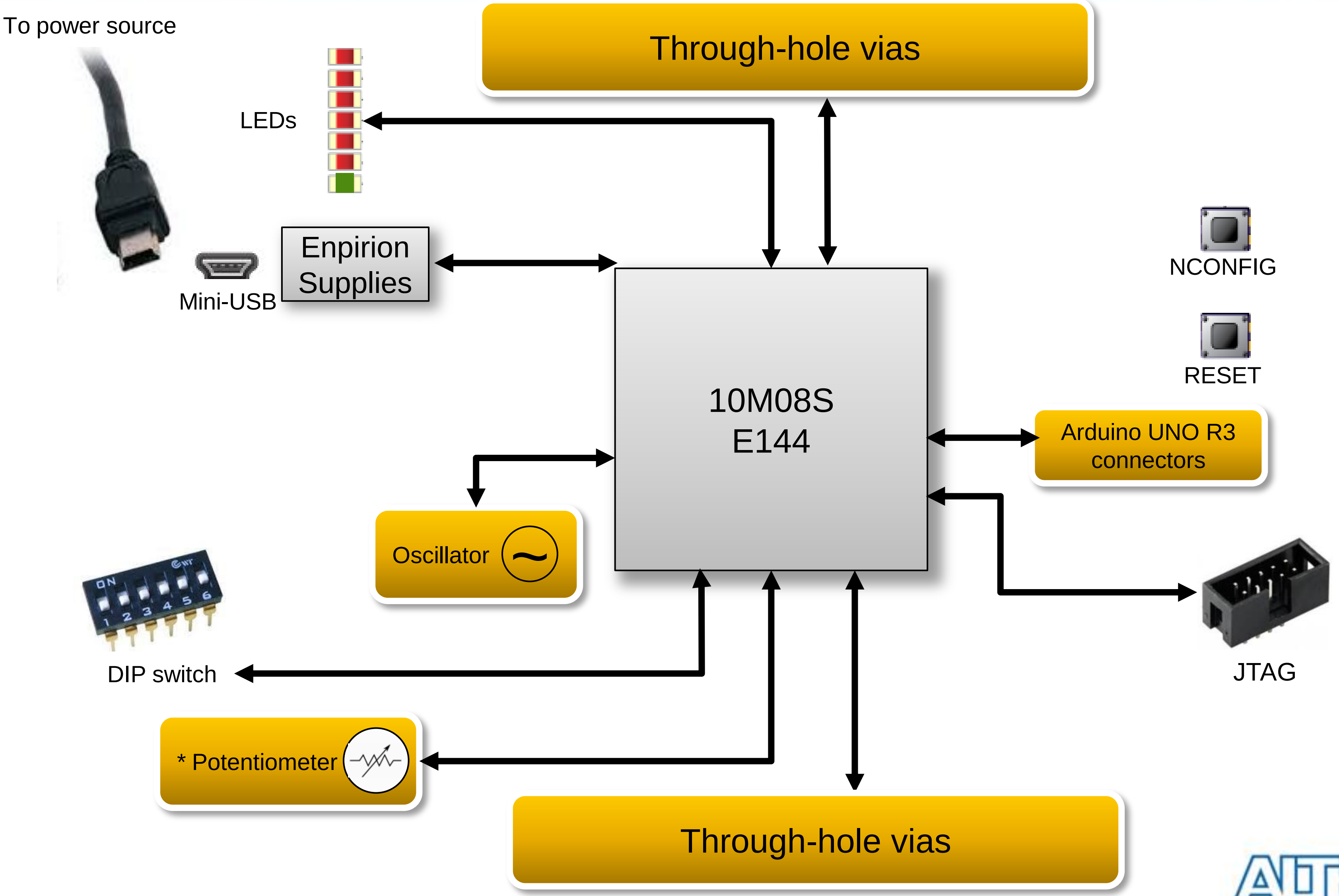
- Contact Distributors for MAX® 10 Kit details (distributor designed)
- Ecosystem partners in planning or R&D
- MAX 10 controller for Stratix® 10 FPGA Kits

1 MAX® 10 FPGA - Evaluation Kit, Feature List

- **Target Sub-segments**
  - Broad-base customers
- **FPGA**
  - 10M02D, 36-pin WLCSP (27 I/O)
  - 10M02S, E144 (101 I/O)
  - 10M08S, E144 (101 I/O)
  - 10M50S, E144 (101 I/O)
- **Standard Kit Features**
  - Manual power Measurement using resistor jumpers
  - Powered from USB cable, **Enpirion** Power Supplies
  - Crystal OSC (non-programmable)
  - JTAG pin header
  - Buttons, LEDs, Switches
  - 80 I/O through-holes
  - **Download cable NOT included**
- **Memory Interfaces**
  - None
- **Display**
  - None
- **Components and Interfaces**
  - Arduino UNO R3 connector
  - Potentiometer footprint

P/N: **EK-10M08E144ES/P (Open)**
Price: ***$49.95 resale***
Available: ***Sept 2014***

1 MAX® 10 FPGA - Evaluation Kits, Block Diagram



To power source

LEDs

Through-hole vias

Mini-USB

Enpirion Supplies

10M08S E144

NCONFIG

RESET

Arduino UNO R3 connectors

Oscillator

JTAG

DIP switch

* Potentiometer

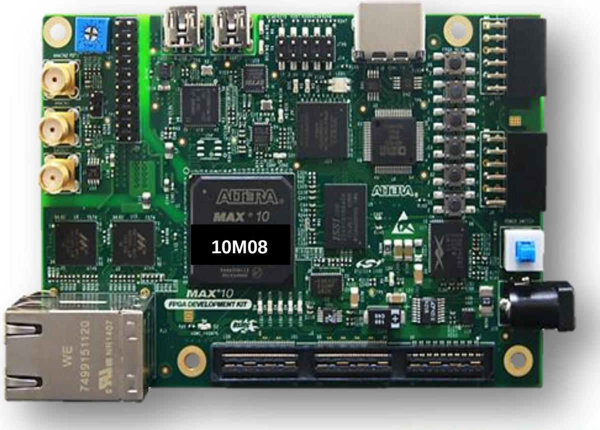
Through-hole vias

Customer must purchase and install.

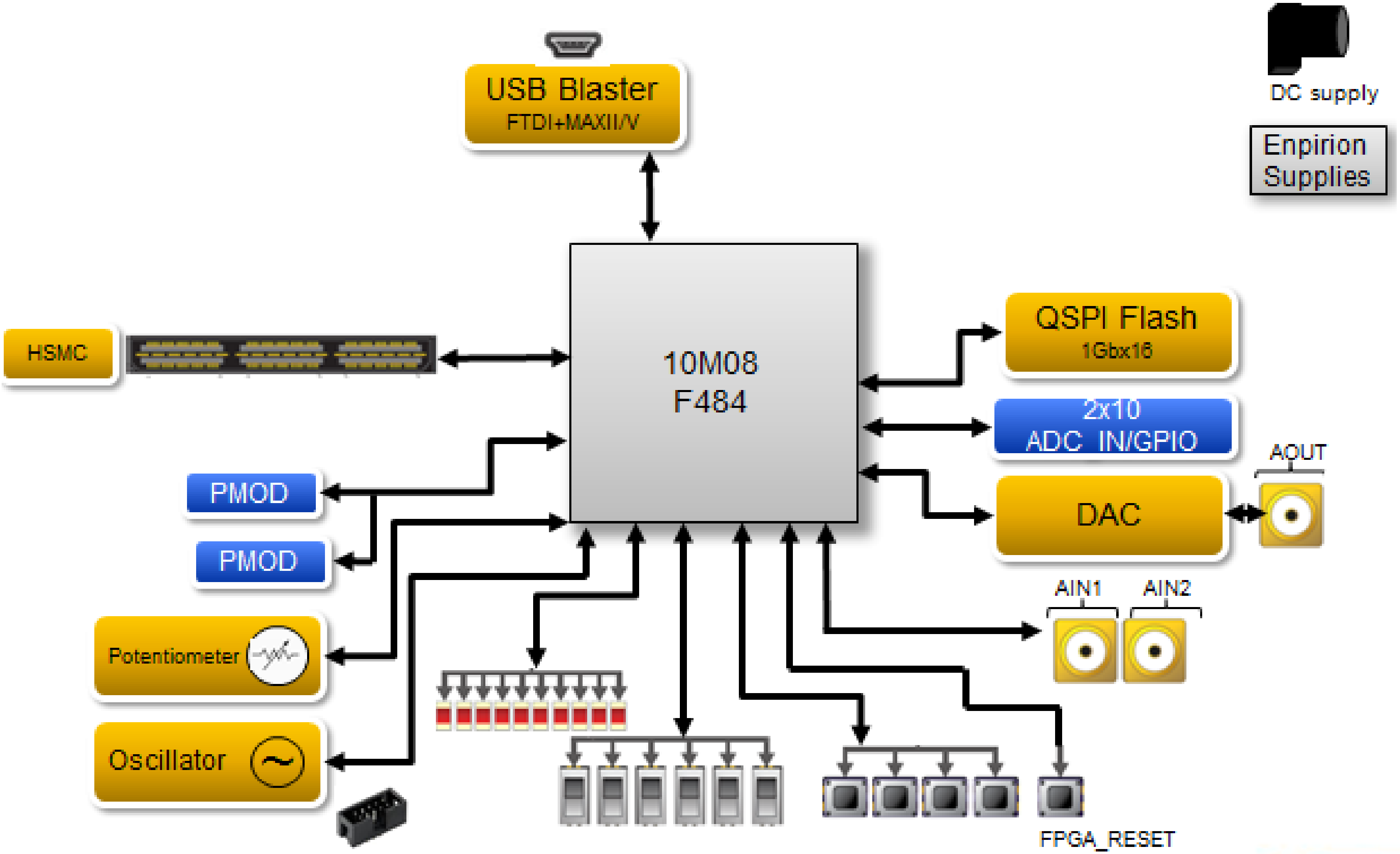
2 MAX® 10 FPGA – 10M08 Demo Board, Feature List

- **Target segments**
  - General customer demos
- **FPGA**
  - F484 Package
  - 10M08 (8K LEs, 250 I/Os)
  - D (dual supply) device
- **Standard Kit Features**
  - QSPI Flash
  - Power Measurement on all FPGA supplies
  - 12V Supply, **Enpirion** Power Supplies
  - Programmable Oscillators
  - Mini-USB on-board Blaster
  - JTAG pin header
  - Programmable clock OSC
- **Memory Interfaces**
  - None
- **Display**
  - None
- **Components and Interfaces**
  - HSMC connector
  - 4 SMAs (AIN, VREF, CLK, AOUT)
  - DAC
  - Potentiometer
  - 2x PMOD connector

P/N:	**Not Orderable**
Allotment:	***160 for WW FAE Org***
Available:	***October 2014***



2 MAX® 10 FPGA – 10M08 Demo Board, Block Diagram

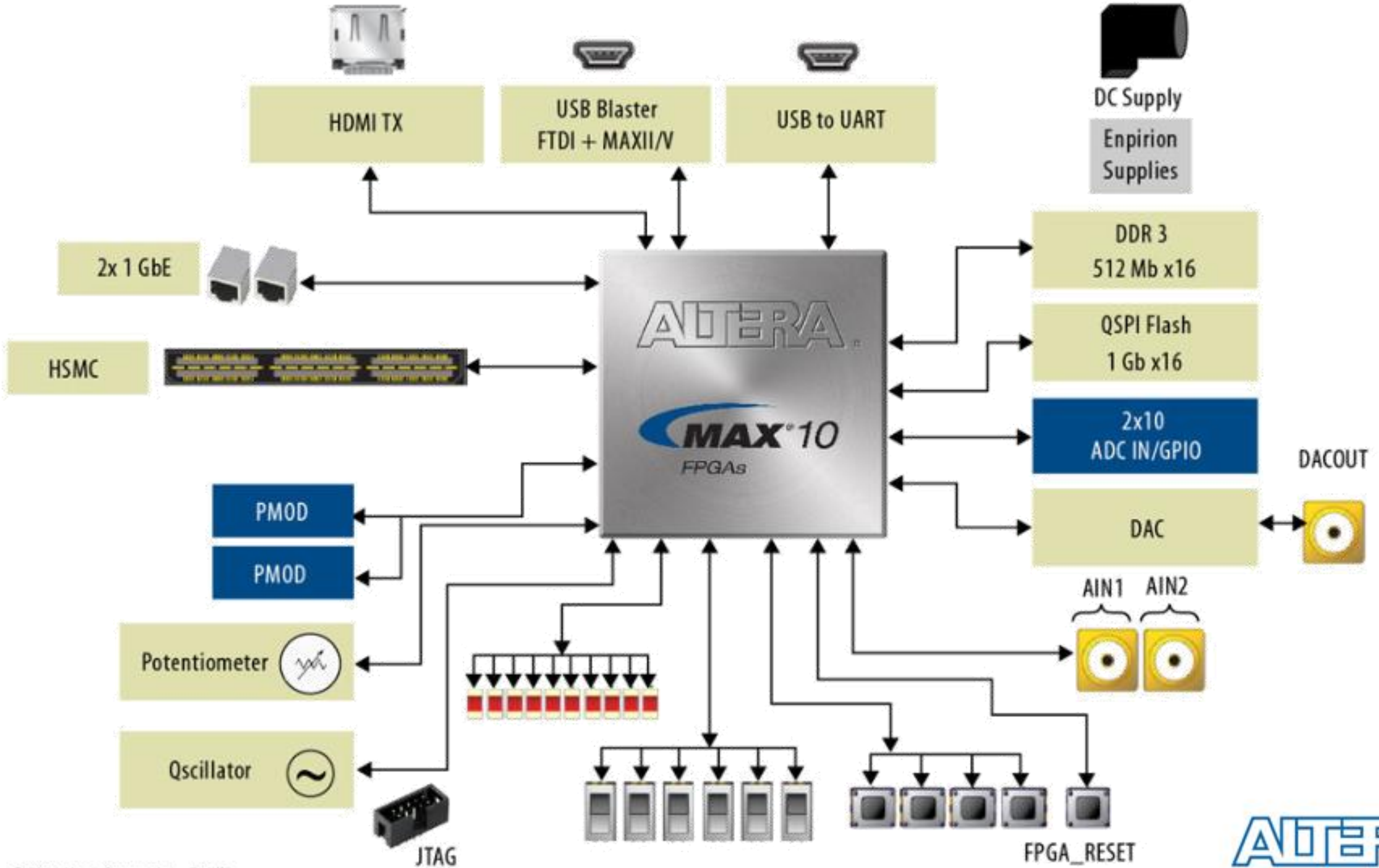


3 MAX® 10 FPGA - Development Kit, Feature List

- **Target segments**
  - General customer evaluation
  - motor control, ind Ethernet, smart grid
  - Auto infotainment, e-vehicle, ADAS
  - Comms/Comp/Storage Chassis management
- **FPGA**
  - F484 Package
  - 10M50 (50K LEs, 360 I/Os)
  - D (dual supply) device
- **Standard Kit Features**
  - QSPI Flash
  - Power Measurement on all FPGA supplies
  - 12V Supply, **Enpirion** Power Supplies
  - Programmable Oscillators
  - On-board Blaster
  - JTAG pin header
- **Memory Interfaces**
  - DDR3 x16 with ECC @ 300 MHz
- **Display**
  - HDMI out
- **Components and Interfaces**
  - HSMC connector
  - 2x Marvel 88E1111 Ethernet PHYs (MII & RGMII interfaces)
  - USB2.0 UART
  - 4 SMAs (AIN, VREF, CLK, AOUT)
  - DAC
  - Potentionmeter
  - 2x PMOD connector
  - Programmable OSC

P/N:	**DK-DEV-10M50-A**
Price:	***TBD (~$199 Target)***
Pre-ordering:	***December 2014***
Available:	***Q1 2015***

3 MAX® 10 FPGA - Development Kit, Block Diagram



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4 MAX® 10 FPGA - NEEK 10, Objectives

- **Capture Nios® II users with new Generation 10 NEEK**
  - FPGA microcontroller, ADC, accelerometers, etc.

- **MAX FPGA Development Kit base board + NEEK add-on**
  - Develop new demos & port existing NEEK S/W demos
- **Requirements for NEEK 10 add-on being gathered**
  - 7 inch LCD capacitive touch screen
  - Sensors (orientation, accelerometers)
  - Audio in/out
  - Bluetooth and/or WiFi module

P/N: **TBD**
Price: ***TBD (~$299 Target)***
Pre-ordering: ***Q1 2015***

Thank You!

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Uniquest Corporation
Uniquest b/d, 271-2 Seohyun-dong
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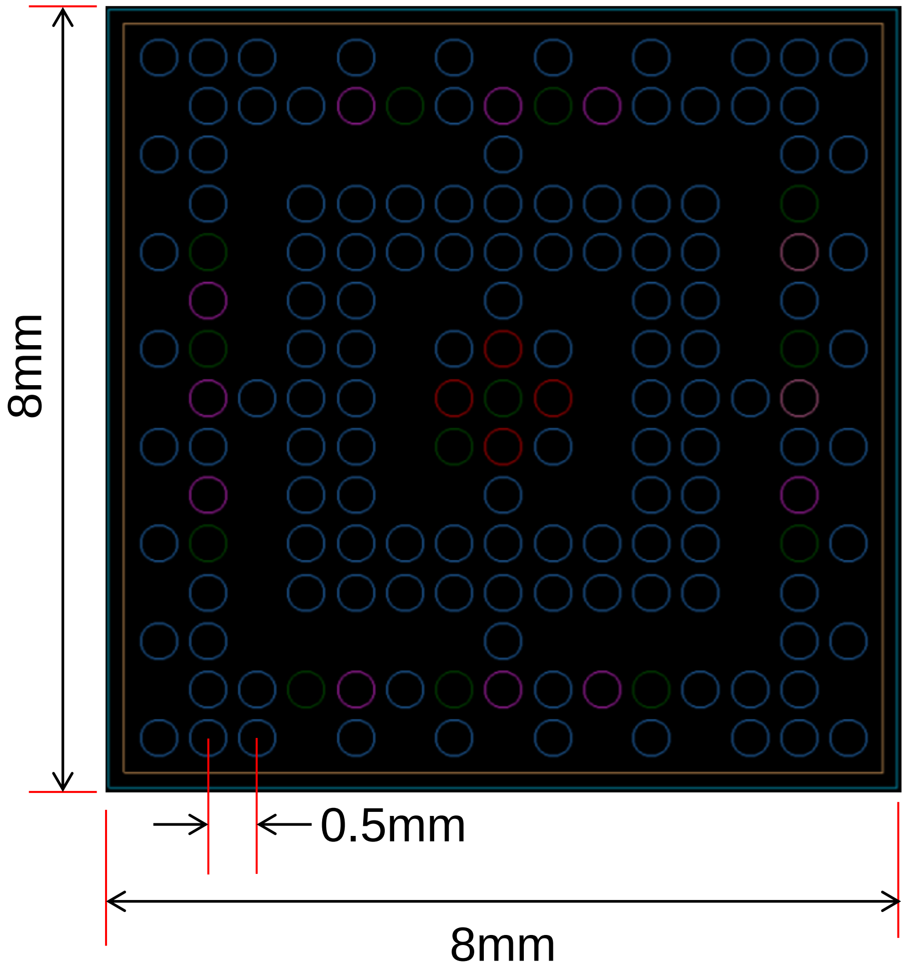
Fax: +82-31-776-9887
contact@axios.co.kr
http://www.uniquest.co.kr

MEASURABLE ADVANTAGE™

Appendix

MAX 10 FPGA M153 Package – "Easy PCB" Footprint



Intentionally created gaps in ball grid array to allow space for PCB traces and/or through-hole via's.

Goal: **"Easy" PCB board design**

1. Use 0.8mm pitch design rules instead of 0.5mm rules.
    - 2 layer signal breakout (SMD on both component and PCB)
    - 3 mil line/space
    - 16 mil PTH
    - Shared P/G PTH
2. Avoiding use of blind or buried via's.
3. Minimize the number of PCB layers needed to route to all device pins.

Note: Altera recommended PCB layout (preliminary) in 4Q 2013