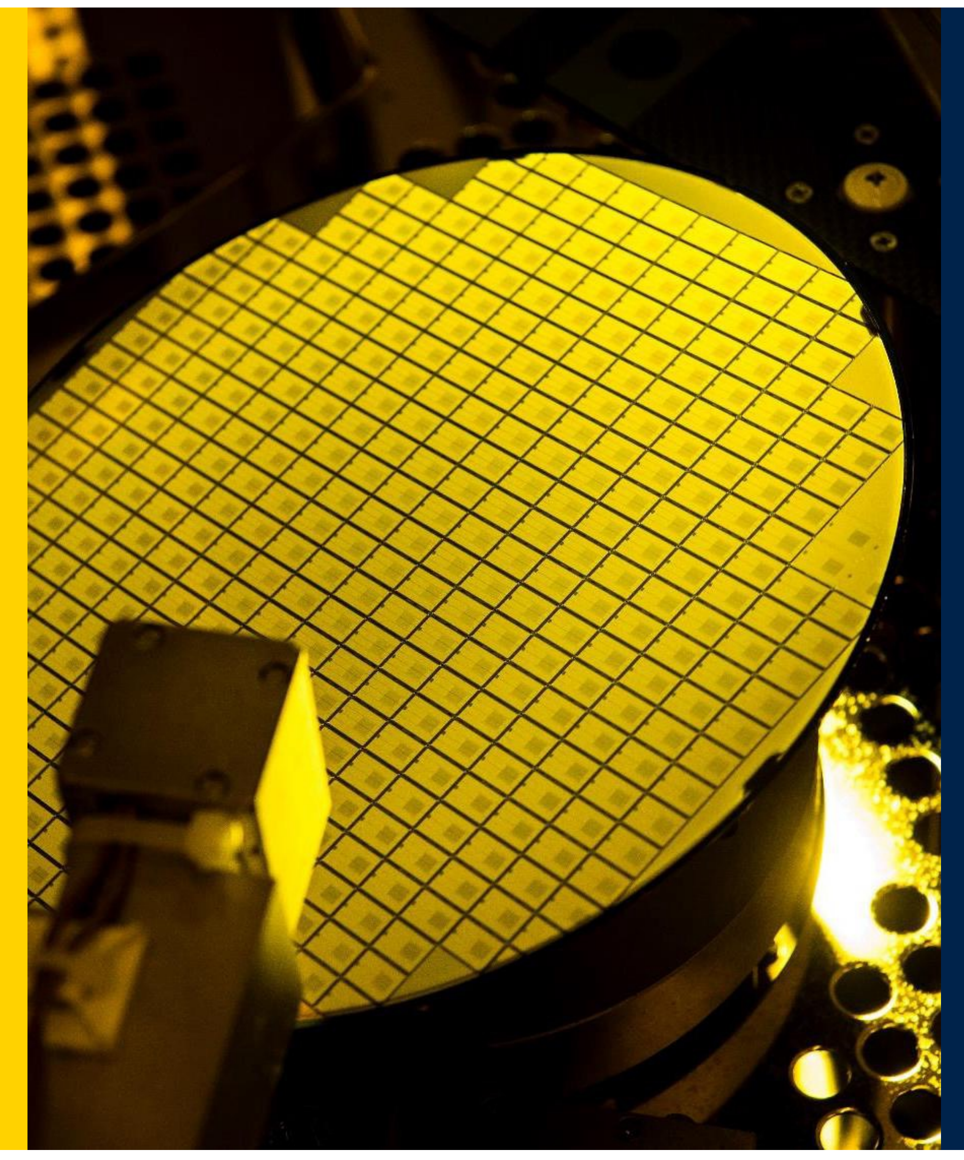


ST SiC MOSFET: the breakthrough technology to boost power electronics performance

STMicroelectronics
정지윤 매니저

Agenda

1 SiC MOSFET technology overview

2 ST Gen4 SiC introduction

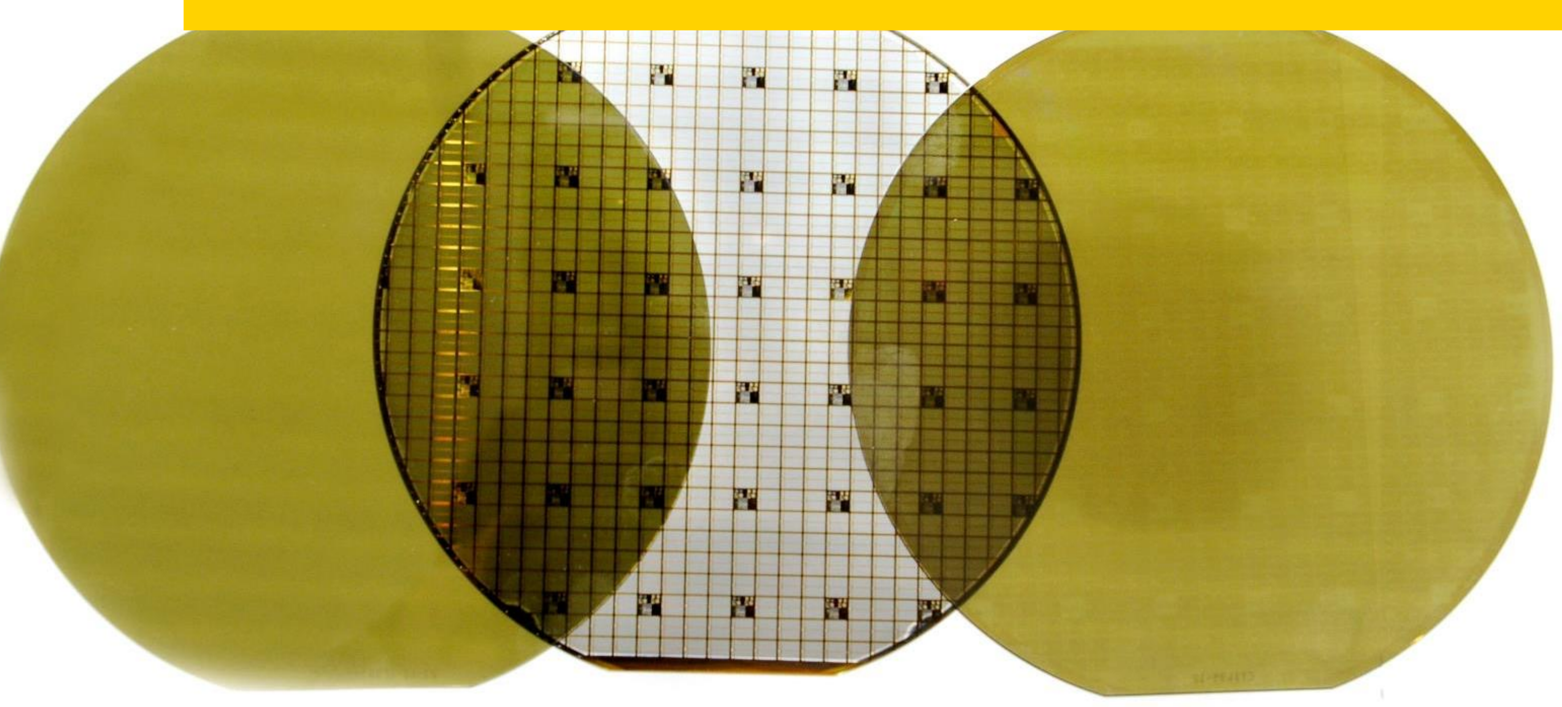
3 Gen4 vs. Gen3 & peers

4 ST SiC package technologies

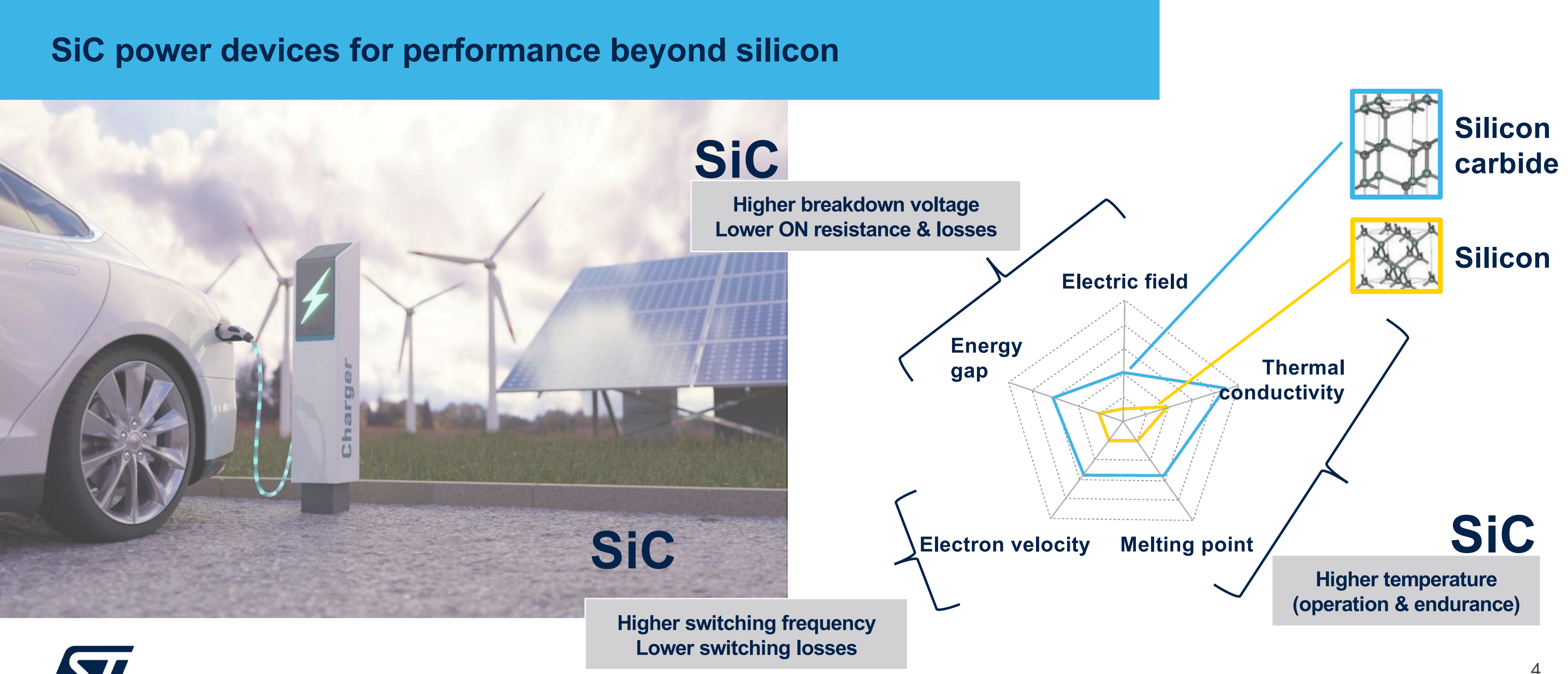
5 ST power modules

6 Q&A

SiC MOSFET technology overview



Why silicon carbide?



Power semiconductors for key applications

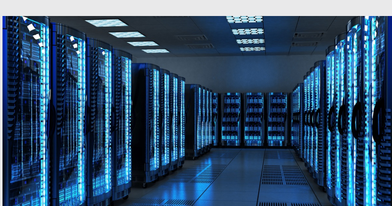
The SiC MOSFET is the best technology so far for high-voltage, high-frequency and high-power system applications

P_{OUT} (W)
100k
10k
1k

Si IGBT
Si MOSFET
Silicon Carbide
GaN
Traction Inverter
DC-DC Converter
Power Supply
OBC
Power supply & DC-DC Converter

1k
10k
100k
1M
f_{SW} (Hz)

Major trends driving the adoption of SiC

	Automotive	Industrial		
What?	Electric vehicle	Charging station	Renewable energy	 Power supplies
Where?	• On-board chargers, • DC-DC converters, • Traction inverters, • E-compressor.	• Industrial chargers, • EV DC fast chargers, • EV wireless chargers.	• Solar inverters • Energy storage systems • Wind power.	• AC-DC server power supplies (focus on AI) • Telecom AC-DC rectifiers • UPS
Why?	Small size & weight, high efficiency, longer driving range.	High efficiency, lower cost, optimal thermal management	Higher efficiency, lower system cost.	Higher efficiency, higher power density, lower energy bills.

ST Gen4 Silicon Carbide introduction

ST SiC vertical integration approach

Norrköping

Substrate manufacturing
- 150 mm volume production
- 200 mm with industrial quality and yields

Singapore

Front-end manufacturing
150 mm SIC diodes and MOSFET production on 150 mm wafers

Shenzhen

Back-end assembly & test
Advanced power packages and modules

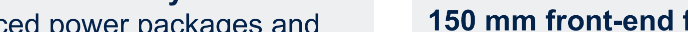
Chongqing

Front-end manufacturing
(under construction, start operation in Q4/25)

Catania

ST Silicon Carbide Campus
Vertically integrated silicon carbide facility
- Substrate manufacturing (Operational)
- 200 mm front-end manufacturing (under construction, start operation in Q4/25)
- Back-end assembly and test (under construction)

150 mm front-end fab
- Front-end manufacturing of SiC devices on 150 mm wafers

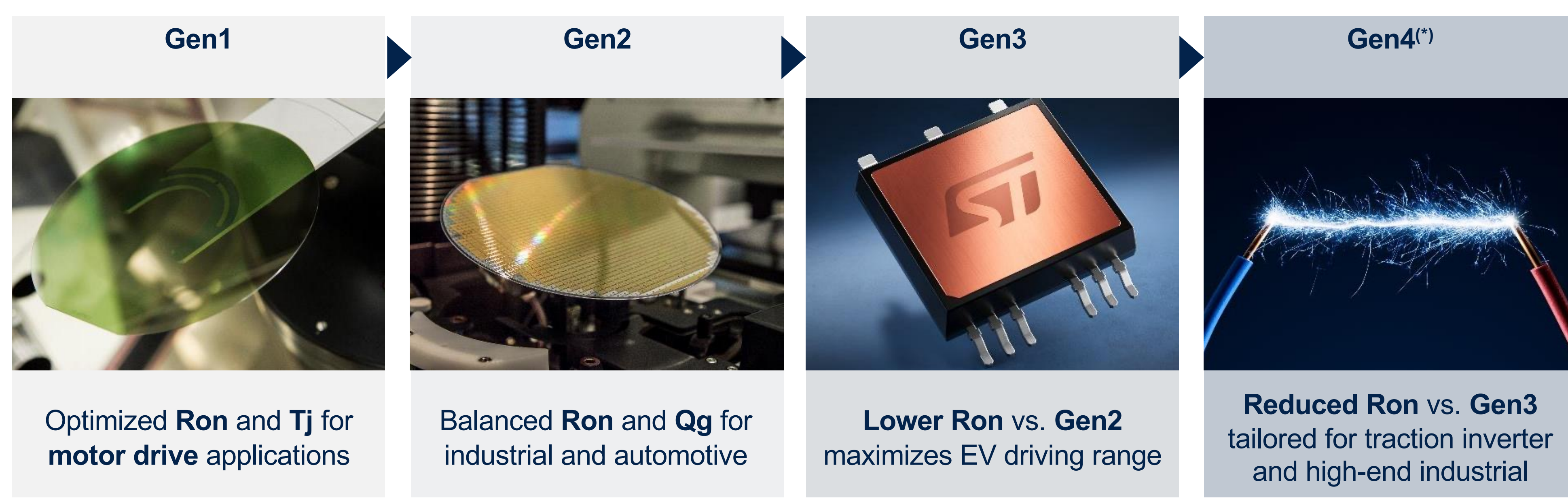


Bouskoura

Back-end assembly & test
Advanced power packages and modules

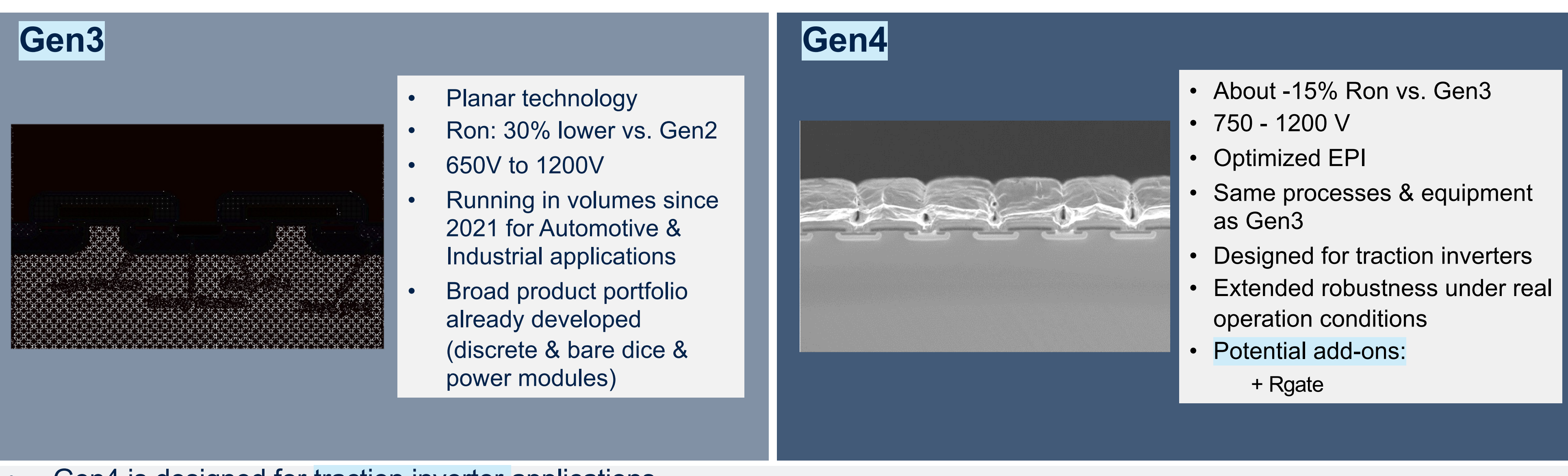
Pioneering Silicon Carbide development for over 25 years

A story of ongoing evolution that continues with the ramping up of fourth generation SiC MOSFET technology

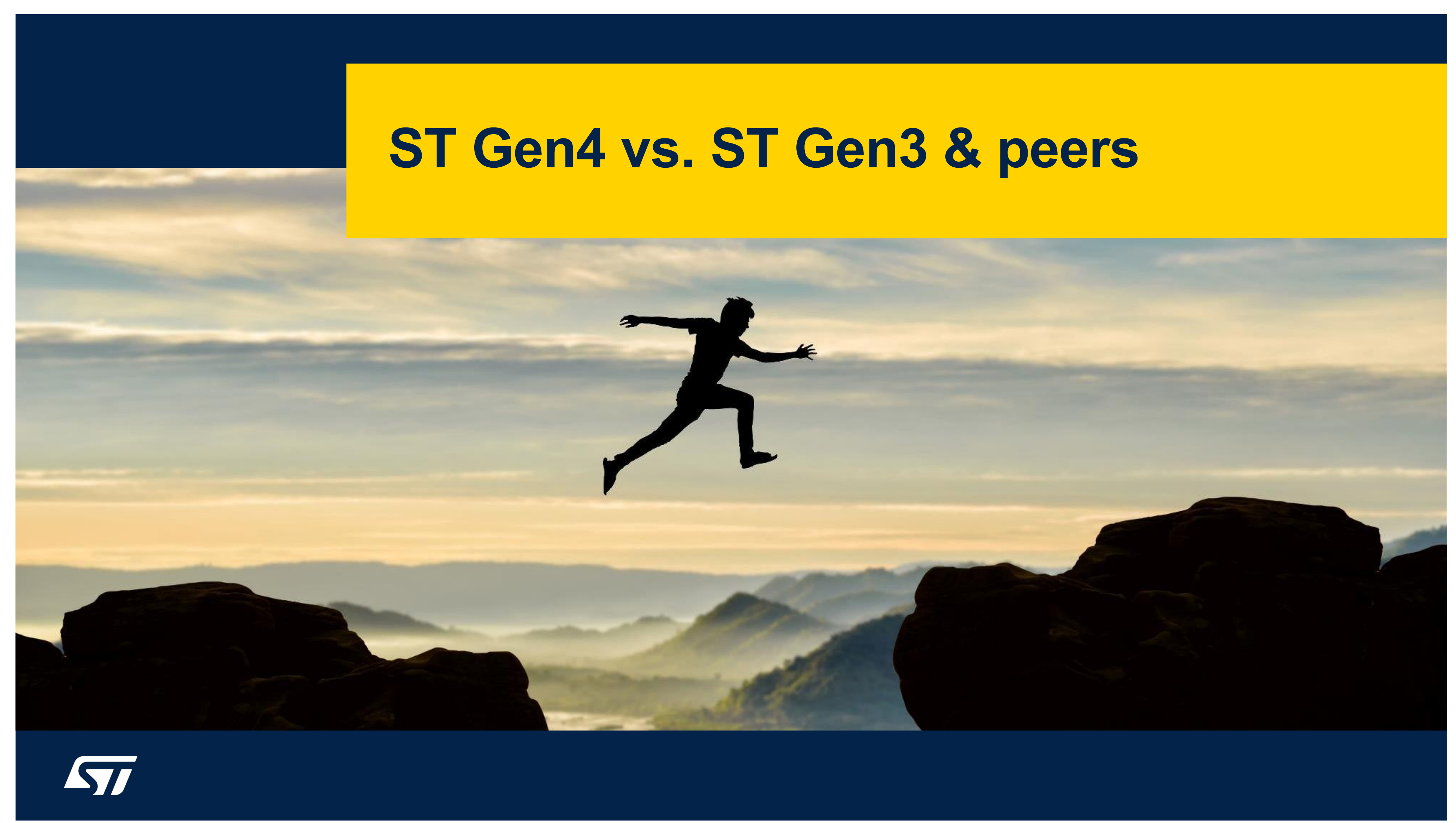


(*)750V in production, 1200V coming soon

SiC technology evolution



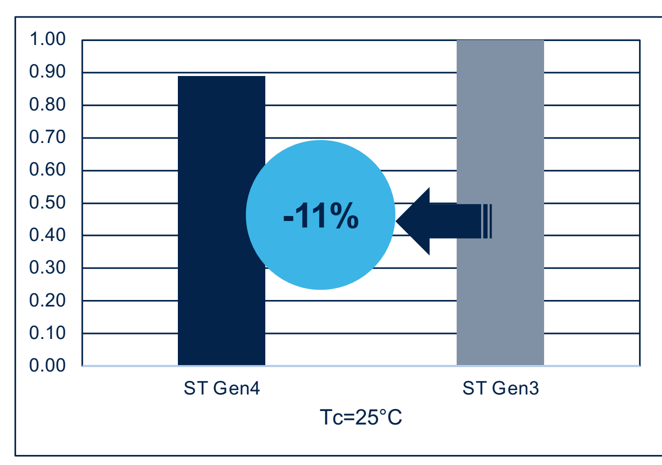
- Gen4 is designed for traction inverter applications
- Gen4 builds on Gen3 benefits with higher power density, also improving energy efficiency in other key industrial applications (e.g., PSU for AI servers)
- Robustness beyond real traction inverter stress conditions
- Several die layout topologies and top metal schemes to match customers power module requirements

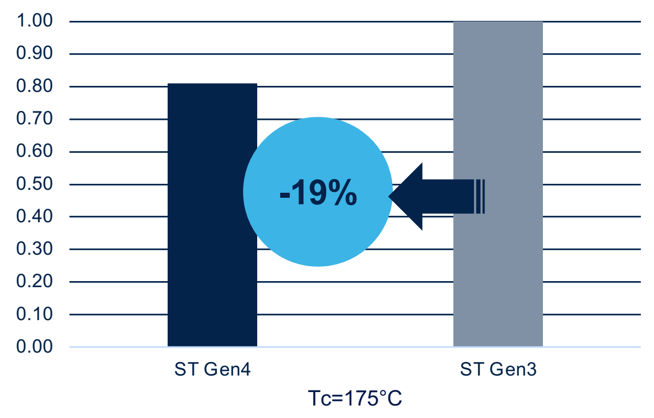

ST Gen4 vs. ST Gen3 & peers

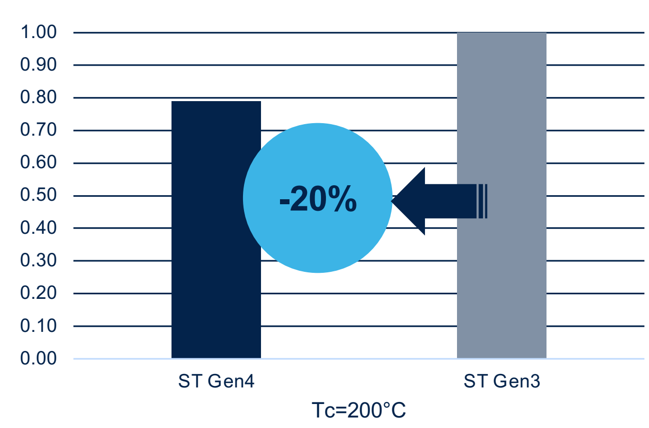
ST Gen4 vs Gen3 $R_{DS(on)}$ comparison

$R_{DS(on)}$ comparison based on same die size and layout (1200 V Gen4 test vehicle)

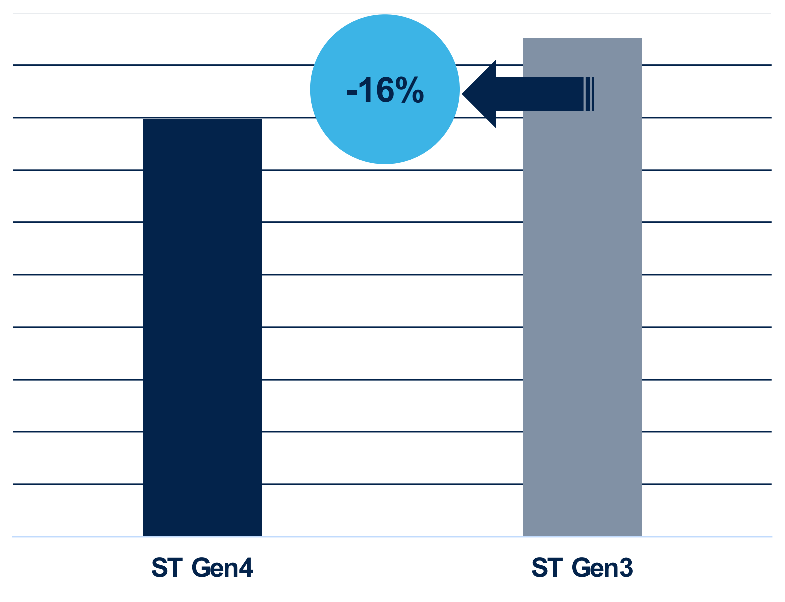
Normalized $R_{DS(on)}$





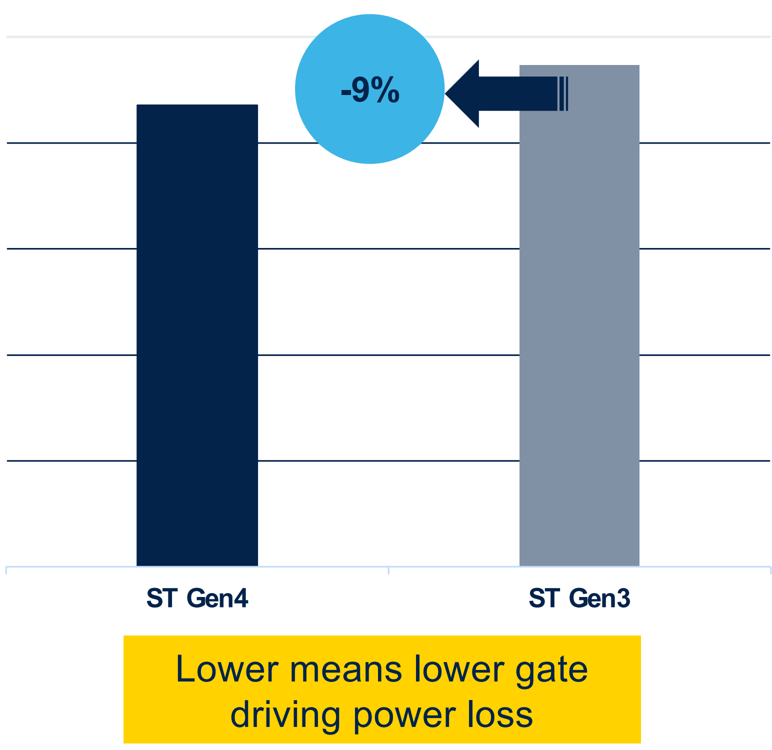


ST Gen4 vs Gen3
Better figure-of-merit (FOM) for energy efficiency



Lower is better in hard switching topologies

$R_{DS(on)}$ x QG (mΩ x µC) at 25°C



ST Gen4 vs peers

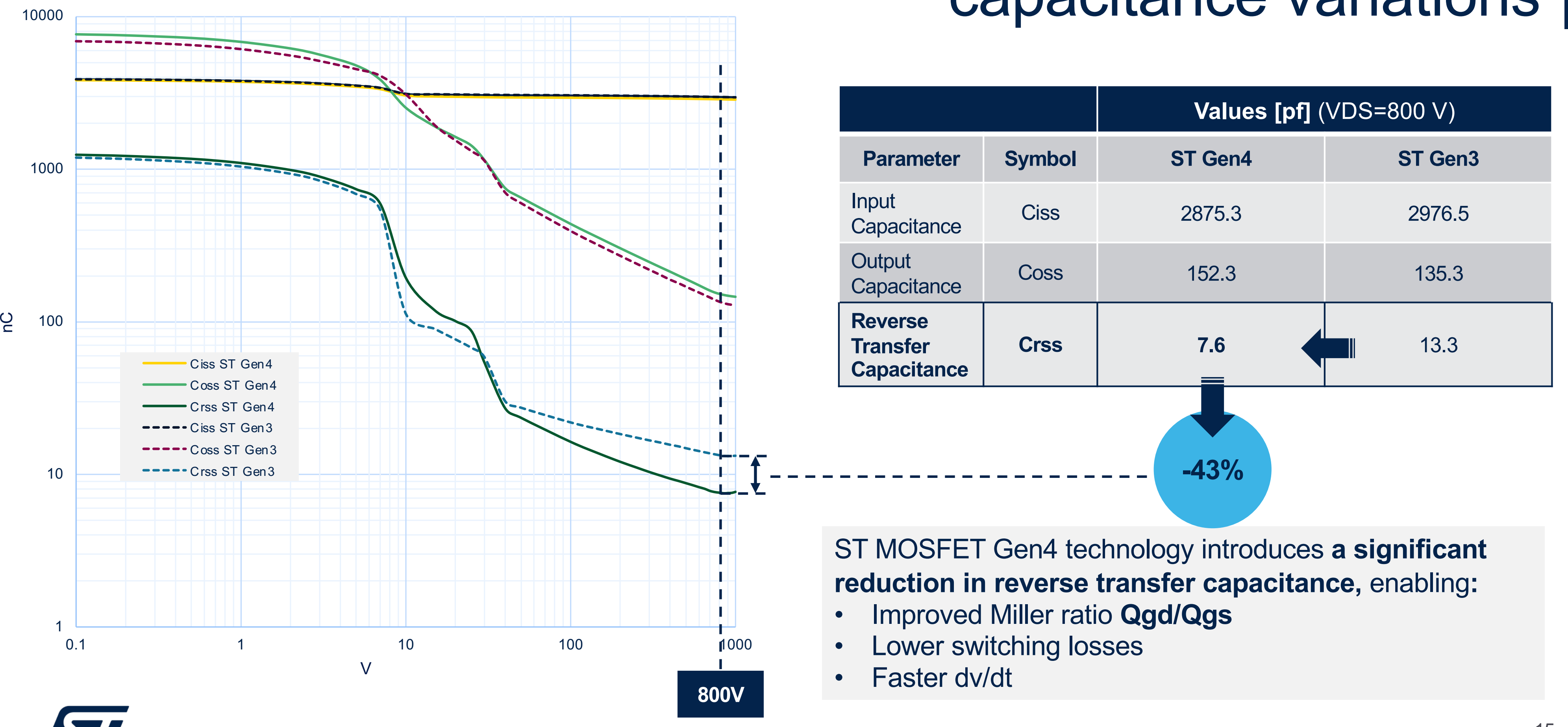
Figure-of-merit (FOM) comparisons

	Ron*Total Area Die (mΩ.cm²) @RT	Ron*Total Area Die (mΩ.cm²) @ 175°C
ST Gen4 Planar	2.95	5.6
Competitor A / Peer A (Planar)	3.62	7
Peer B (Trench)	2.75	6.7
Peer C (Trench)	2.95	6.22
Peer D (Planar)	2.65	5.85

-5%

$R_{DS(on)}$ * Total Area benchmark based on normalized target $R_{DS(on)}$ of 10 mΩ, RT

ST Gen4 vs Gen3 capacitance variations



		Values [pf] (VDS=800 V)	
Parameter	**Symbol**	**ST Gen4**	**ST Gen3**
Input Capacitance	Ciss	2875.3	2976.5
Output Capacitance	Coss	152.3	135.3
Reverse Transfer Capacitance	**Crss**	**7.6**	13.3

ST MOSFET Gen4 technology introduces **a significant reduction in reverse transfer capacitance,** enabling:

- Improved Miller ratio **Qgd/Qgs**
- Lower switching losses
- Faster dv/dt

ST Gen4 vs Gen3 improved Miller ratio

Turn-on Analysis

ST Gen4
ST Gen3

Vgs [V]
Time (sec)
VGS_pk-
VGS_pk-

Turn-off Analysis

ST Gen4
ST Gen3

Vgs [V]
Time [sec]
VGS_pk+
VGS_pk+

***VGS_pk-* reduction**
to increase robustness against the AMR for the Gate Oxide

***VGS_pk+* reduction**
to mitigate risk of parasitic turn-on and optimize the switching losses

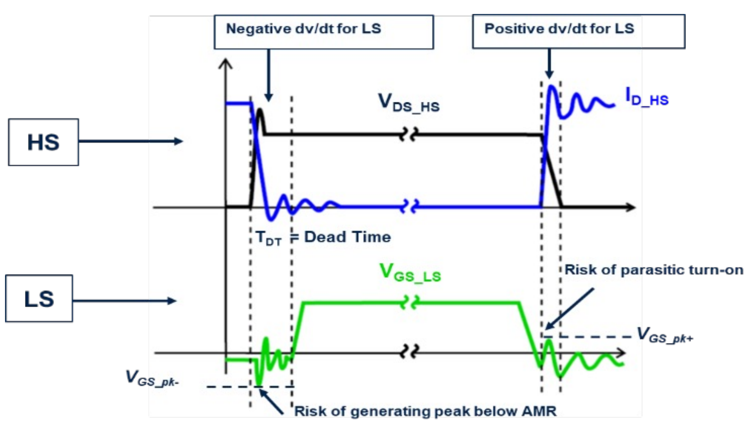
Miller Ratio Qgd/Qgs

- It is the ratio between Qgd and Qgs. It can be considered as the sensitivity of the component to fast switching inducing voltage spike on the gate.

  It has to be as low as possible.

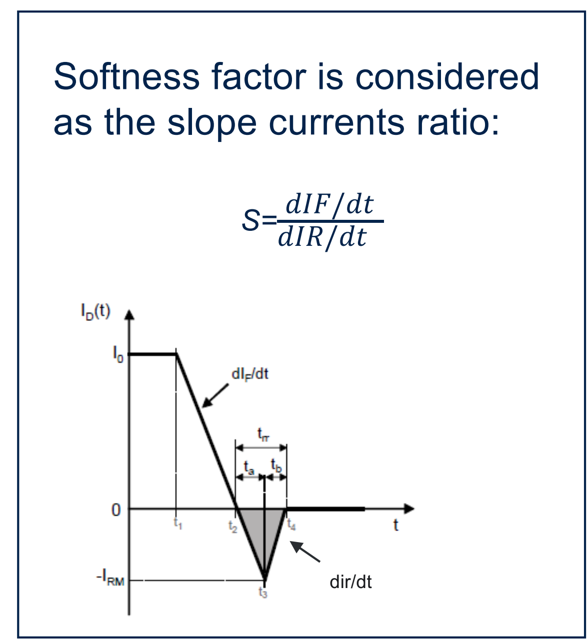
Applicative Benefits

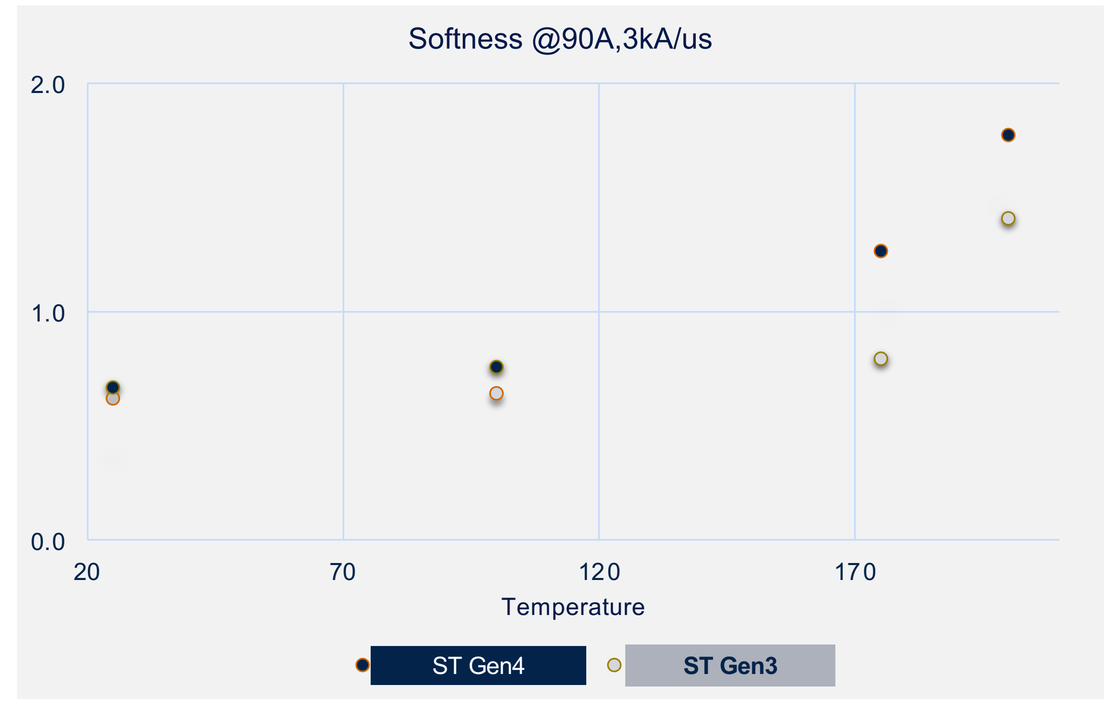
- **Robustness →** the negative glitch exceeding the AMR (-10V) may impact the SiC MOSFET reliability;
- **Power losses →** the positive glitch increases the losses in hard-switching applications;



Gen4 vs Gen3 body diode softness

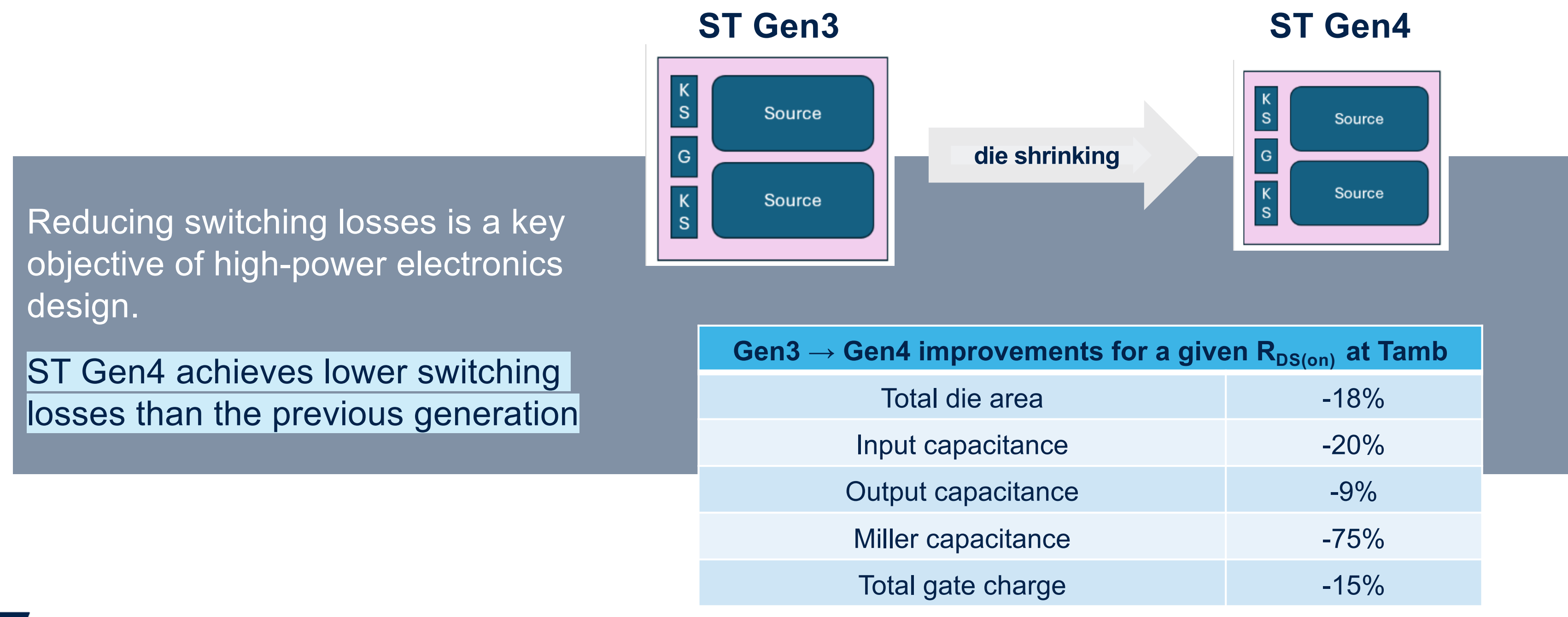
Superior Gen4 diode softness at higher temperatures and di/dt and current helps reduce Eon (switching losses) for applicative conditions





1200 V Gen4 vs Gen3
Comparison for a given $R_{DS(on)}$

ST Gen4 enables the accelerated design of more cost-optimized, efficient, compact, and reliable systems

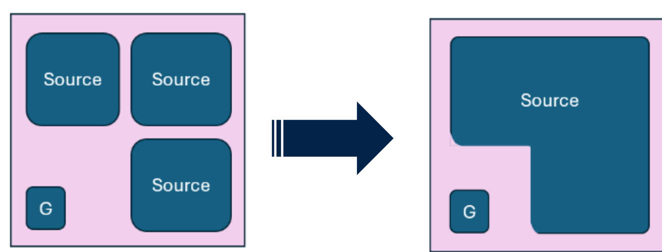


Gen3 → Gen4 improvements for a given $R_{DS(on)}$ at Tamb	
Total die area	-18%
Input capacitance	-20%
Output capacitance	-9%
Miller capacitance	-75%
Total gate charge	-15%

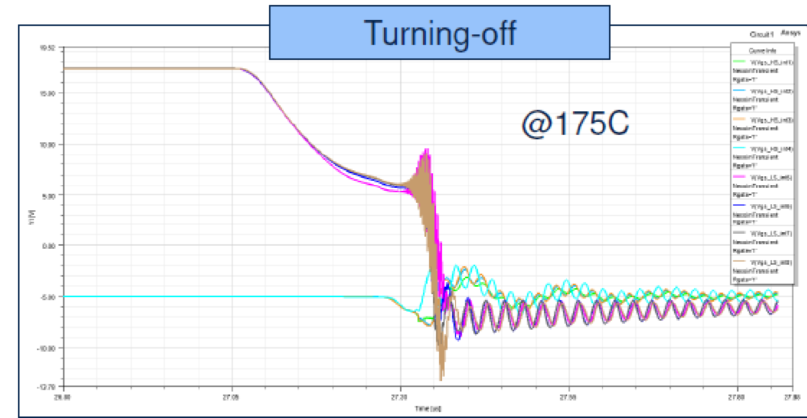
ST Gen4
Embedded Rg for easy paralleling of dice

Applicative benefits

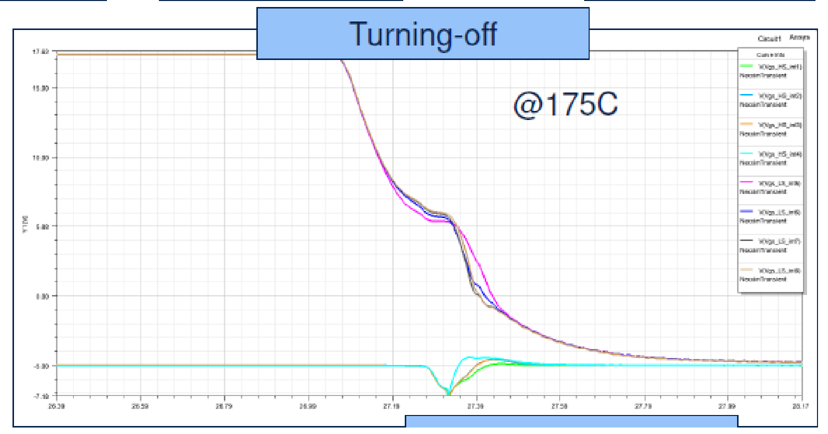
- **Robustness →** ringing on gate and drain voltage when several dice are connected in parallel is reduced
- **Power losses →** thanks to reduced ringing, switching speed can be increased leading to higher efficiency
- **Cost reduction →** Rg already integrated in the die helps to reduce or remove the discrete one



Embedded Rg helps making the parallel easier



Without embedded decoupling Rg



With embedded decoupling Rg

Same Rg_{Total} = Rgext (*)+ Rgint . (*) Rg on gate driving board

ST SiC package technologies

SiC MOSFET package technologies

PowerFLAT 8x8	TO-LL	H2PAK-7L	HU3PAK	ACEPACK SMIT	HiP247 (3 ,4, long leads)	STPAK	Bare dice
Surface mounting					Through-hole	Special package solutions	
Very thin (<1 mm) Well accepted in power conversion Leadless **Industrial domain**	**2.4 mm** (max) thickness Good Rthj-a performance Leadless **Industrial domain** Kelvin source for optimized driving Good thermal dissipation	**AG qualified at 175°C** Kelvin source for optimized driving High runner for automotive customers	**AG qualified at 175°C** Top side cooling Kelvin source for optimized driving Very good thermal dissipation	**AG qualified at 175°C** Isolated top side cooling Suitable for different configurations (HB, dual die, etc.) High power Modular approach	**AG qualified at 200°C** **Very common industry standard** Kelvin source option for optimized driving High creepage version (1700 V) in development	**Unique solution for traction inverter** **AG qualified at 200°C** **Very high thermal dissipation efficiency** Sense pin for optimized driving Multisintered package High creepage option available	**WLBI & KGD** **T&R or RWF options** **Compliant with the most stringent automotive quality requirements**

Top-side cooling package: HU3PAK*

Automotive quality standards
AEC-Q101 qualified

High temperature capability
Tj (max)= 175°C

High voltage rating
Up to 1200 V

Improved thermal dissipation
Top-side cooling

Efficient
Kelvin source pin enables higher efficiency

Electric arc prevention
Higher creepage distance for better isolation

Compactness
SMD package for more compact systems

Smaller form factor
Direct top-side connection to heatsink

* registered and/or unregistered trademarks of STMicroelectronics International NV or its affiliates in the EU and/or elsewhere

ACEPACK* SMIT

Flexible
Suitable for several applications

Robust
2500 Vrms electrical isolation

Easy
SMD assembly

Thermal performance
Dice chips on direct bonded copper (DBC) substrate

Fast in switching
Reduced parasitic inductance and capacitance

Ideal
For building a complete system

Configurable
Several configurations available and low stray inductance

Reliable
High reliability and robustness, miniaturized power sideboard

Cost-effective
Cost-effective system approach

Compact
Compact design and very high power density

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Multisintering STPAK*

Automotive quality standards
AEC-Q101 qualified

High temperature capability
Tj (max)= 200°C

High voltage rated
650 V / 1200 V

Mechanical reliability
Improved thermal performance due to bottom direct sintering to heatsink

Control
Sense pin for enhanced control

System compactness
High power density

Flexibility
Modular design approach

High efficiency
Gen3 SiC MOSFET embedded

Robustness
Internal clip design

Cooling system reduction
Very good thermal dissipation

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ST power modules

System-level design factors for power module packaging

Electrical performance

- High power density
- Low connect resistivity
- Minimize parasitic(R,C,L)

Mechanical performance

- High stability against mechanical and thermo-mechanical loads
- Longer lifetime

Thermal performance

- Balanced temperature distribution within the package
- Ensure effective heat dispassion
- Low Rth material selection

Environmental protection

- Ensure robustness against environmental conditions (humidity, temperature)
- Electrical isolation

Assembly

- Cost optimization
- Miniaturization
- Smart process flows

ACEPACK power module solutions

ACEPACK Power Module - Silicon Carbide MOSFET

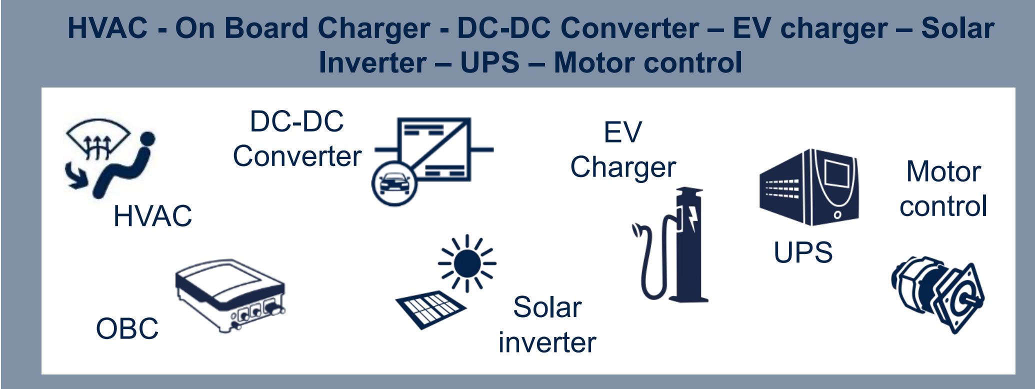
ACEPACK **DMT-32**

ACEPACK **1 & 2**

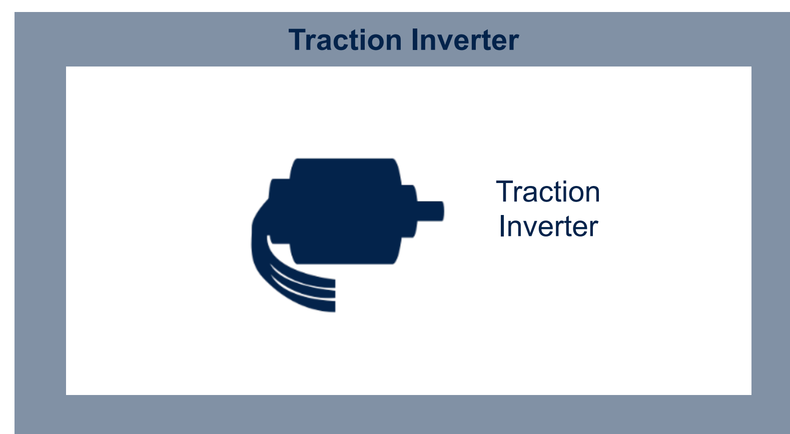
ACEPACK **GEMINI***

5 kW — 10 kW — 30 kW — 340 kW →

HVAC - On Board Charger - DC-DC Converter – EV charger – Solar Inverter – UPS – Motor control



Traction Inverter



*In development

Q&A

Our technology starts with You

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