알테라의 고해상도 영상처리 4K 솔루션

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ALTERA FAE

Industry Trends?

The EBU Technical Committee believes that the current focus of the CE industry to provide only an increased resolution ("4k") and ignoring other enhancements is not a sufficiently large step for the introduction of successful new broadcasting services.

The TC believes that ***the current '4K Ultra-HD' approach of the consumer electronics industry is unsatisfactory*** *and will be of* ***limited success in broadcasting****.*

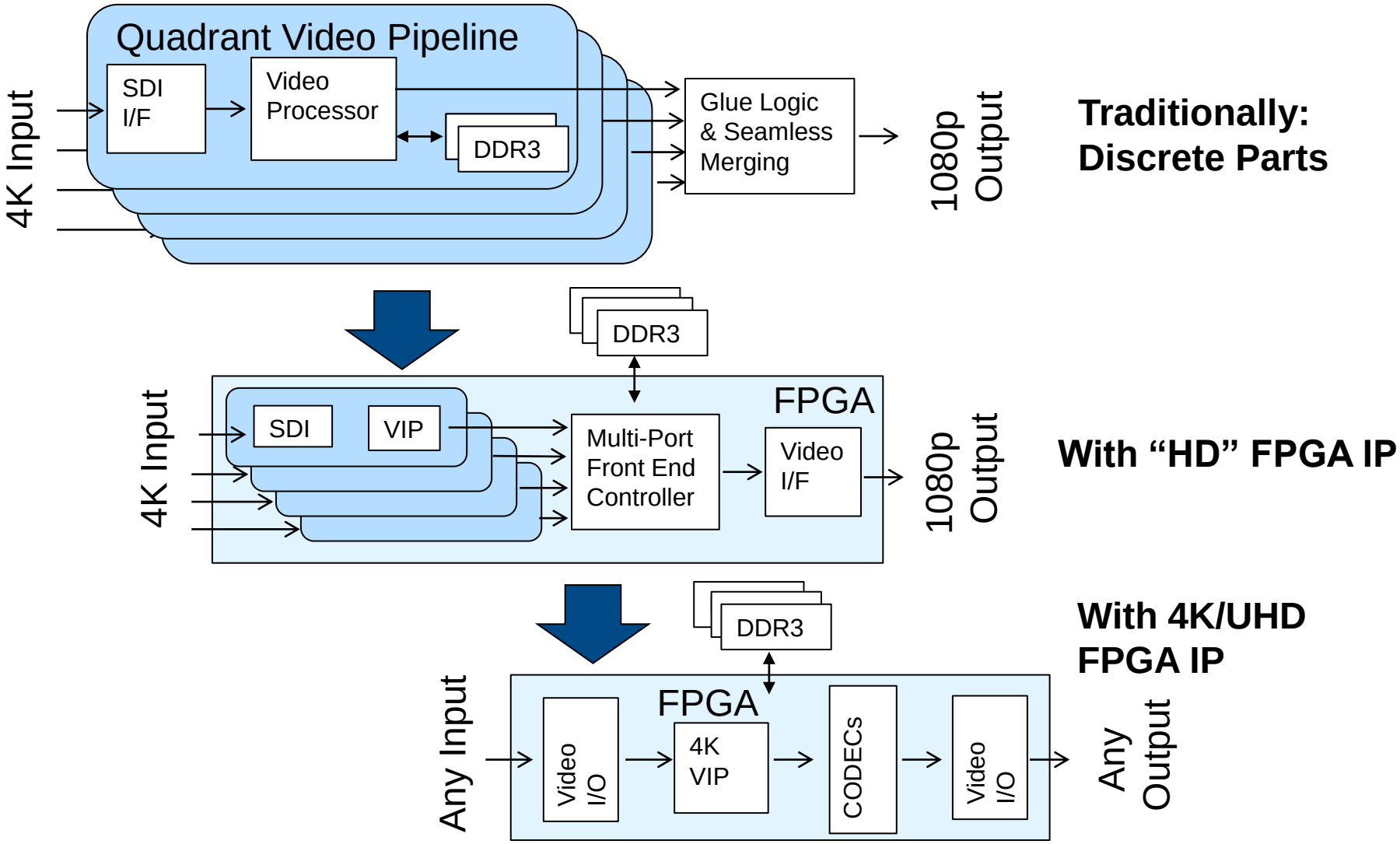
The EBU proposes that an enhanced 1080p format (e.g. higher frame rate, higher dynamic range, wider colorimetry and advanced sound system audio) be developed for broadcasting.

EBU POLICY STATEMENT ON ULTRA HIGH DEFINITION TELEVISION

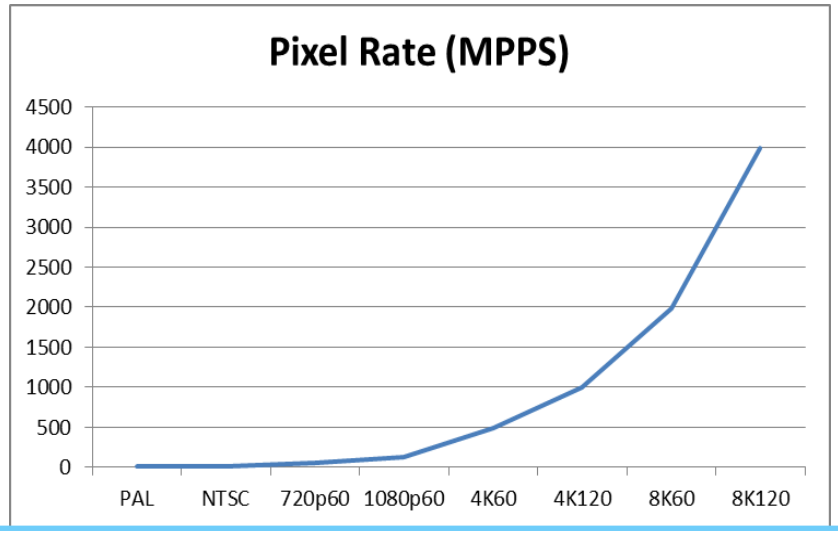
Agenda

- A design approach for implementing 4K video systems
  - FPGA clock rate vs. pixel rate
  - Processing order
  - Connectivity
  - Component approach
  - Memory bandwidth requirement
  - Resource usage
- 4K solution of ALTERA
  - VIP(Video and Image processing suite) IP
  - Connectivity Solution : DisplayPort, HDMI, Multi-rate SDI
- 12G SDI demo

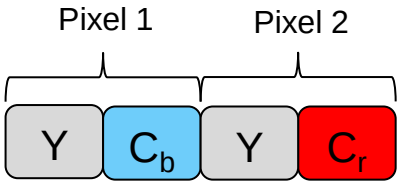
4K VIP value proposition: Then, Now, & Future



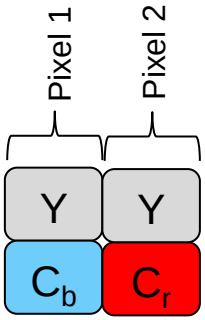
FPGA clock rate vs. pixel rate (1)



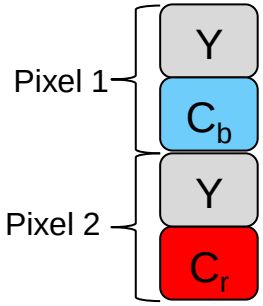
Pixel rate (in millions of pixels per second) for various video formats



PAL/NTSC



HD (1080p60)



UHD (4Kp30)

FPGA clock rate vs. pixel rate (2)

Pixel Rate = P * Clock Rate

Equation 1: Pixel rate versus clock rate (P is the pixel parallization factor)

For SD, video P < 1; for HD video P = 1; and for 4K and higher P>1.

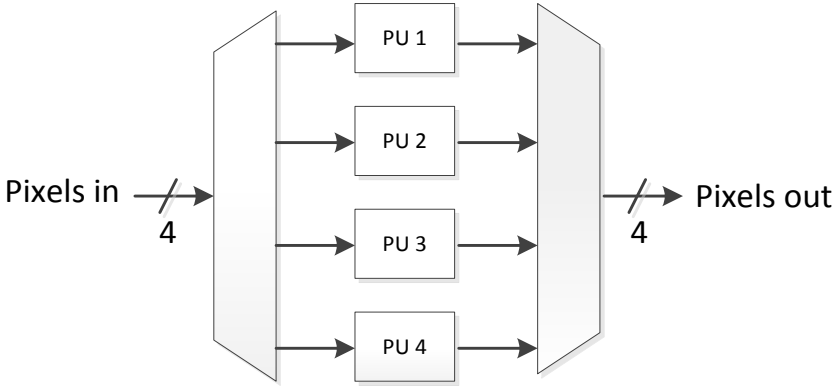
	P=1 pixel per clock	P=2 pixel per clock	P=4 pixel per clock
@ 148.5 MHz	1080p60	4Kp30	4Kp60
@ 297 MHz	4Kp30	4Kp60	4Kp120

FPGA clock rate (MHz) for varying video format and P

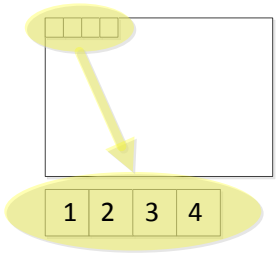
- **Arria 10 rated at 500MHz+ core performance**
- **Room for parallel pixel processing to keep Fmax low**

A10 can support 4Kp60/120 applications with margin

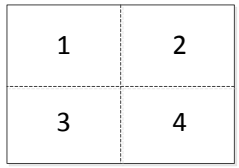
What processing order to use?



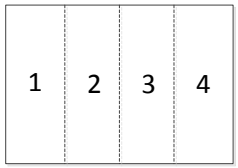
Subdivide the problem: parallel processing



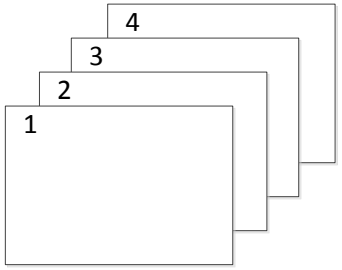
1) Super-sample raster



2) Quadrant based



3) Stripe based



4) Frame based

Processing Order

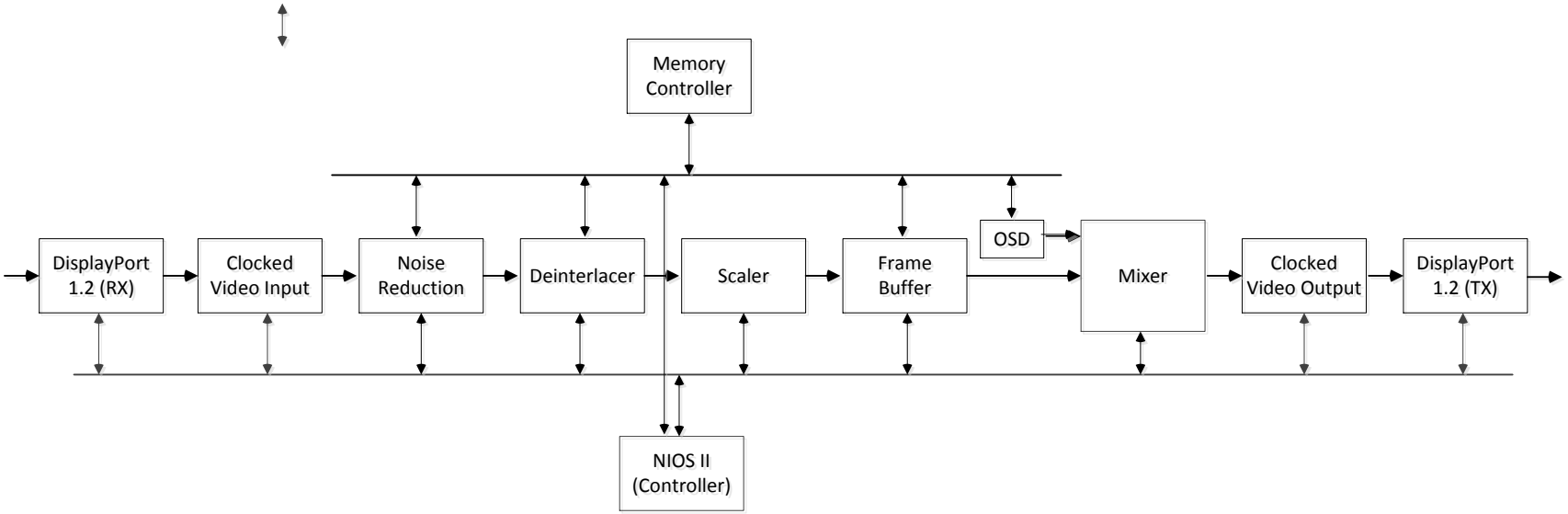
Processing Order	Added Latency	Spatial DD complexity	Temporal DD complexity	Example use
Super-sample raster	None	High	Low	Colour space conversion Clipping, Mixing 4:4:4 <-> 4:2:2 convert
Quadrant based	1 frame	Med	Low	Studio monitor
Stripe based	1 line	Low-Med	Low	Scaling Noise reduction (MATF)
Frame based	4 frames	Low	Med	Multi-Processor

Processing Order: trade-offs

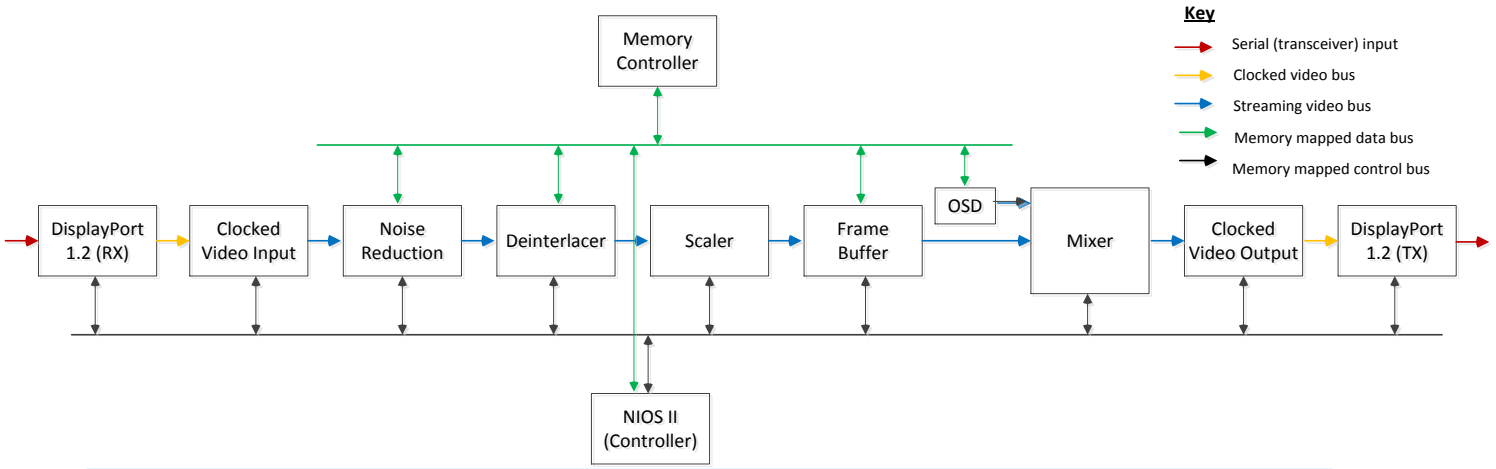
Introducing “video processing channel”

- **Generic video processing channel**

- **Representative video processing channel**



Connectivity (1)



Sample video processing chain (highlighting the different interconnect types)

Interconnect	Typical clock rate(MHz)	Typical Data Width	Flow control support	Factors Determining Data Width Scaling
Serial (transceiver) input	1000 – 12000	1-4 transceivers	No	Protocol
Clocked video bus	150-300 MHz	1-4* pixels x 20 bits/pixel	No	Pixel Rate FPGA clock rate
Streaming video bus	150-300 MHz	1-4* pixels x 20 bits/pixel	Yes	Pixel Rate FPGA clock rate
Memory mapped data bus	200MHz	128-256 bits	Yes	Memory interface width Memory clock rate
Memory mapped control bus	100MHz	32 bits	Yes	Required control bandwidth

Summary of interconnects commonly found in video processing systems

Connectivity (2)

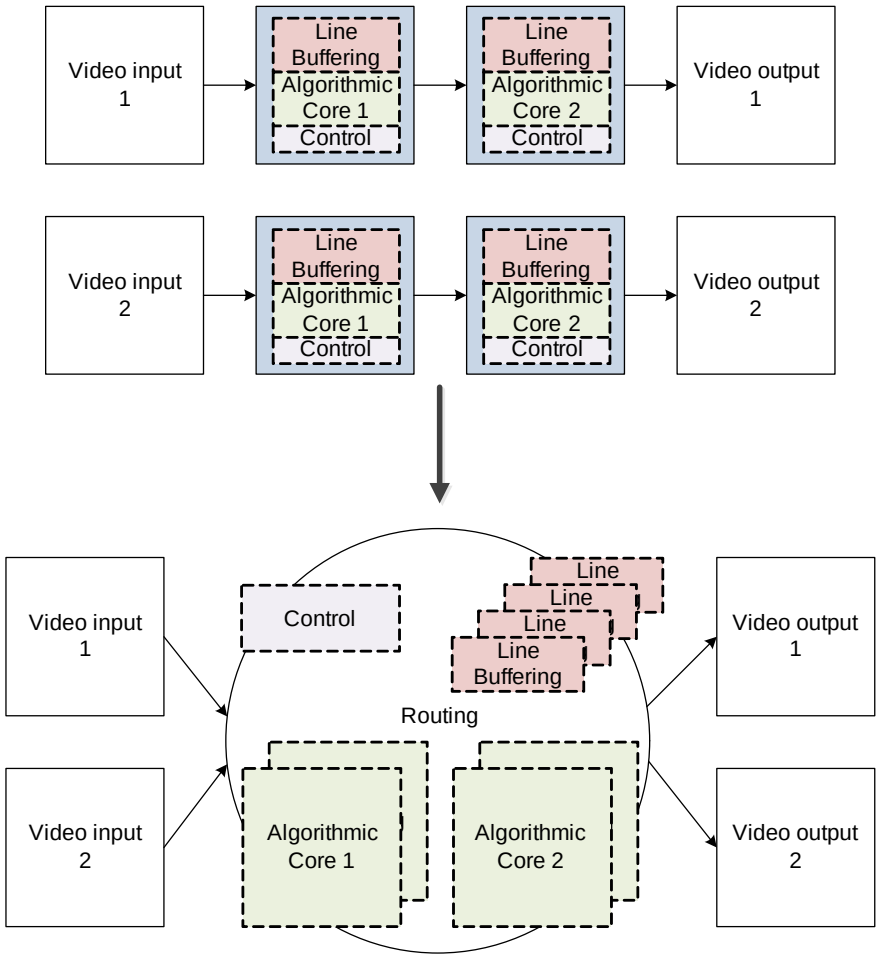
- **Ethernet**
  - Compressed (J2K, other) or uncompressed
    - Compression = higher latency (order 1 frame)
- **SDI**
  - Up to 3G rate standardised today
  - 12G technology demo by Altera and TI at IBC 2013
- **HDMI / DisplayPort**
  - No standards to support beyond 4K60

Format	Pixel Rate	SDI	HDMI	DP	Ethernet (raw)	Ethernet (J2K/other)
1080p	3G	3G SDI	1.3	1.1	10G	1G
4K30	6G	2x 3G, 1x 6G	1.4	1.2	10G	10G
4K60	12G	4x 3G, 1 x 12G	2.0	1.2	40G	10G
4K120	24G	2x 12G, 1x 24G	?	?	40G	10G

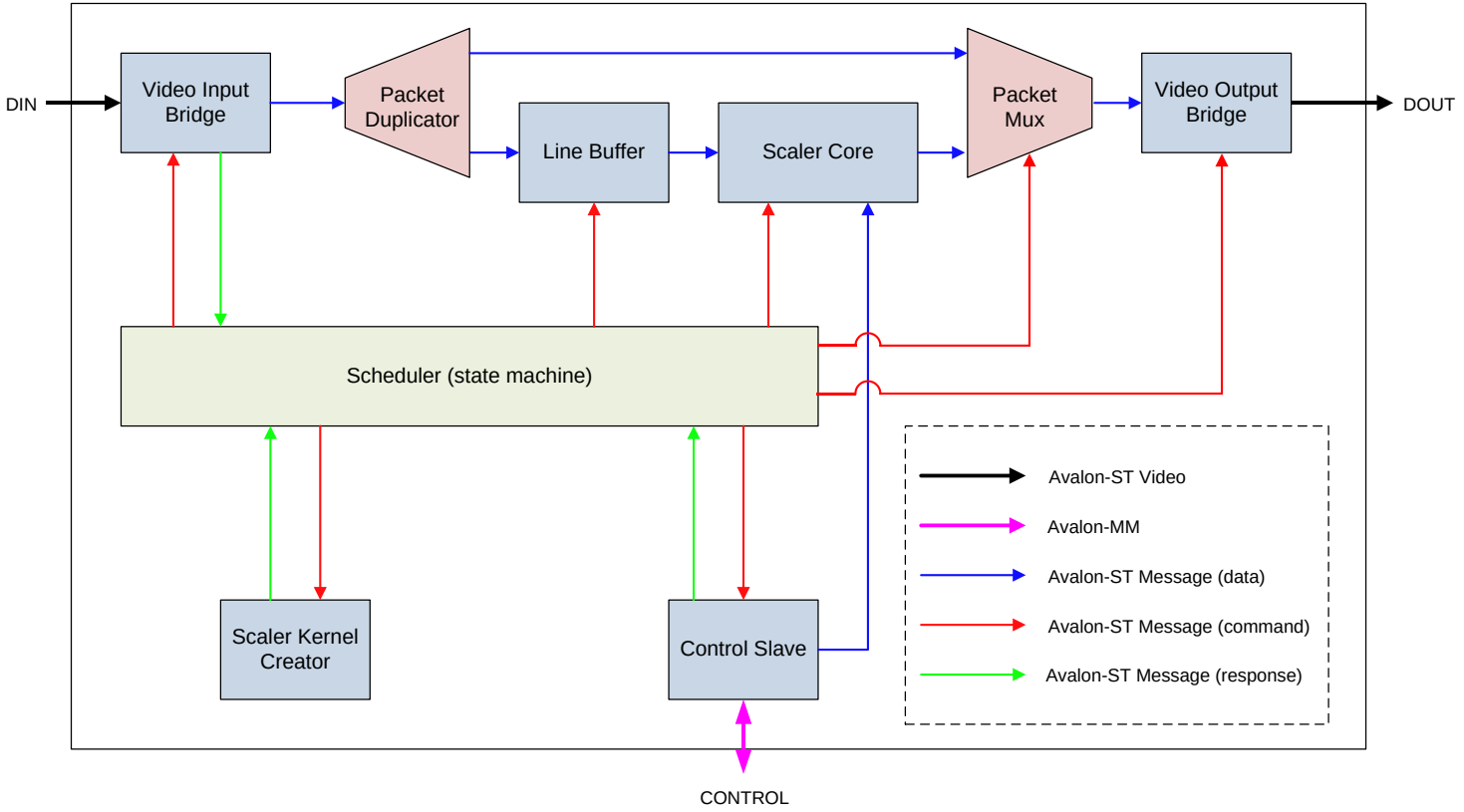
Connectivity versus Pixel Rate

Component approach

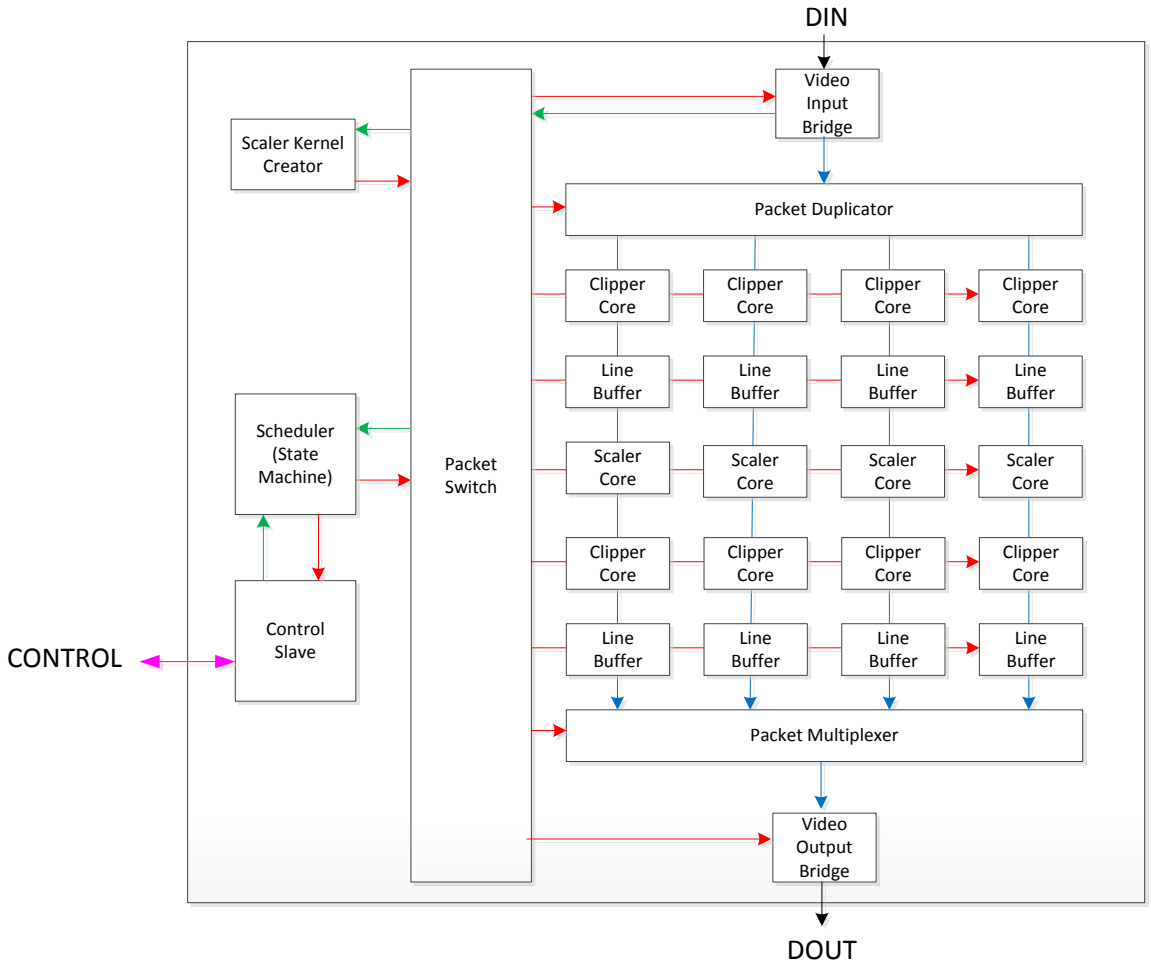
- **Motivations**
  - Scalable library of IP functions
  - Run-time configurability
  - Compile-time configurability
- **Features**
  - Shared common components
  - Separate control
    - Inter line (scheduler)
    - Intra line (algorithmic core)
  - Support prototype designs



Example 1: HD Scaler



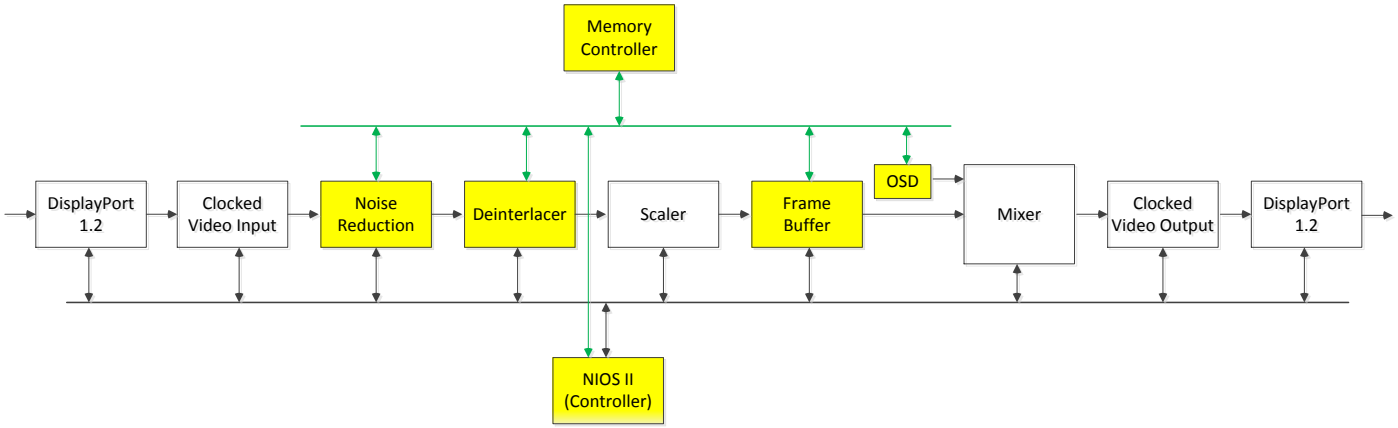
Example 2: 4K scaler



Memory Bandwidth Requirement

Memory Configuration	Theoretical Peak Bandwidth (Gbps)	4K60 frame buffers	8K60 frame buffers	4K60 video channels	8K60 video channel
32-bit DDR3 @ 333MHz	21.3	1	0	0	0
64-bit DDR3 @ 667MHz	85.4	4	1	1 (4,2)	0 (1,0)
32-bit DDR4 @ 1333MHz	85.3	4	1	1 (4,2)	0 (1,0)
64-bit DDR4 @ 1333MHz	170.6	8	2	2 (8,4)	0 (2,1)

Theoretical peak bandwidth for example memory configurations
Bracketed numbers are for (up, down) scale operations – i.e. non-worst case



Typical video processing channel (with blocks requiring off-chip memory access highlighted)

4K Scaler: Line Buffer and Multiplier Requirements

- **Downscaling requirements (Lanczos-2 algorithm)**

	4K -> HD	8K -> HD	4K -> PAL	8K -> PAL
Downscale H (Lanczos 2)	8	16	24	44
Downscale V (Lanczos 2)	8	16	16	32
Max H downscale ratio	2	4	6	11
Max V downscale ratio	2	4	4	8
Line buffers	7	15	15	31
Multipliers per colour plane	16	32	40	76

Buffer and Mutliplier requirements for differing down scaling ratios

- **Up-scaling requirements (Lanczos-2 algorithm)**
  - 8 horizontal and vertical filter taps
  - Equals: 7 line buffers and 16 multipliers per colour plane

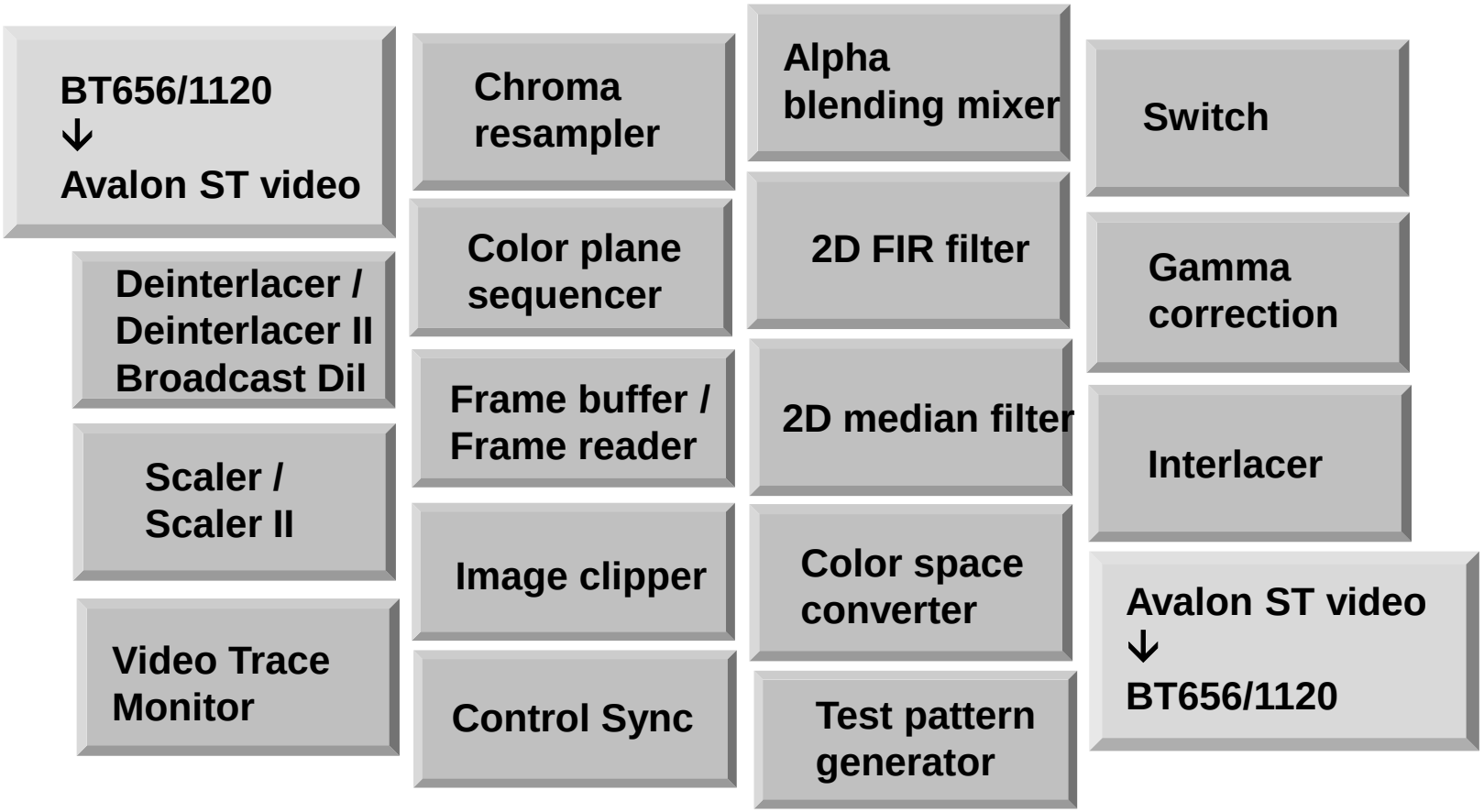
System resource usage (e.g. Arria 10)

- **Using complete 1080p60 pipeline as reference**
  - Including SDI, EMIF, deinterlacing, etc.
- **Arria 10 example devices**
  - GX160 = 1-ch SD-to-4Kp30 format conversion
  - GX320 = 1-ch SD-to-4Kp60 @ 148.5MHz pixel clock
  - GX660 = 1-ch SD-to-8Kp60 @ 297MHz pixel clock
  - GX1150 = 1-ch SD-to-8Kp60 @ 148.5MHz pixel clock

	1080p60	4Kp60	Max on Arria 10
Logic Elements	75k	300k	1150k
Block RAM	283 (M10K)	566 (M20K)	2713 (M20K)
18-bit Multipliers	98	392	3036

Smallest A10 can support basic 4K functions

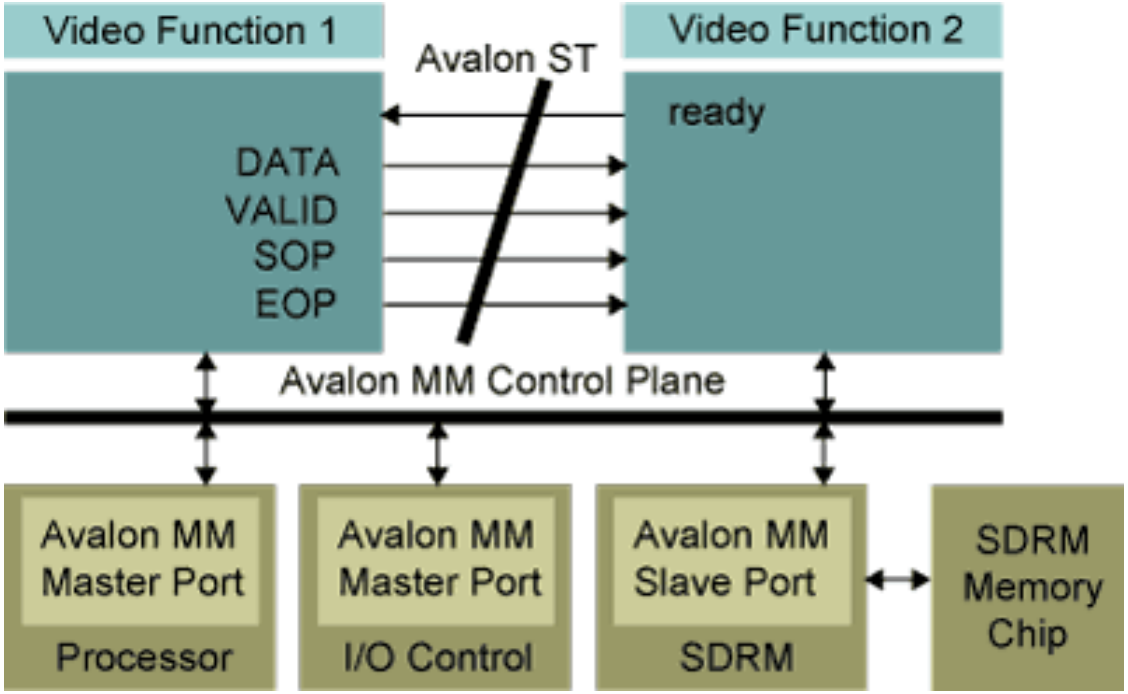
Video Image Processing (VIP) Suite



Current status of VIP IP

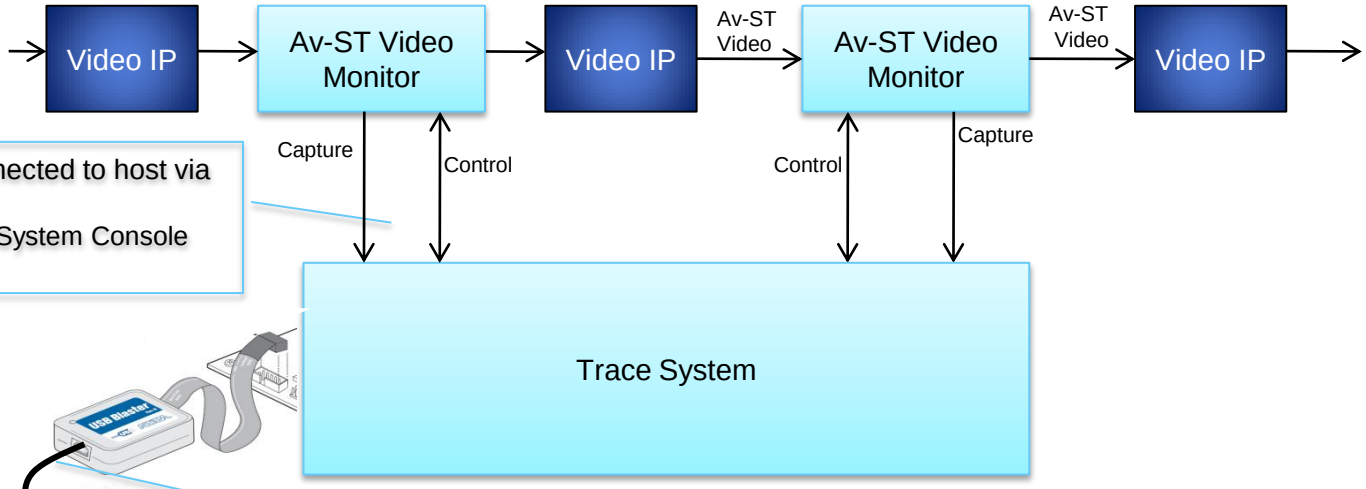
IP Core	UHD/4K support	IP Feature Comments
Avalon-ST video Monitor	Yes	ACDS 14.1
Test Pattern Generator II	Yes	ACDS 14.1
Color Space Converter II	Yes	ACDS 14.1
Clipper II	Yes	ACDS 14.1
Clocked Video Input II	Yes	ACDS 14.1
Clocked Video Output II	Yes	ACDS 14.1
Switch II	Yes	ACDS 14.1
Frame Buffer II	Yes	ACDS 14.1 limited ACDS 15.0 release
Broadcast Deinterlacer	Yes	ACDS 15.0
Chroma Resampler II	Yes	ACDS 15.0
Scaler II	Yes	ACDS 15.0
Color Plane Sequencer	Yes	ACDS 15.1

Open, Low-overhead Interface Standard: Avalon Streaming (ST) Video



Open interface protocol for streaming video data paths and memory-mapped control paths

Video Trace Monitor

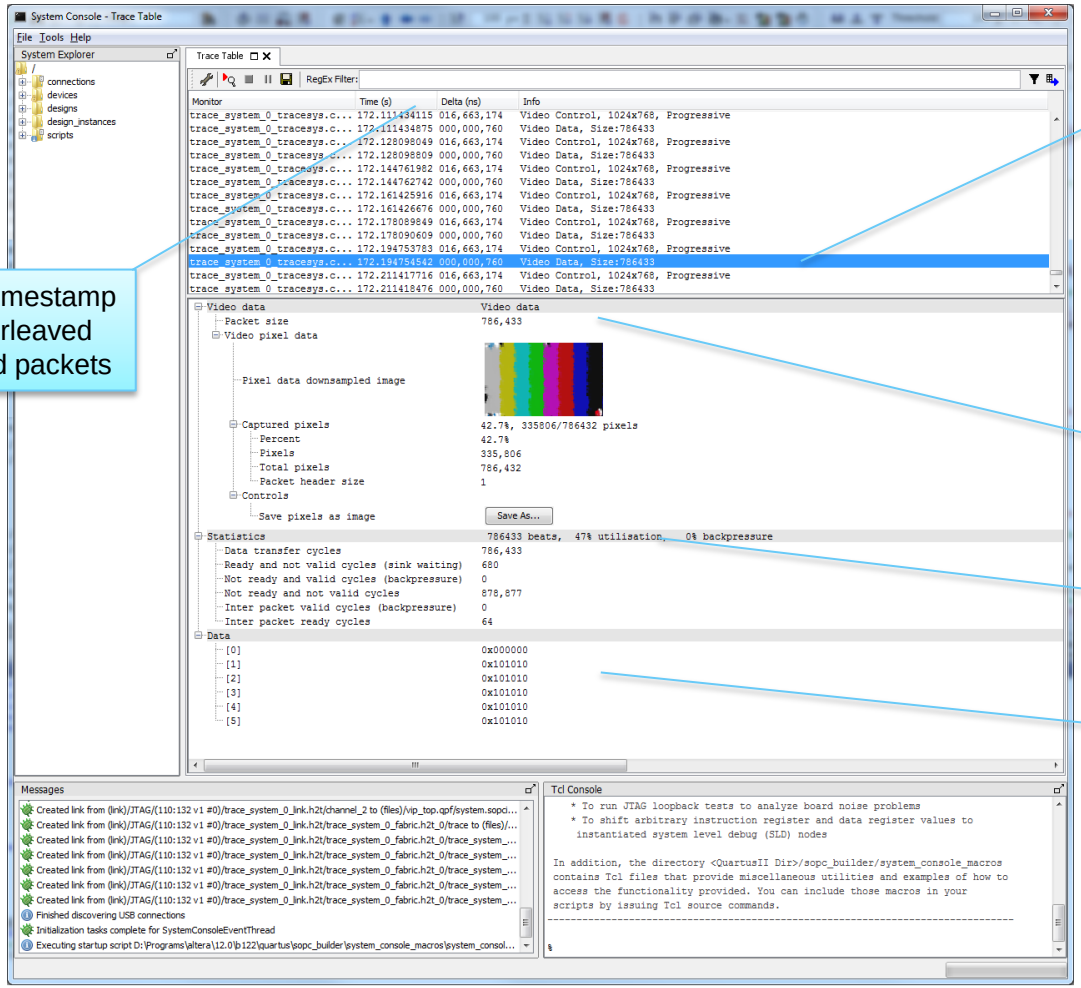


Monitor Capture and Control ports connected to host via Trace System and debug pipe
- Control port enables configuration from System Console
- Captured data output via capture port

Debug pipe
- JTAG or USB

Productivity Tool for Video Debug

Video Trace Monitor – Trace Table View



Live trace of selectable video control and data packets

Global timestamp with interleaved captured packets

Multi-level view

Av-ST Video protocol
- Video data packet information

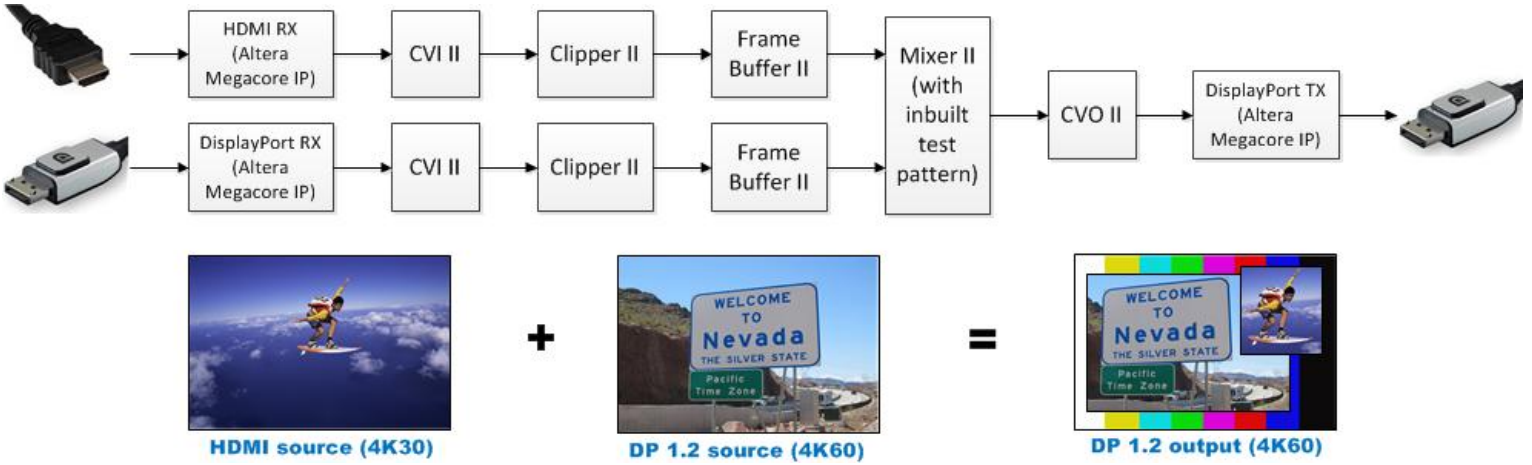
Data flow statistics
- Av-ST standard

Raw packet data
- Up to first 6 beats of data in packet

Connectivity Solution of Altera (1)

DisplayPort

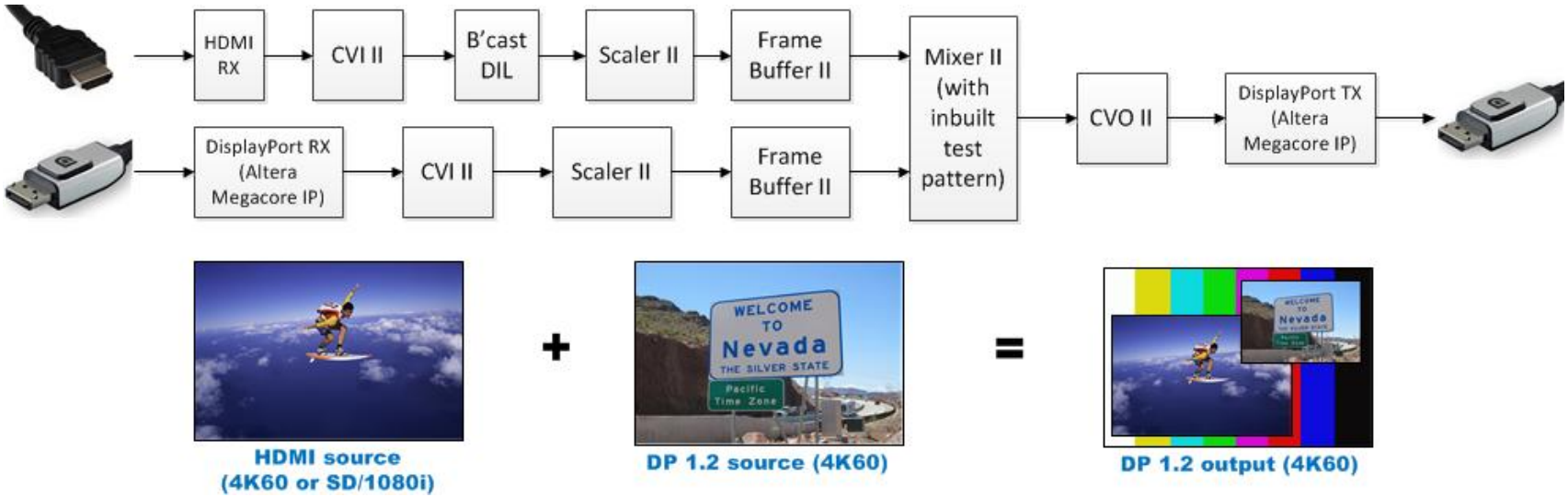
IP Feature	Device support Additions	ACDS example design
DisplayPort 1.1	Arria V , Stratix V	ACDS 14.0
DisplayPort 1.1	Arria V , Stratix V , Cyclone V	ACDS 14.1
DisplayPort 1.2	Arria V , Stratix V	ACDS 14.1
DisplayPort 1.2	Arria V , Stratix V, Arria 10	ACDS 15.0
DisplayPort 1.2	Arria V , Stratix V, Arria 10 , Cyclone V GT	ACDS 15.1
DisplayPort 1.3	Arria 10	ACDS 15.1



Connectivity Solution of Altera (2)

HDMI

IP Feature	Device support Additions	ACDS example design
HDMI 1.4	Arria V , Stratix V	ACDS 14.1
HDMI 2.0	Arria V , Stratix V , Arria 10	ACDS 15.0
HDMI 2.0 Dual viewing add	Arria V , Stratix V , Arria 10	ACDS 15.1



Connectivity Solution of Altera (3)

SDI II

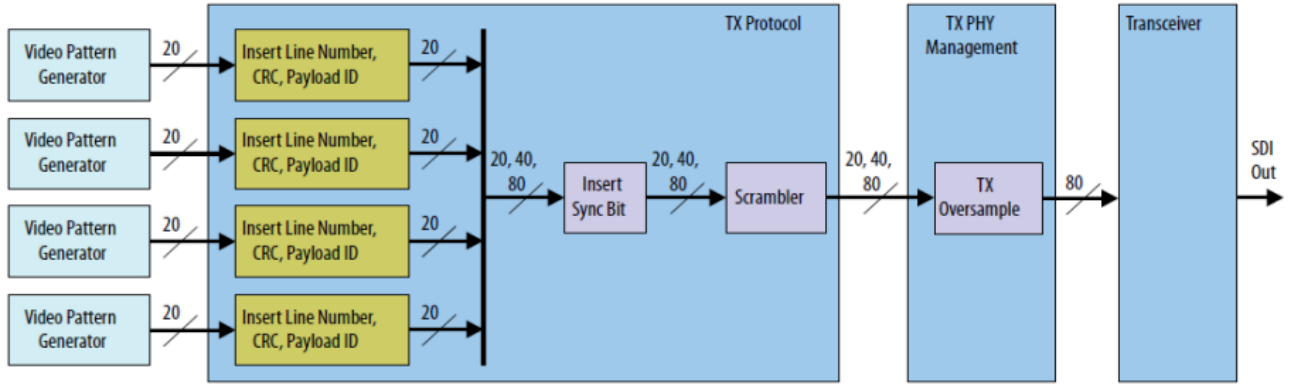
IP Feature	Device support Additions	ACDS example design
Multi-rate SDI (EA version)	Stratix V	ACDS 14.1
Multi-rate 12G SDI II	Stratix V, Arria 10	ACDS 15.0

Multi-rate 12G SDI II

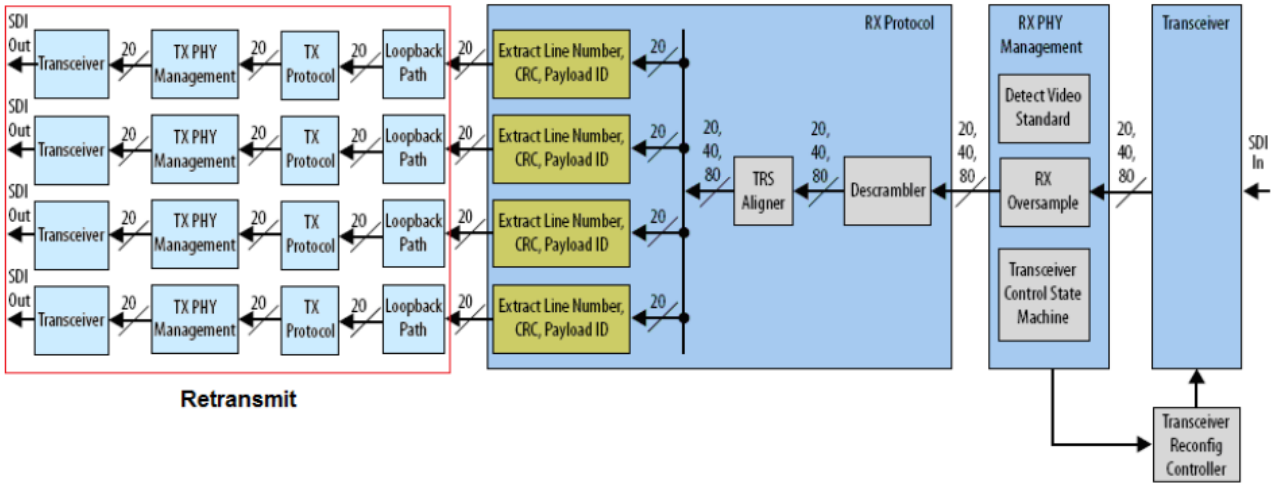
Data Rate	x20 Data Streams Used	User Interface Width
SD (270Mbps)	1	20
HD (1.485 / 1.4835Gbps)	1	20
3G (2.97 / 2.967Gbps)	1	20
6G (5.94 / 5.934Gbps)	2	40
12G (11.88 / 11.868Gbps)	4	80

Multi-rate 12G SDI demo (1)

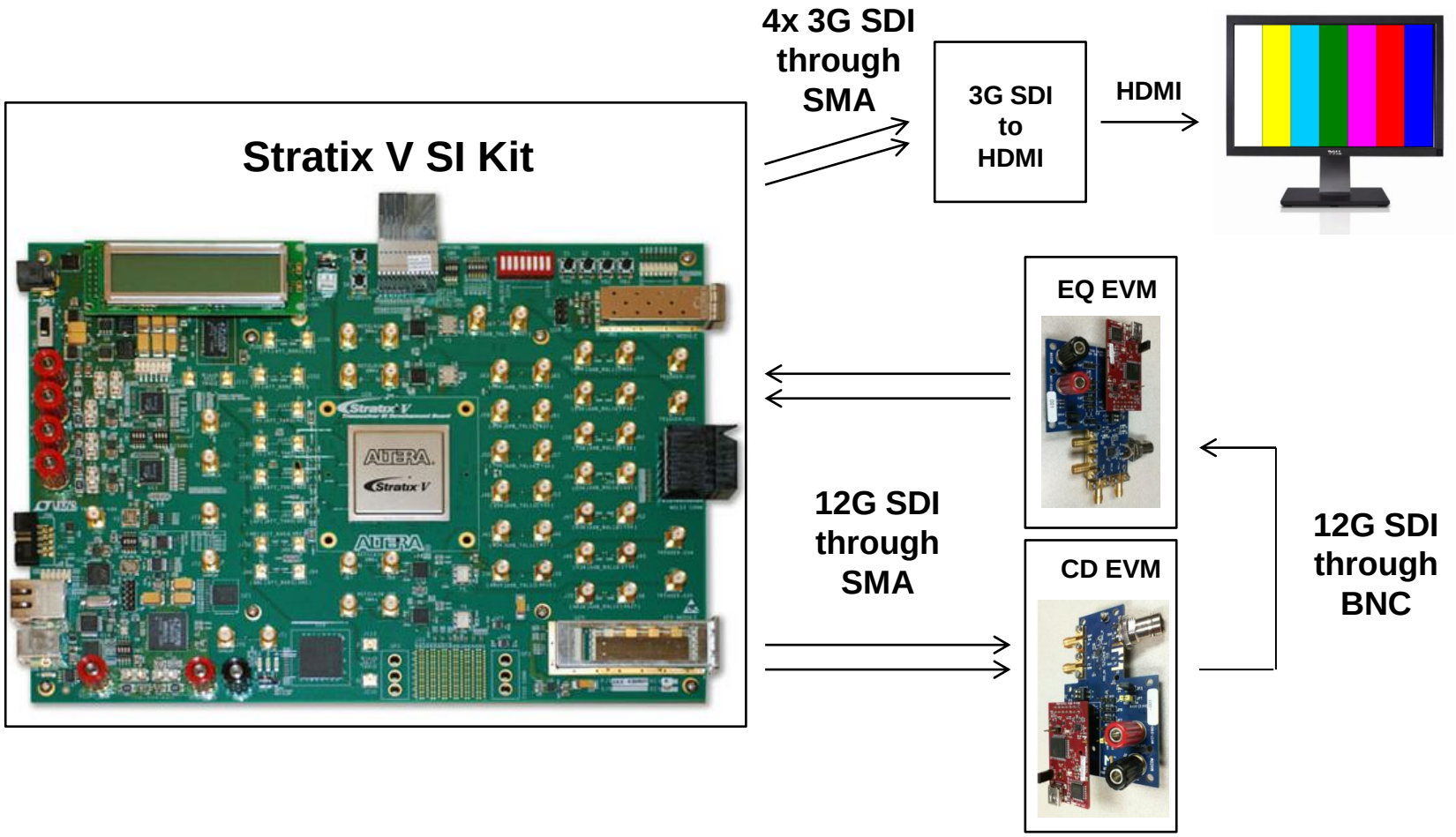
- Transmitter



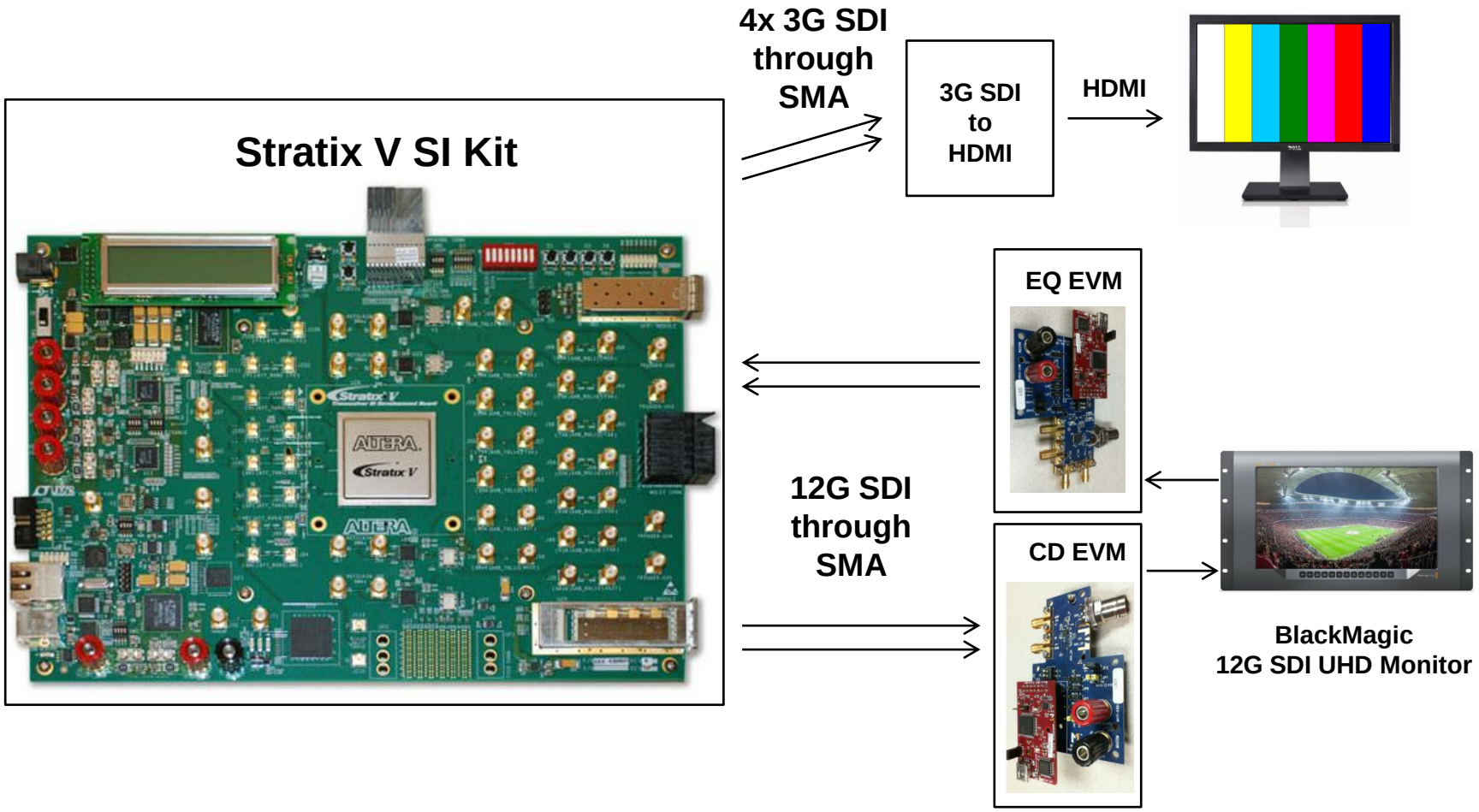
- Receiver



Multi-rate 12G SDI demo (2)



Multi-rate 12G SDI demo (2)



Thank You