Any Media Over Any Network

July 14th, 2015

AGENDA

- **The Megatrend:** Any Media Over Any Network
- Solutions for Any Media Over Any Network
- Strategic Partner of Choice for Broadcast and Pro A/V

The Megatrend: Any Media Over Any Network

Media

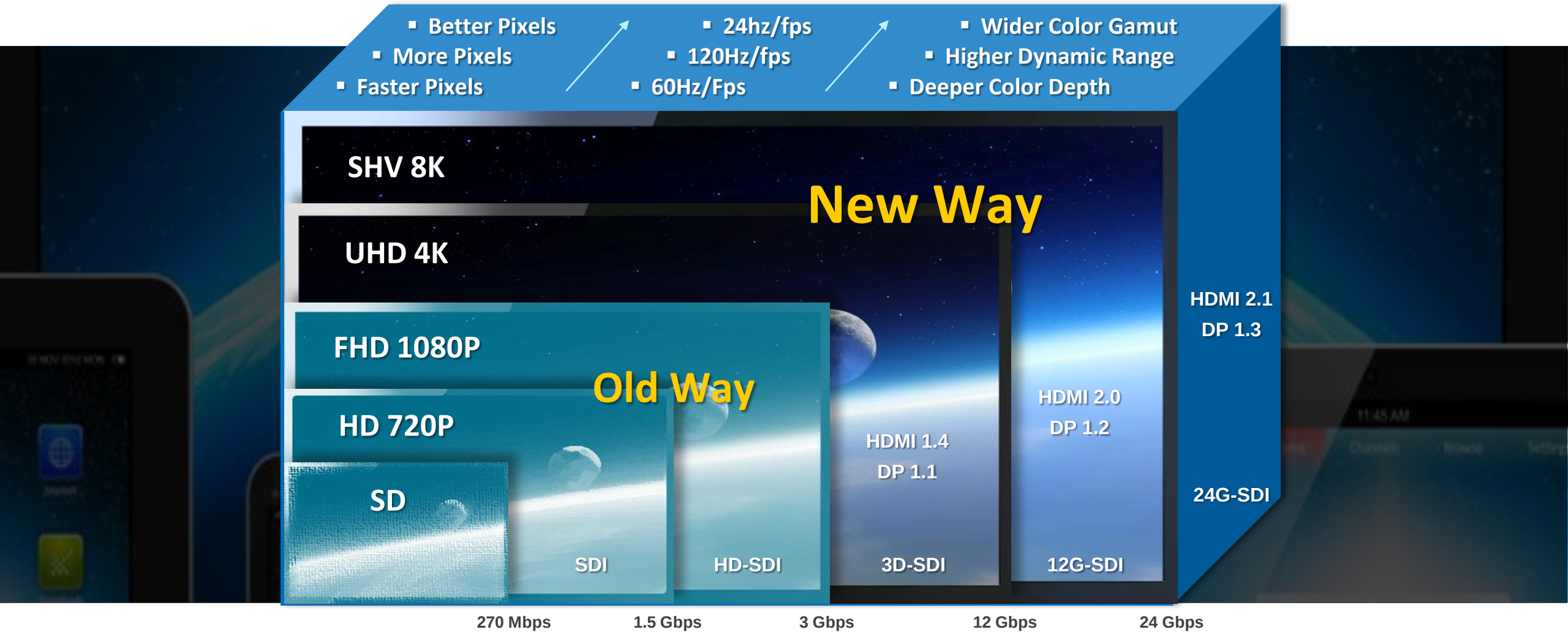
- Live News and Sports
- User/Social Content
- Massive Video Libraries

Network

- Enterprise
- Home
- Cable
- Satellite
- OTT
- Over IP

Consumer Demand for Higher Quality Content

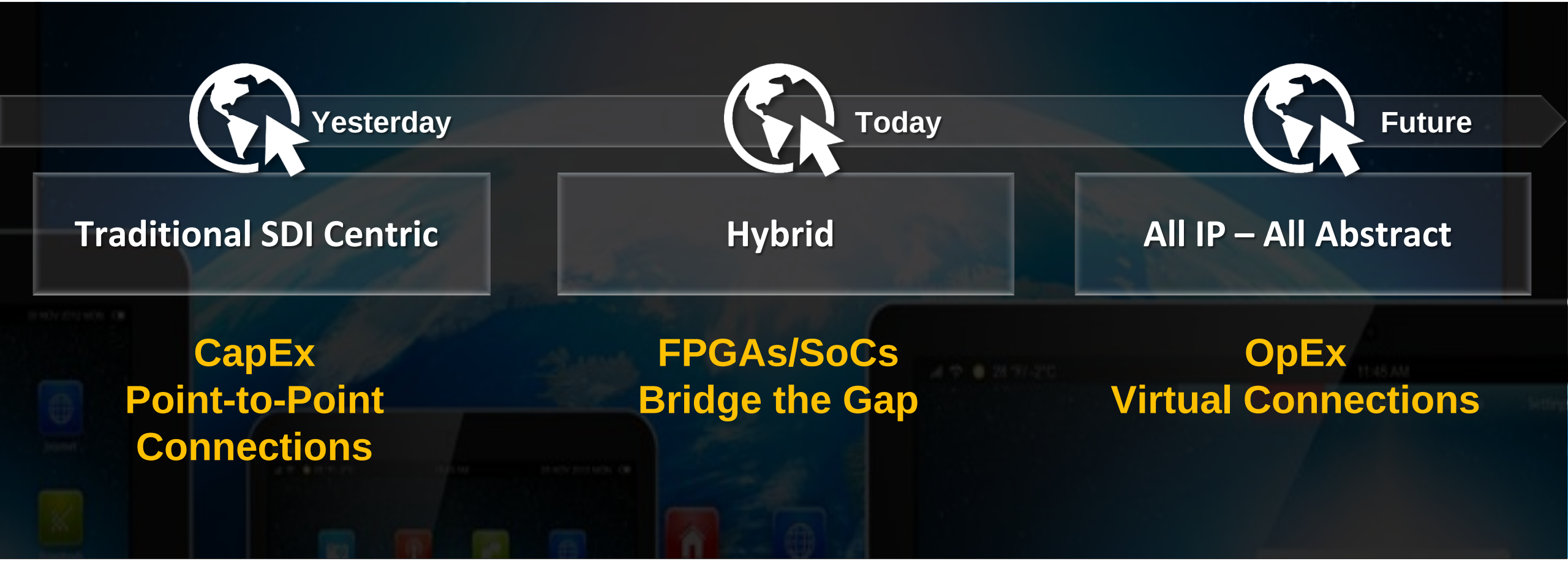
It Cannot Be Done the Old Way



MSOs and Terrestrial

OTT LIVE & VOD OVER BB or LTE

The Broadcast Facility Evolution to All IP



Moving the Truck and Studio to the Cloud

Broadcast Function Virtualization (BFV)

Candidate Functions

- Contribution encoding (TICO, LLVC, VC-2)
- SMPTE 2022/2059
- Transcoding (H.265 / H.264 / VP9)
- Video effects, processing
- Video and metadata analytics
- Distribution of produced content to the CDN and to consumer

It Starts with Xilinx – ALL PROGRAMMABLE

Connectivity	SDx	Video Processing	Compression	Image Processing	Cloud Computing

Next Gen Requirements	All Programmable Solutions
Connected	Audio, Video and Imaging Connectivity
Secure	Design and Content Protection
Software-Defined	SDAccel and SDSoC Environments
Virtualized	Cloud Accelerators, SDN
Analytics	Embedded Vision
Video Everywhere	Transport and Processing of 4K and Beyond

Xilinx Announcements at NAB 2015

Xilinx Enables Any Media over Any Network with Suite of All Programmable Professional Video Solutions

- New cores for HDMI, DisplayPort, UHD-SDI
- New cores for 4K video processing
- New platforms for video processing and connectivity

Xilinx Delivers Next Generation of Video over IP Connectivity to Address Emerging All IP-Based Networks

- Enhancements to support SMPTE ST 2022-7, JPEG2000
- New cores for Video over IP FEC, TICO & SMPTE ST 2059

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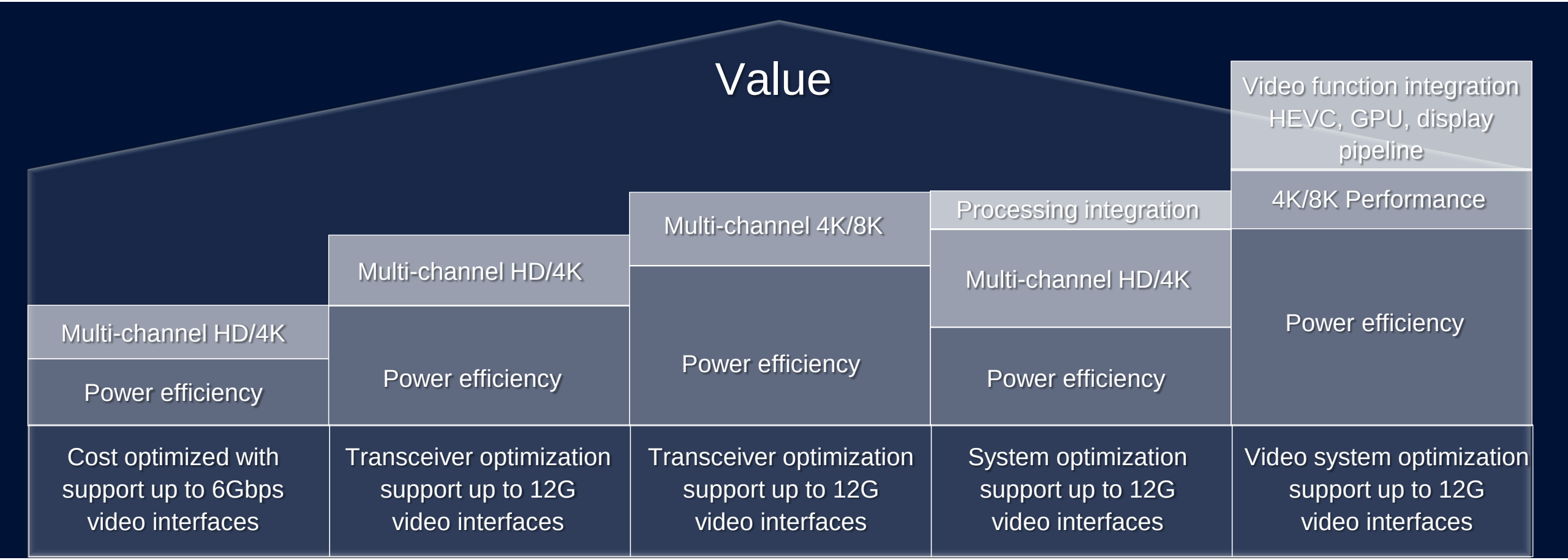
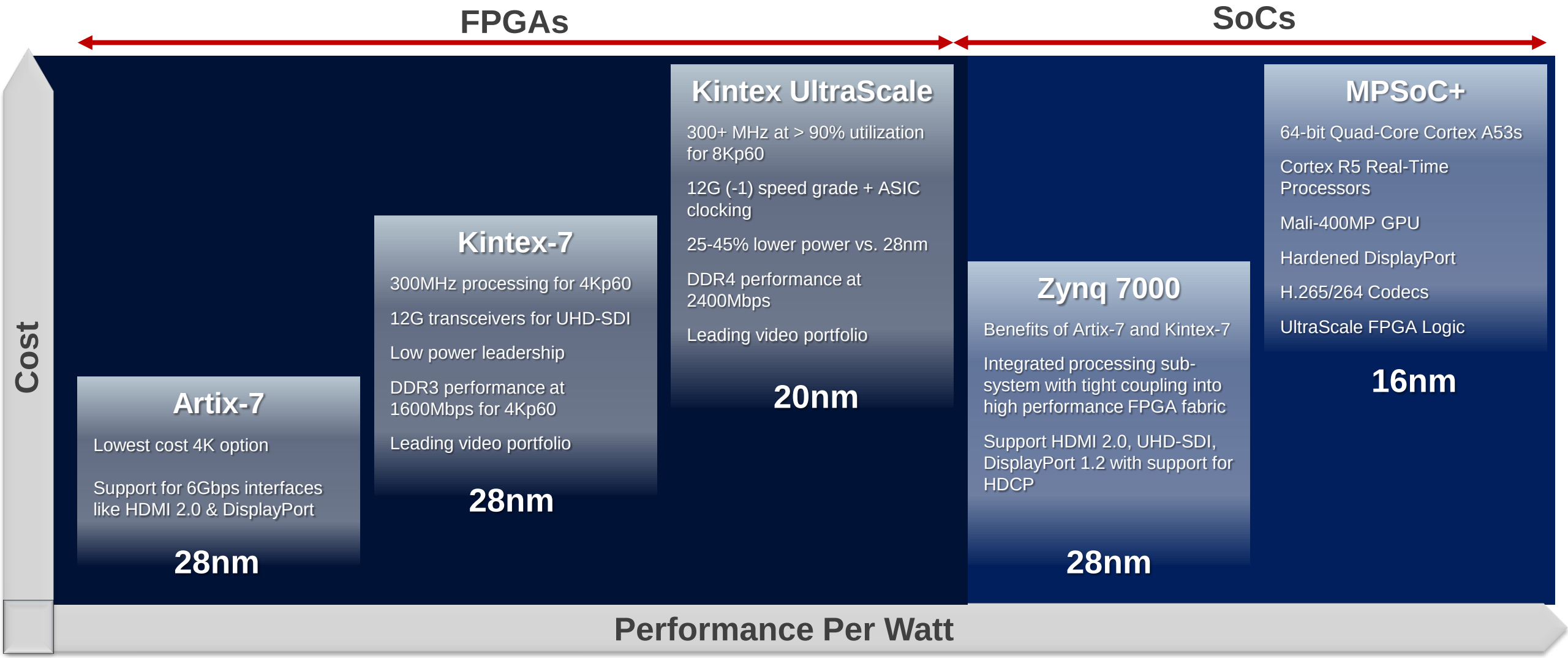
Broadest Cost and Performance Optimized Portfolio



Broadcast and Pro A/V Silicon, Tools and IP Offering



Broadest In-House IP Support: HDMI 2.0 - ST2022 - DisplayPort - UHD-SDI

‘Any Media Over Any Network’ - Connectivity

DisplayPort 1.2

- Xilinx LogiCORE IP
- TX and Rx
- MST, HDCP, Audio

HDMI 1.4/2.0

- Xilinx LogiCORE IP
- TX and Rx
- HDCP, Audio

UHD-SDI

- Xilinx LogiCORE IP
- TX and Rx
- SD/HD/3G/6G/12G-SDI

Xilinx DisplayPort Solutions

LogicCore Feature Set

- Full Featured RX and TX link and stream policy makers
- Hot Plug Detect and Aux channel
- Auto lane rate and width negotiation
- Support for 1.67, 2.7 and 5.4Gbps
- 1,2 and 4 lanes
- Reference design with HDCP 1.3
- RGB and YCbCr 444, 422 support
- DPCD and EDID
- Up to 8-ch audio
- SST and MST support (up to 4 independent streams)
- Support for Kintex®, Artix®, Virtex®, Kintex UltraScale® and Zynq® All Programmable SoC

DisplayPort Source (TX)

- Needs no external components
- DP Redriver (TI DP130) is recommended if driving long cables

DisplayPort Sink (RX)

- DP Retimer (TI's DP159 in X-mode) is recommended for implementing robust DisplayPort Rx
- DP Retimer reclocks data eliminating accumulated timing jitter
- Xilinx DP Tx to Xilinx DP Rx use case needs no external components

Xilinx HDMI Solutions

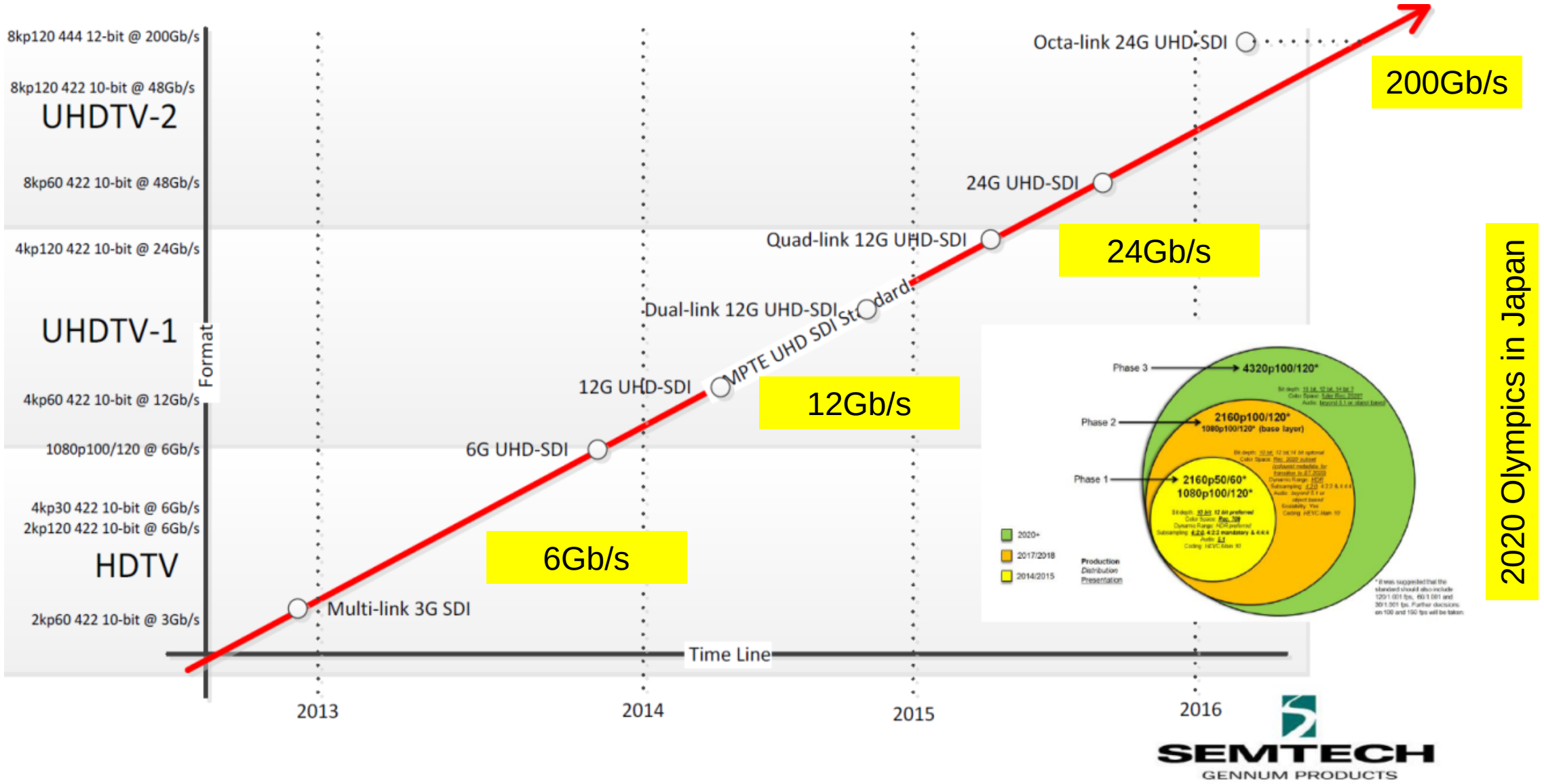
LogicCore Feature Set

- HDMI 1.4/2.0, up to 4K@ 60 fps
- Video formats RGB 4:4:4, YUV 4:4:4, 4:2:2, 4:2:0
- 8-ch audio
- Data Display Channel (DDC)
- Status and control data channel (SCDC)
- Hot plug / EDID
- Dual View and Multi-stream audio support
- AXI4-S interface support
- Reference design of TX/RX loop provided, including software driver
- Tx use external level shifter for TMDS signaling
- Support for Kintex®, Artix®, Virtex®, Kintex UltraScale® and Zynq® All Programmable SoC

New HDMI 2.0 FMC to support 4K

- inrevium TB-FMCH-HDMI4K
- 2x HDMI 2.0 connectors
  - 1x HDMI4K Source
  - 1x HDMI4K Sink
- Stackable FMC supports additional TB-FMCH-HDMI4K
- Available now

SMPTE 32NF70 UHD-SDI Standards Timeline



SEMTECH
GENNUM PRODUCTS

Xilinx UHD-SDI Solutions

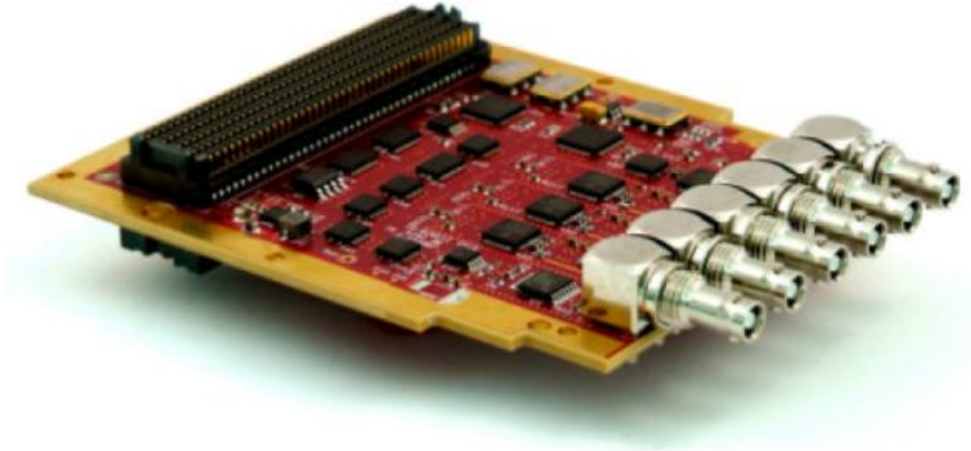
Implementing SDI on Xilinx FPGAs

- UHD-SDI LogicCore
  - Supports SD, HD, 3G, 6G and 12G SDI data rates
  - RX and TX
  - 7-Series GTX, UltraScale GTH
  - Support for Kintex®, Virtex®, Kintex UltraScale® and Zynq® All Programmable SoC
- Board guidelines
  - RX on board uses external SDI cable equalizer
  - TX on board uses SDI cable driver
  - AC coupling between GTs Cable drivers/EQ

All SDI cores & ref designs
are free of charge from Xilinx

New 12G SDI FMC to support 4K

- Inrevium TB-FMCH-12GSDI
- 6x 75Ω HD-BNC connectors
  - 1x 12G-SDI input, 1x 12G-SDI output
  - 3x 12G-SDI in/out, 1x Video Sync input
- Stackable FMC supports additional TB-FMCH-12GSDI
- Available now



Xilinx UHD-SDI Logic-Core Feature Set

UHD-SDI RX

- Per line Error Checking using CRC (EDH for SD-SDI only)
- Line number extraction
- Extracts ST 352 payload IDs
- Automatic rate and video format detection, including level A and level B detection in 3G-SDI mode
- Automatic detection of number of elementary streams in 6G/12G
- Extraction EAV, SAV and TRS

UHD-SDI TX

- Optional gen of CRC for error checking (EDH for SD-SDI)
- Optional Line number gen and insertion
- Optional insertions of ST352 payload IDs
- Supports 1, 2,4,8, 16 data streams muxing
- Automatic sync bit insertion
- Hooks to allow ancillary data insertion

Xilinx IP for SMPTE ST 2022

SMPTE ST 2022-5,6,7

- **Supports multiple SD/HD/3G-SDI channels**
  - E.g. 6x HD-SDI or 3x 3G-SDI
- **Automatic SDI format recognition**
- **Hitless/seamless switch protection**

SMPTE ST 2022-1,2,7

- **Supports multiple channels of compressed streams**
  - Up to 16 TS channels
- **ASI or TS inputs supported**
- **Hitless/seamless switch protection**

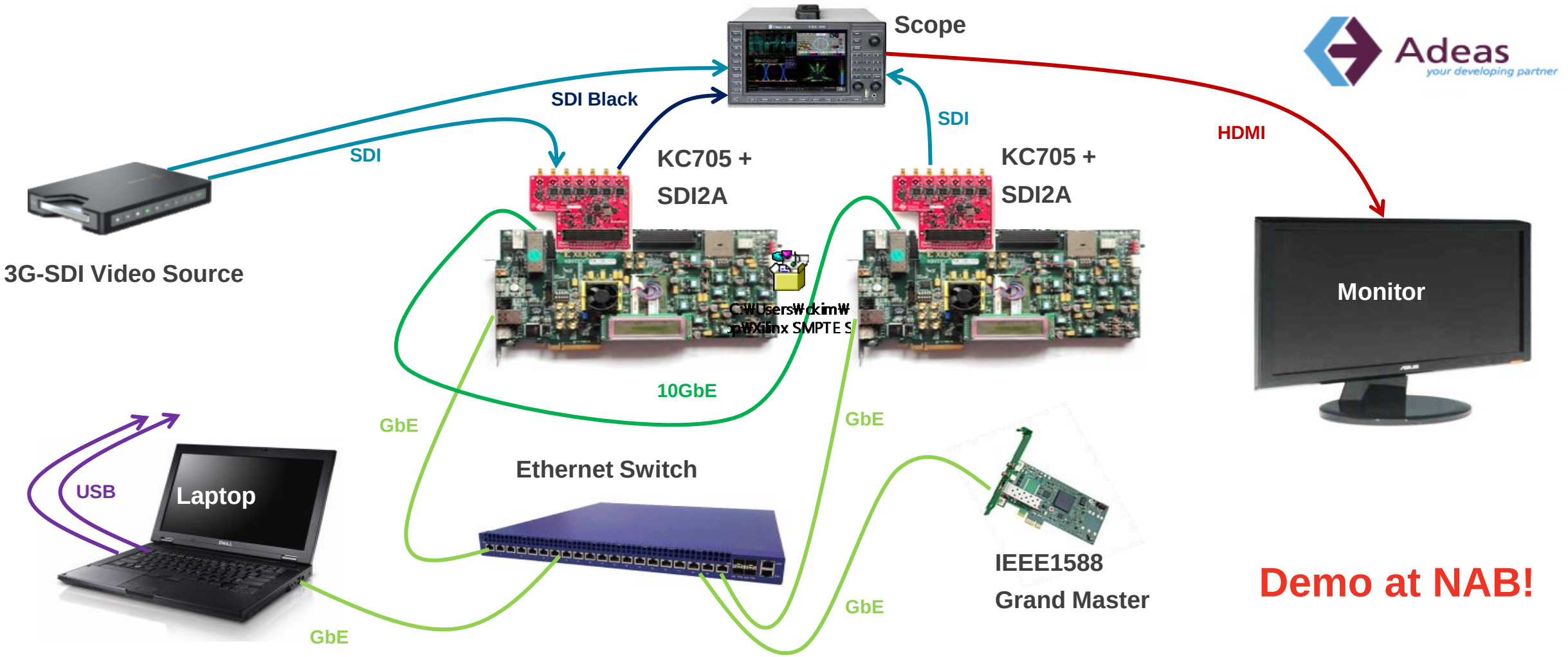
Video over IP FEC

- **Supports multiple channels of compressed streams**
  - E.g. 512 TS channels
- **IP-in to IP-out supported**
- **Hitless/seamless switch protection**

- **Common feature set with support for:**
  - Per stream basis Forward Error Correction (FEC)
  - Supports Level A and Level B FEC operations
  - Supports block-aligned and non block-aligned FEC operations
  - Dynamic switching of L and D values in FEC matrix over AXI4-Lite interface
  - Supports Virtual Local Area Network (VLAN)
  - AXI4-Stream data interfaces and AXI4-Lite control interface
  - User configurable Ethernet, IP, UDP and RTP headers over AXI4-Lite interface
  - Configurable channel selection based on IP source address, UDP destination port, and RTP SSRC identifier over AXI4-Lite interface
  - Supports SD-SDI, HD-SDI, 3G-SDI Level-A and B

- **Note that cores do <u>not</u> support system level functions such as:**
  - IPv6
  - PCR Transport Stream (TS) Jitter
  - Packet buffering
  - IGMP2/IGMP3
  - Full clock recovery schemes

ST 2059 + ST 2022 Demo



‘Any Media Over Any Network’ - Processing

RTVE

Omnitek

- Omnitek IP core and Xilinx ref design
- Scaler, deinterlacer, overlay
- Multichannel up to 4K 60hz

PCIe Video DMA Controller

Omnitek

- Omnitek IP core optimized for video
- Ingest/generate streams up to 4K
- Up to PCIe Gen 3

‘Any Media Over Any Network’ - Codecs

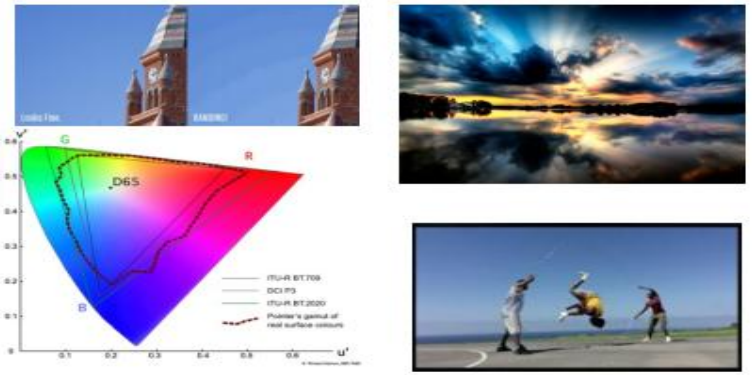
TICO with IntoPIX

intoPIX TICO
secure image technology

- intoPIX IP core for light compression
- HDMI 2.0 <> HDMI 1.4
- 12G-SDI <> 3G-SDI

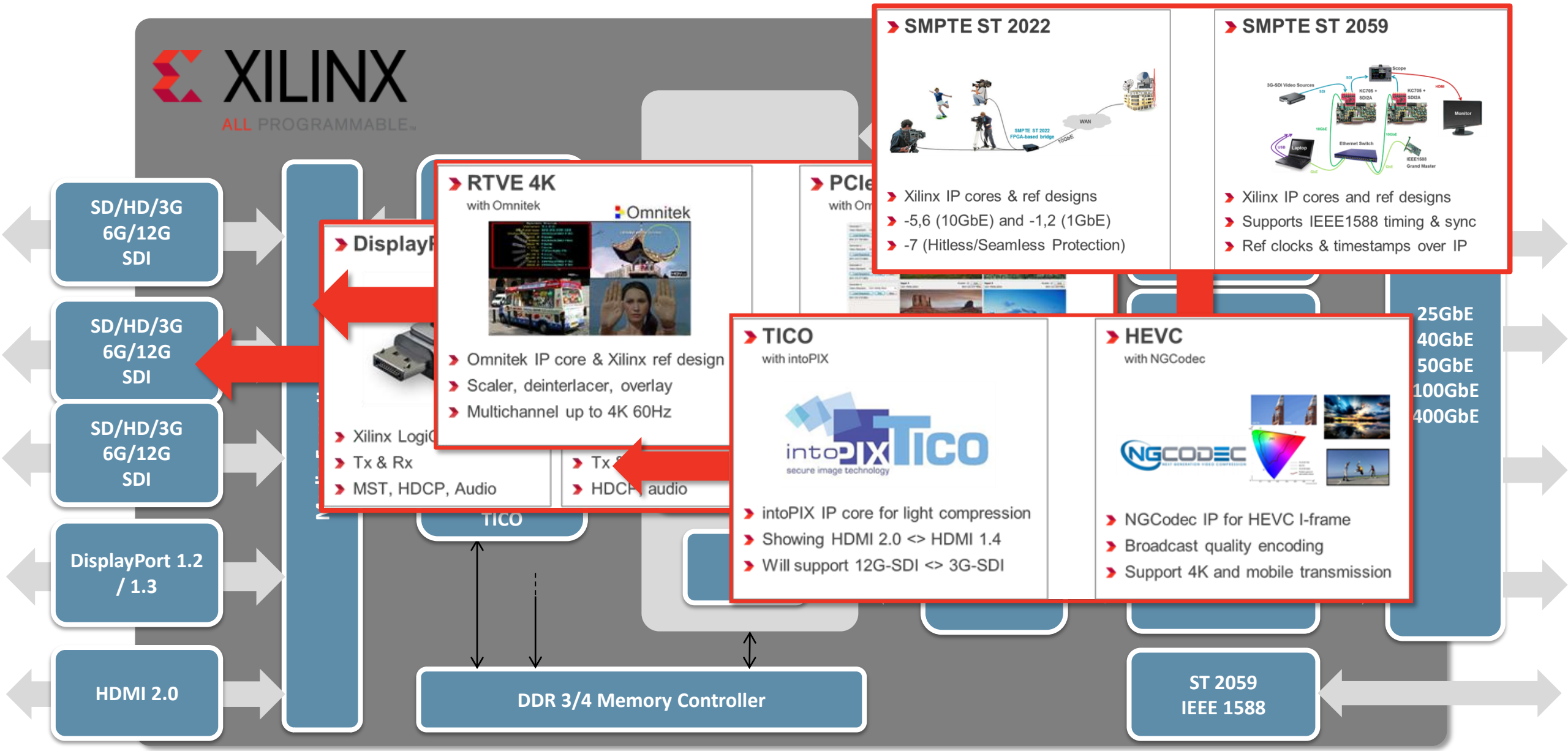
HEVC with NGCodec

NGCODEC
NEXT GENERATION VIDEO COMPRESSION



- NGCodec IP for HEVC I-frame
- Broadcast quality encoding
- Support 4K and mobile transmission

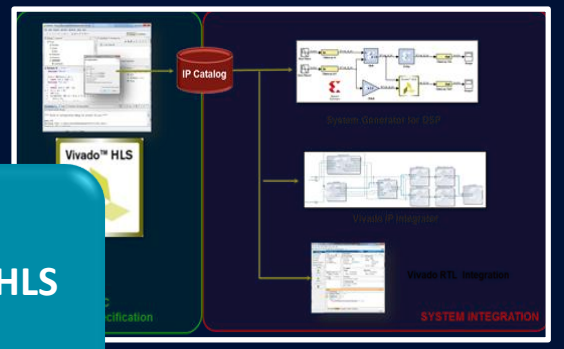
Any Media over Any Network



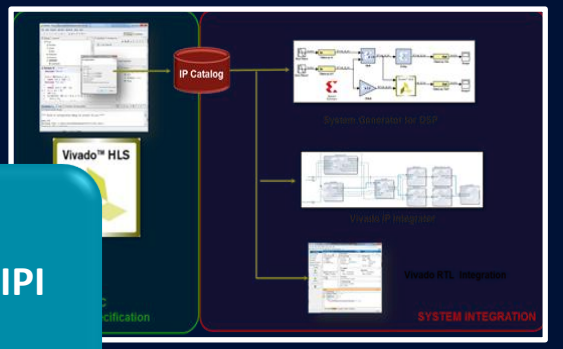
Tools and Methodologies to Accelerate BFV

PCIe
Video DMA

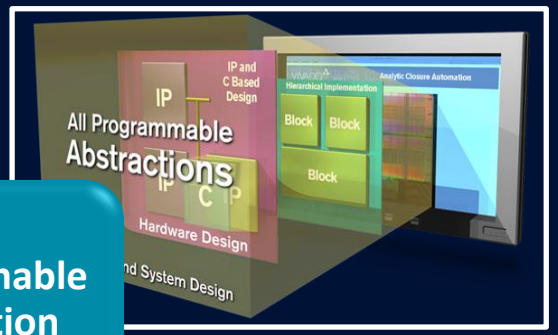
Vivado HLS



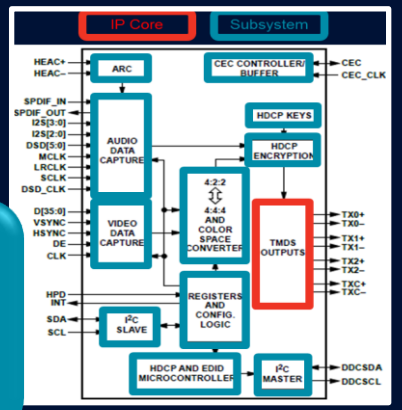
Vivado IPI



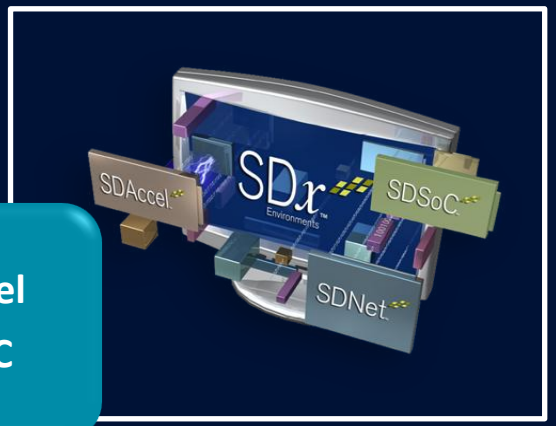
Programmable
Abstraction

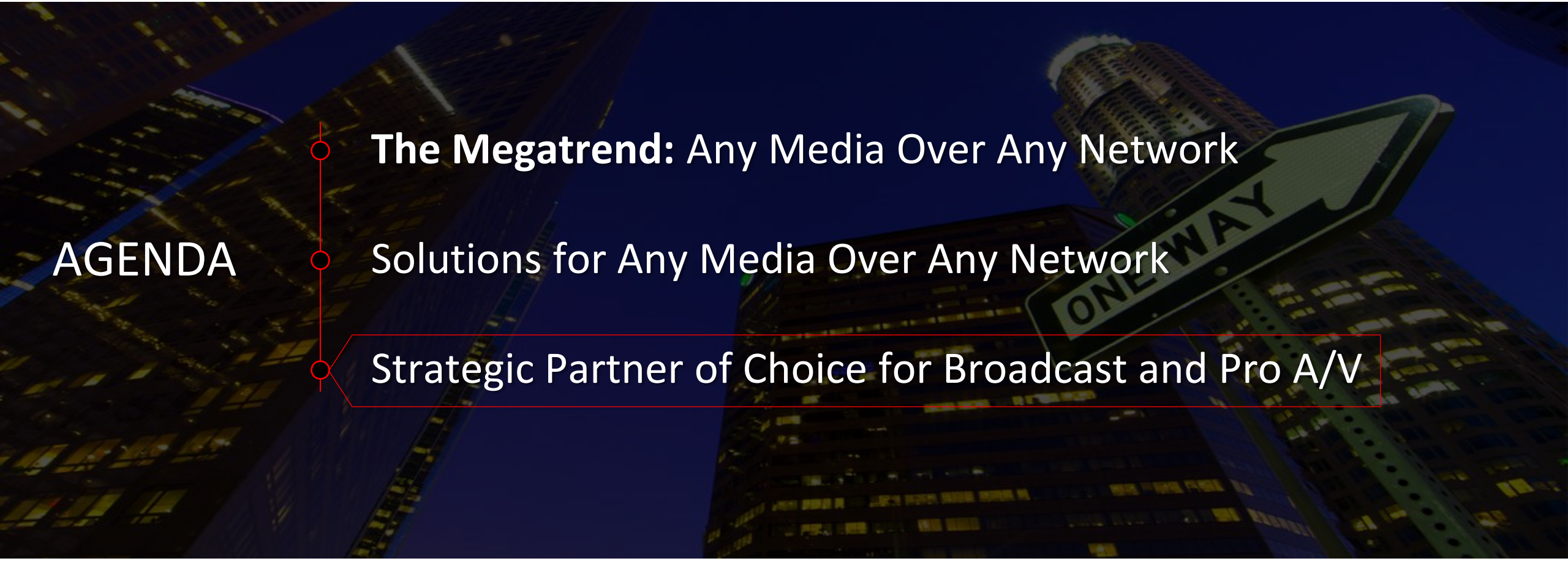


IP
Subsystems



SDAccel
SDSoC





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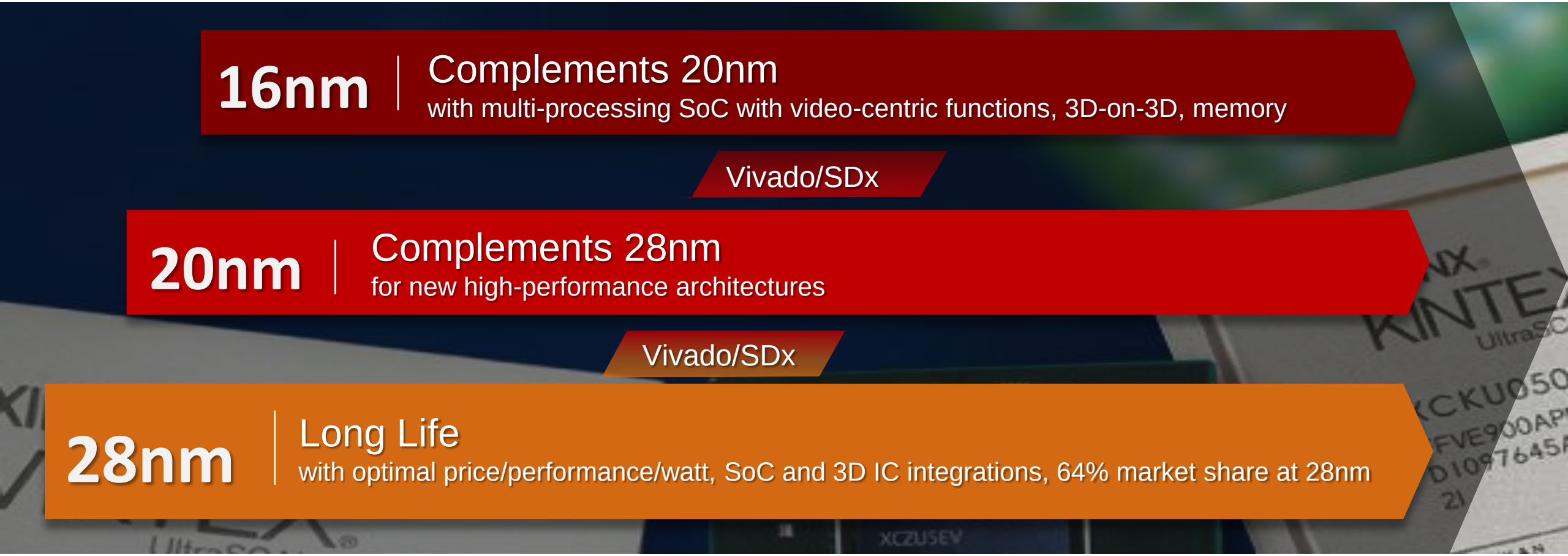
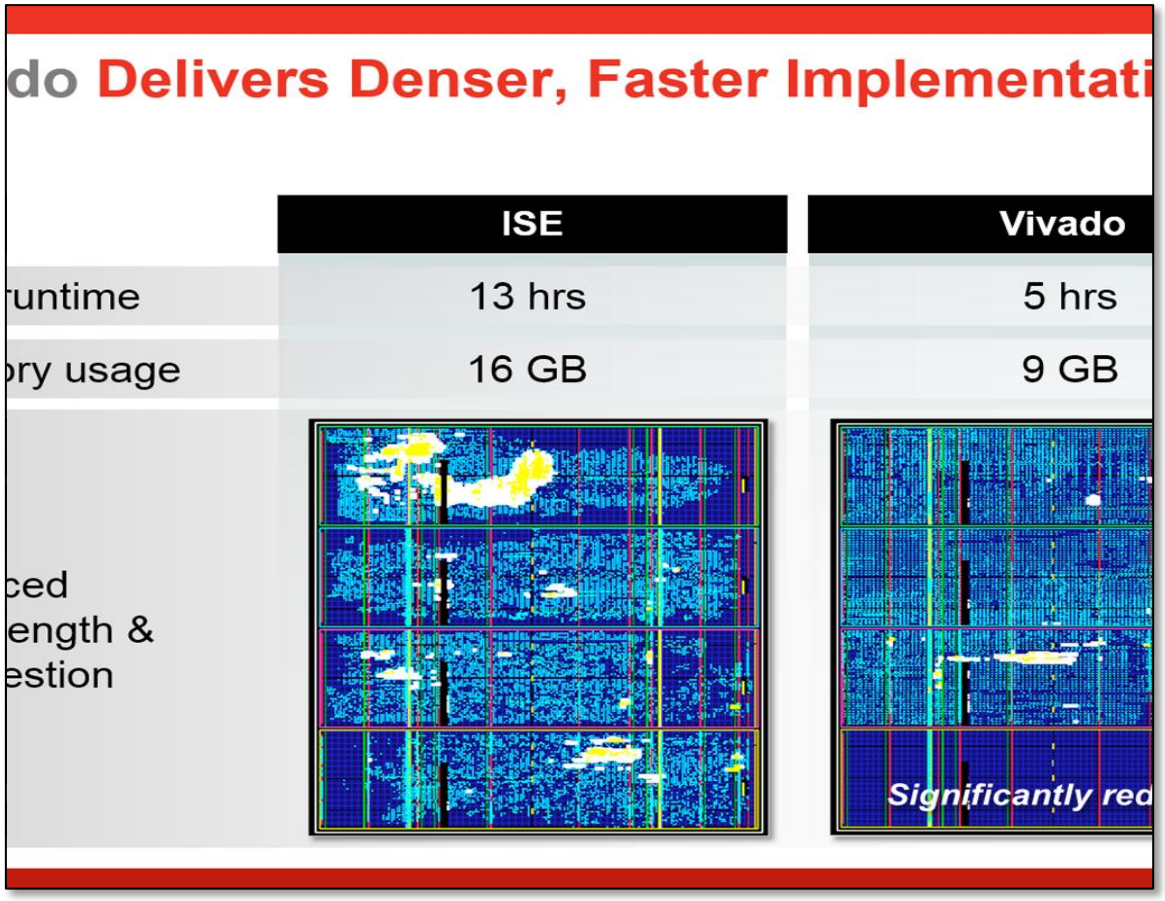
Proven Silicon Technology Leadership

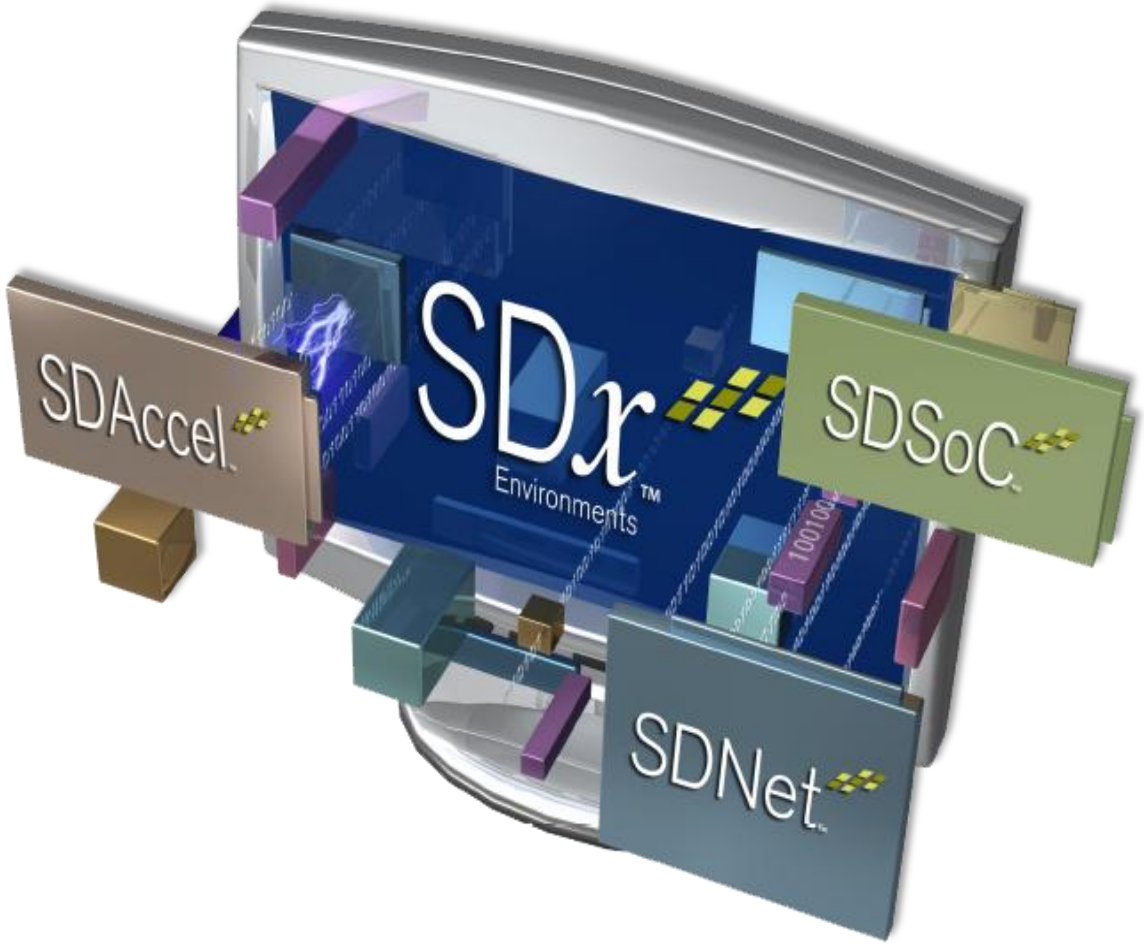


Concurrent Nodes with FPGAs, SoCs, and 3D ICs

Helping You Be More Productive



Accelerating Your Design Cycles



New SDx™ Development Environments For Software and Systems Engineers

SDx	Enables	To Replace	Why
SDSoC	**Zynq SoC and MPSoC**	**ARM-ASSPs, DSPs**	**100x performance gain**
SDAccel	X86 + PCIe FPGA (Kintex, Virtex)	GPUs, CPUs	25X performance / watt advantage
SDNet	FPGA only	NPUs	Performance, flexibility, security

- **SDSoC**
  - Ideal for software engineers and system architects with little to no FPGA expertise
  - Ideal at the architectural phase in considering / designing with Zynq
  - May benefit Zynq designs in progress however this needs to be qualified

From silicon to solutions…