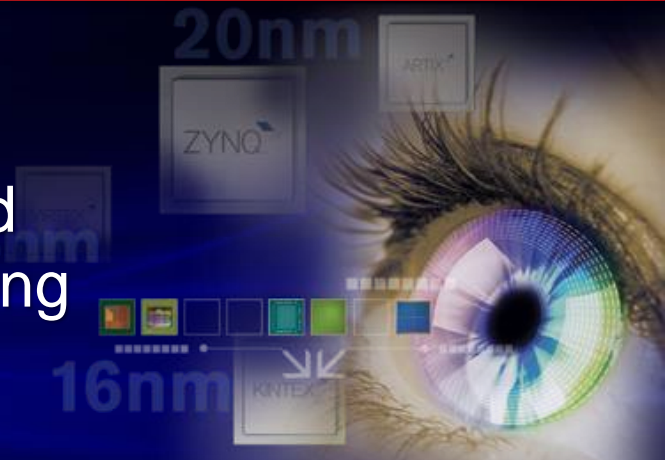


## Delivering a Generation Ahead

How to Efficiently Implement Flexible and Full-Featured Digital Radio Solutions Using All Programmable SoCs

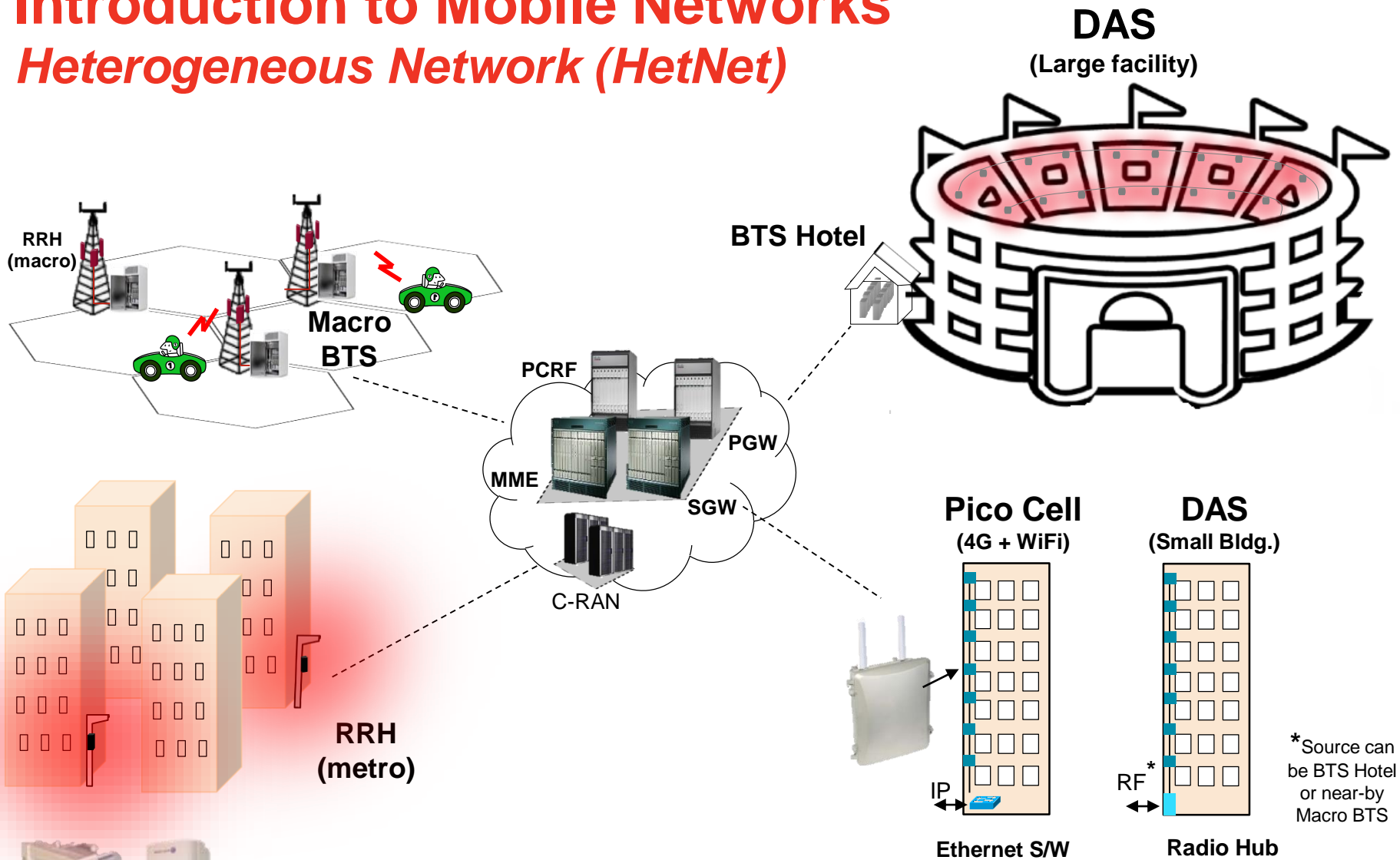


# Agenda

- Introduction to Mobile Network
- Introduction to Xilinx Solution
- Guidelines to Building Efficient Radio Designs
- Radio Design Examples
- Summary

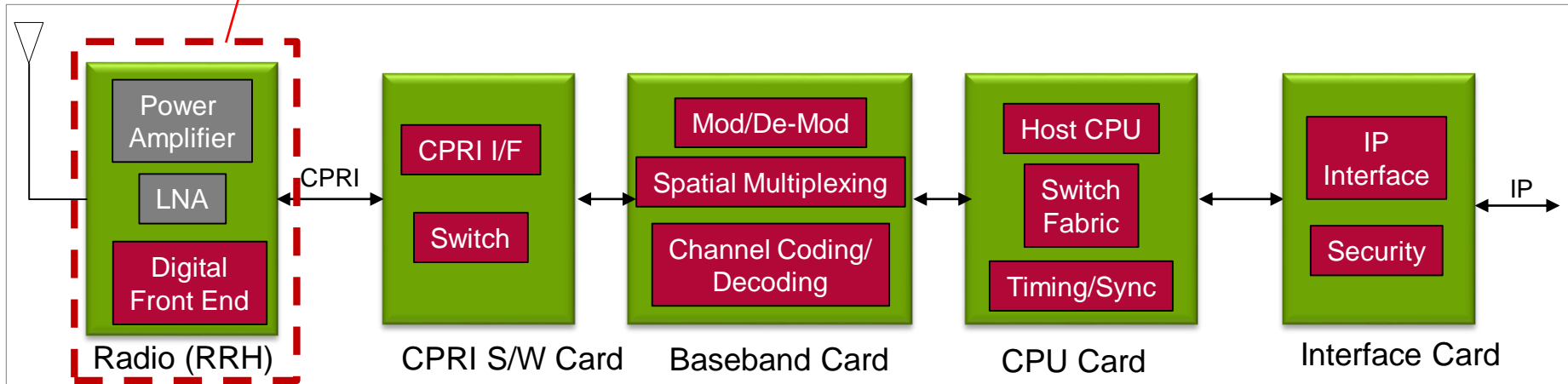
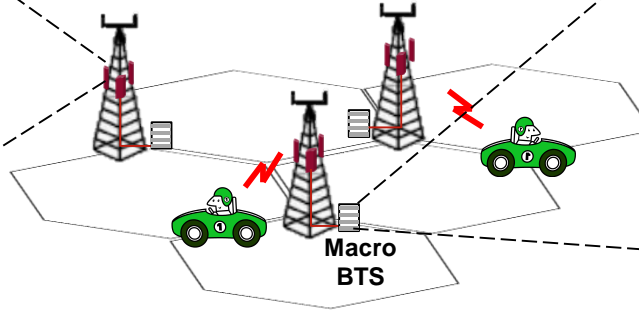
# Introduction to Mobile Networks

## Heterogeneous Network (HetNet)



MME – Mobility Management Entity  
 SGE – Serving Gateway  
 PGW – Packet Gateway  
 PCRF – Policy and Charging Rules Function

# Base-Station - Introduction

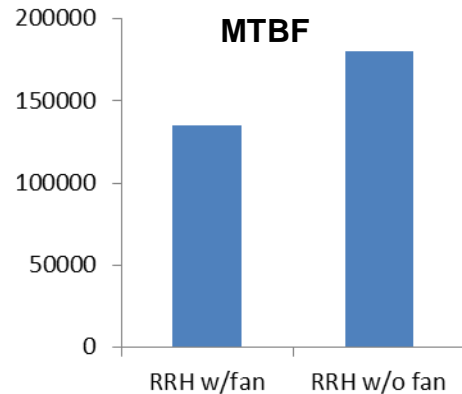


# RRH - Dynamics

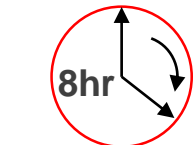
Harsh temperatures:  
-40C to +50C



Fan Increases OpEx



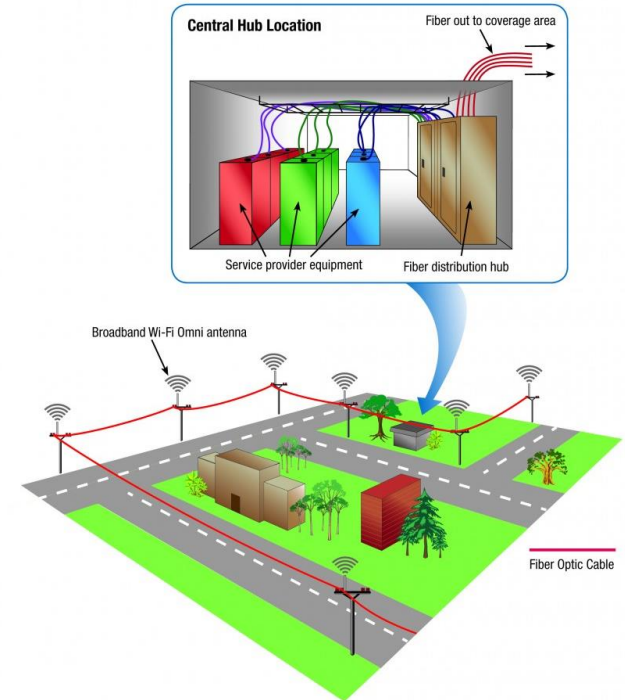
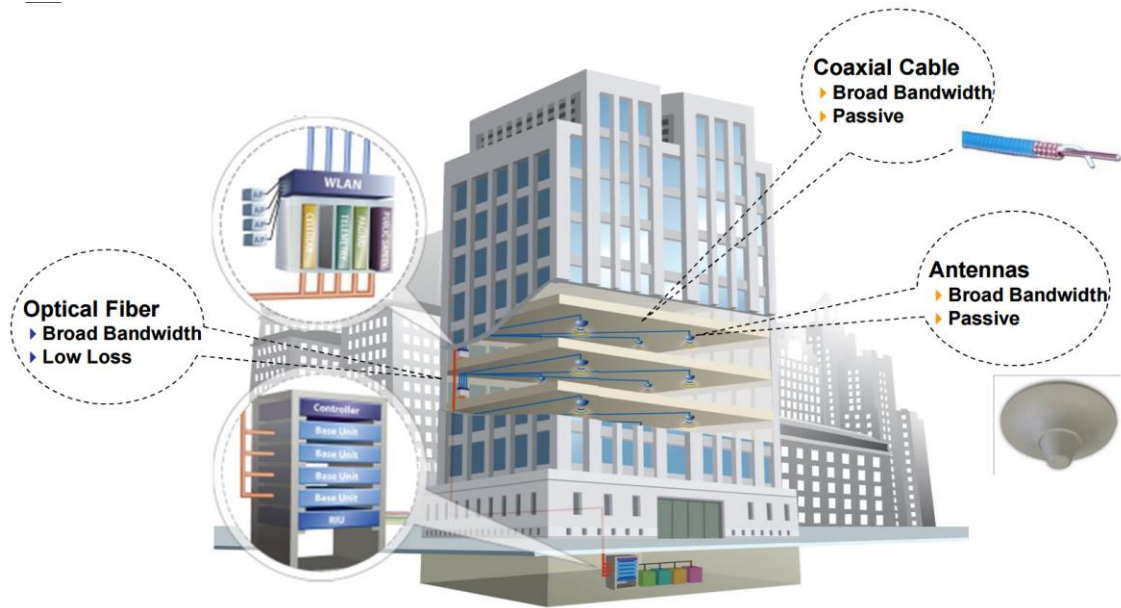
Limited Power – Solar & Wind



## Major Challenges

- Heat dissipation without using fan
- Reduce power consumption while supporting wider bandwidths
- Reduce foot print to lower rental cost by using bill boards etc.
- Reduce cost to make it attractive for emerging markets to do wide-scale deployment

# DAS - Dynamics

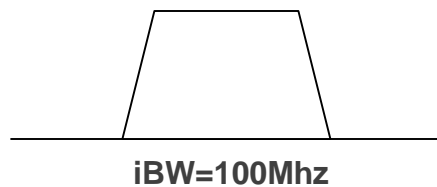


## Major Challenges

- Support different bands, bandwidths, protocols
- Ease of deployment
- Leverage existing Ethernet network
- Scalable to support different types and sizes of venues
- Small form-factor, low cost and high performance

# Multi-Band

- With rapid adoption of LTE, 2G and 3G are being re-farmed and replaced with LTE
  - Multi-band RRH to optimize CapEx and OpEx
  - To enable network sharing
  
- Pushing the limits of all the function blocks including DFE



Today



2yrs +

# Summary of Challenges

## ➤ Variety of radios for:

- Different bands
- Protocols
- Number of antennas
- Transmit power of PA
- Form-factor
- Techniques
- Support variety of network management software

## ➤ Power consumption and power dissipation

## ➤ Interface with variants of CPRI implementations done by OEMs

## ➤ Implementation approach

- ASSP: Support sub-set that has the highest volume → Leaves major gap in product offering
- ASIC: Support high volume mainstream deployments → Late entrant for emerging configurations e.g. multi-band



▪ RRH & Metro Cell



▪ AAS

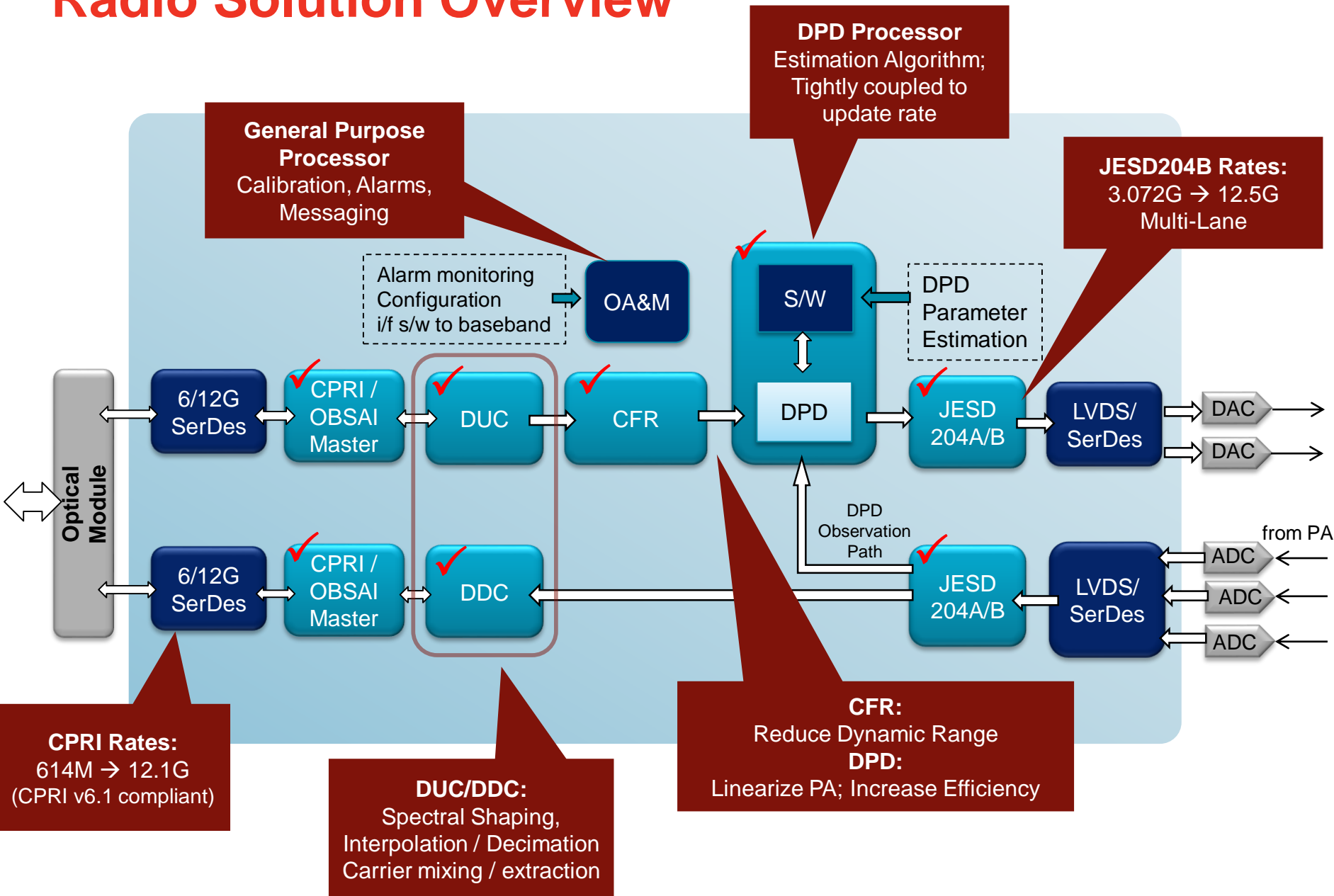


▪ Repeater/Relay



▪ DAS

# Radio Solution Overview



# Zynq-7000 All Programmable SoC

## ► Dual Core ARM(1GHz)+NEON

- Core 0 - O&M Processing
- Core 1 - DPD Engine

## ► DSP48

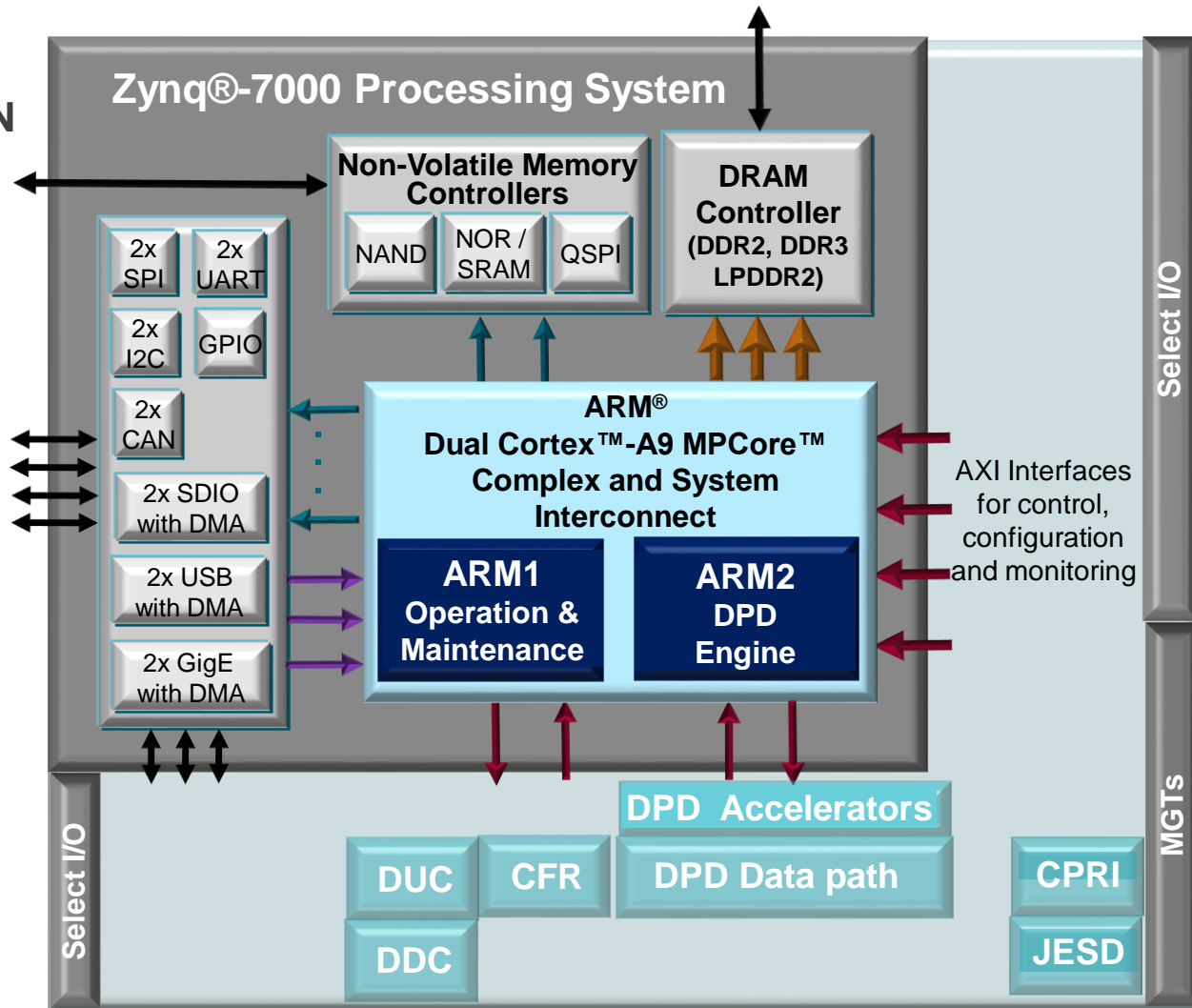
- Symmetric, Half-band filters
- DPD data path

## ► BRAM

- DPD capture buffer
- NCO memory

## ► SerDes

- CPRI
- JESD204B



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# Agenda

## ➤ Introduction to Mobile Network

## ➤ Introduction to Xilinx Solution

## ➤ Guidelines to Building Efficient Radio Designs

- High clock rate capabilities of 7 series FPGAs/SoCs
- Focus on functionality used for the data path of digital radio applications
- Review of design rules and fabric capabilities
- Additional benefits brought by 20/16nm UltraScale™ architecture

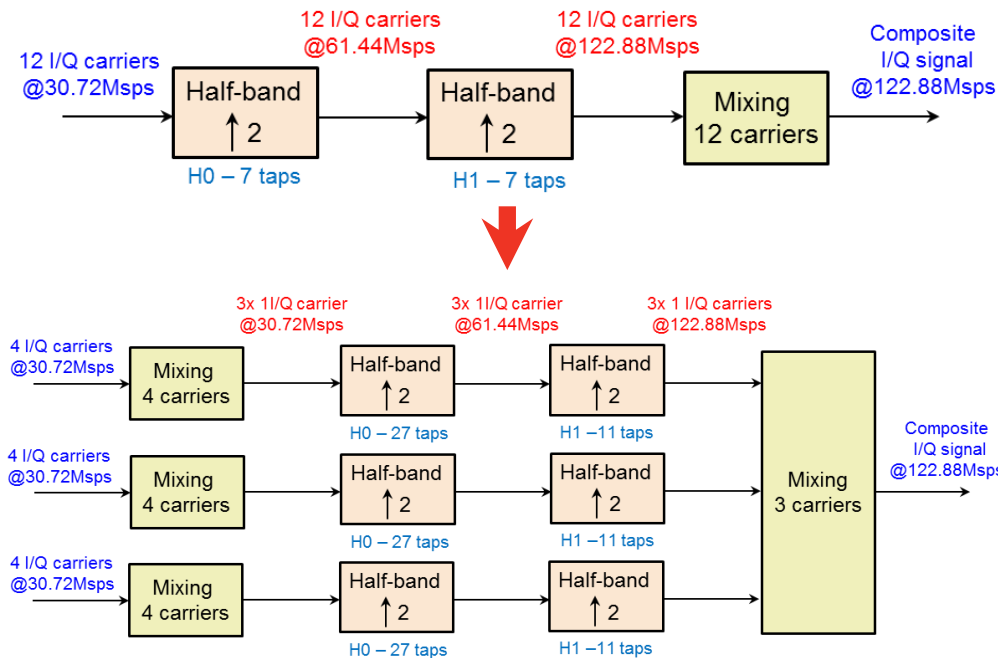
## ➤ Radio design Examples

- 500MHz clock rate on mid-speed grade 7 series device
- High utilization ratios
  - Almost 100% of the slice logic resource
  - More than 90% of the DSP48 resource and 70% of the BRAM resource

## ➤ Summary

# DFE Architecture and Algorithmic Optimization

- DUC/DDC complexity increases with iBW and number of carriers
  - Alternative architectures to optimize implementation
- Sub-band splitting and multi-stage carrier mixing/extraction



**50% LUT savings**

**60% DSP48 savings**

- Filter-bank architecture with FFT based implementation
- Filter architecture supporting multiple channel configurations
- Rasterized DDS

# Design Guidelines - Multi-cycle vs. Multi-channel

- **“Low” sampling rate operator implemented with a high clock rate**
  - Multi-cycle (or folded) architecture, exploiting the multiple clock cycles available per input sample
  - Multi-channel architecture, where multiple signals are time-multiplexed on input
- **Multi-channel implementation to be preferred**
  - Reduced logic utilization
  - Better timing performance achievable
- **Example (7 series): filtering of 16 data streams at 30.72Ms/s**

Design	Slices	LUT	FF	DSP4 8	Filter Characteristics
16-channel parallel filter	590	1660	2355	48	95-tap symmetric 491.52MHz clock rate
16x single channel multi-cycle filter	650	1760	3610	64	
16-channel parallel filter	450	1300	2015	41	81-tap symmetric 491.52MHz clock rate
16x single channel multi-cycle filter	650	1760	3610	64	

**Multi-channel architecture:  
5 to 25% LUT savings  
25 to 35% DSP48 savings**

# Design Guidelines - Pipelining

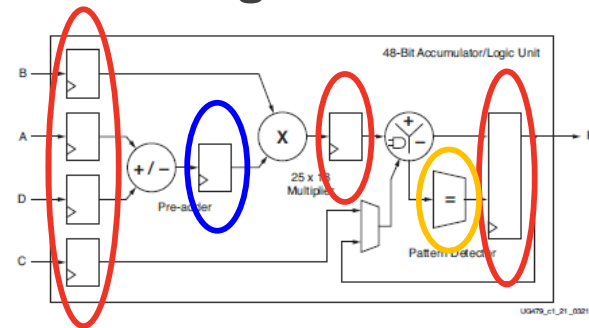
## ➤ Appropriate pipelining is key for high clock rate designs

- Abundant flip-flop resource in the FPGA fabric
- Hierarchical pipelined design

## ➤ Pipelining recommendations for fabric building blocks

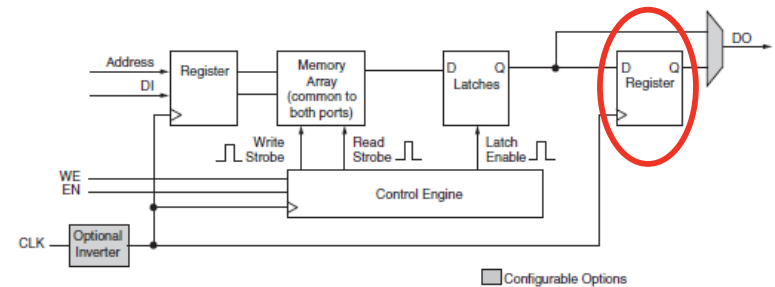
### – DSP48:

- To be fully pipelined
- Pattern detector can support > 500MHz



### – BRAM:

- To be fully pipelined
- Specific mode for power minimization
- Limit output data multiplexing



### – LUT Logic:

- Minimize the number of logic levels, and data routing paths
- One register every one or two LUT level

# Design Guidelines – LUT/SRL Compression

## ➤ Fabric feature enabling better packing

- Resource utilization optimization
- Limitation of routing congestion
- Up to 40% dynamic power reduction

## ➤ Applications in radio applications

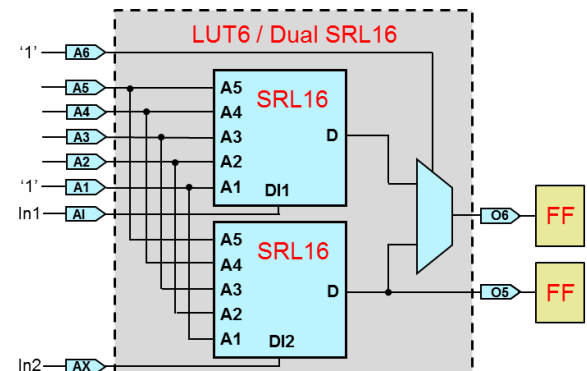
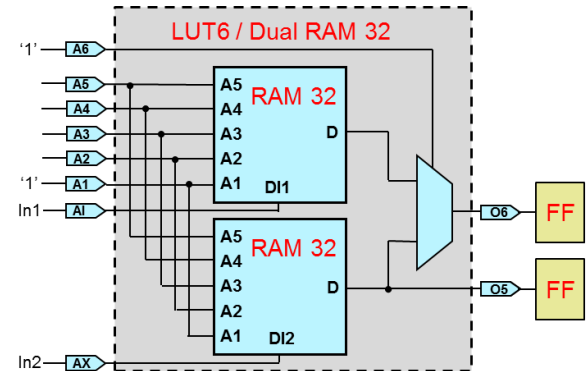
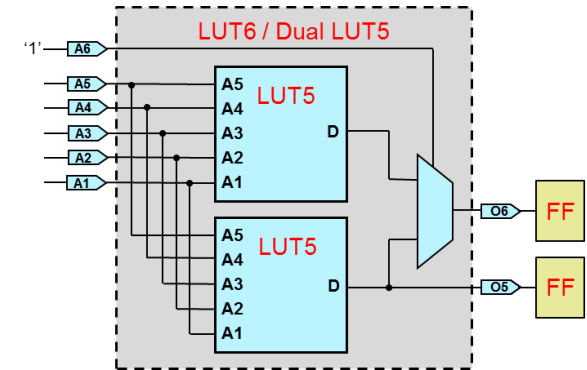
- Short delay lines
- Filter coefficient ROMs
- 2-input multiplexers

## ➤ Usage rules

- The two output FFs must be used
- To be applied to related logic

## ➤ Vivado® tool support

- Can also be controlled with HDL attributes



# Design Guidelines - Example

## ➤ Complex multiplier

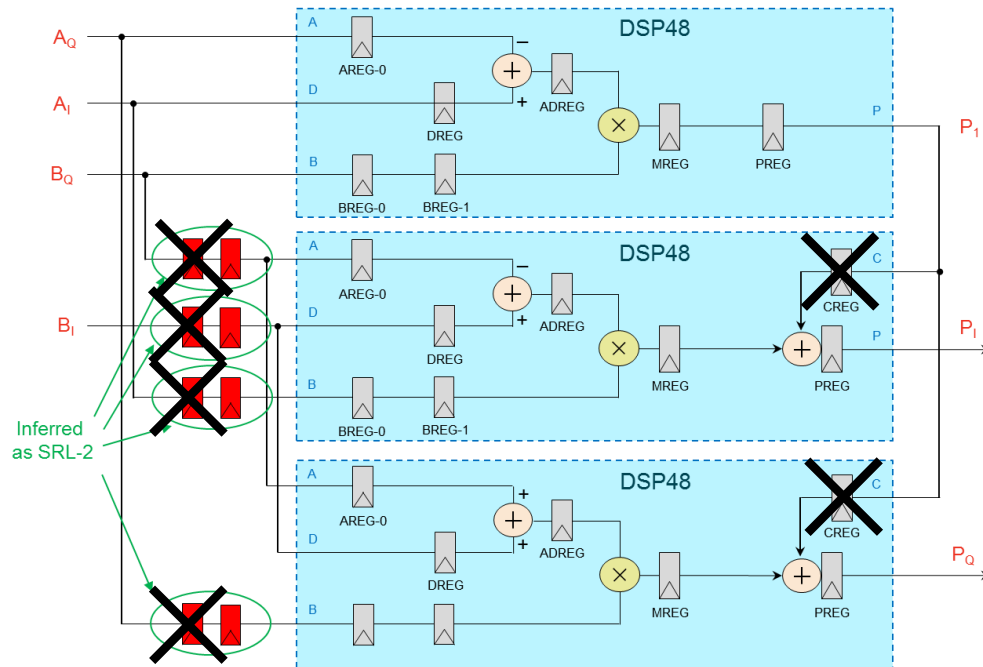
$$-(A+jB)*(C+jD) = (A*C-B*D)+j(A*D+B*C)$$

## ➤ Implementation with 3 DSP48s

- $P1 = D*(A-B)$
- $Re = P1 + A*(C-D)$
- $Im = P1 + B*(C+D)$

## ➤ Example

- 16-bit complex multiplier



Latency	LUT	FF	DSP48	Max Clock Speed (7-Series mid speed grade)
3 cycles	0	0	3	292 MHz
4 cycles	0	0	3	408 MHz
5 cycles	0	48	3	458 MHz
6 cycles	32	64	3	650 MHz

# Design Guidelines - Control Sets

## ➤ Clock management and distribution

- Limit the number of independent primary clocks.
- Synchronization between clock domains
- Place clocking elements close to the top level

## ➤ Reset strategy

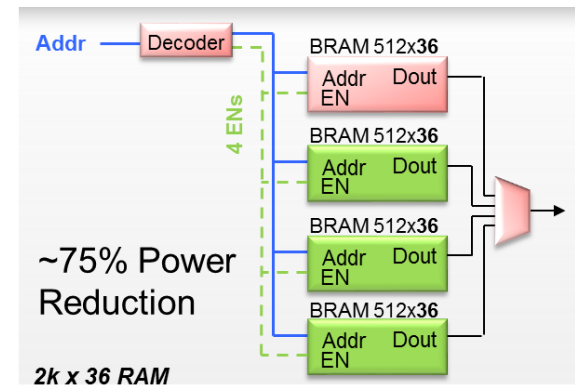
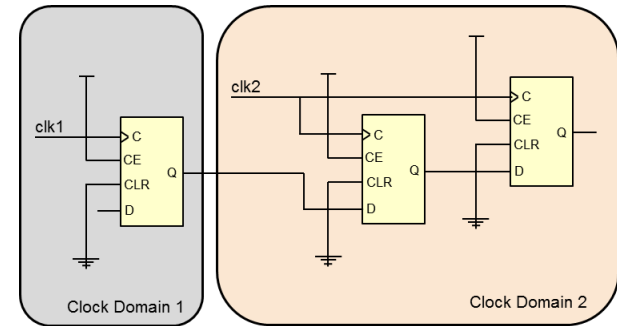
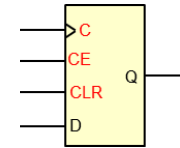
- Limit reset utilization as much as possible
- Synchronous reset to be preferred

## ➤ Clock enable strategy

- Limit usage of clock enables as far as possible
  - Multi-cycle implementations
  - Power reduction
- Pipelining to eliminate high fanout nets

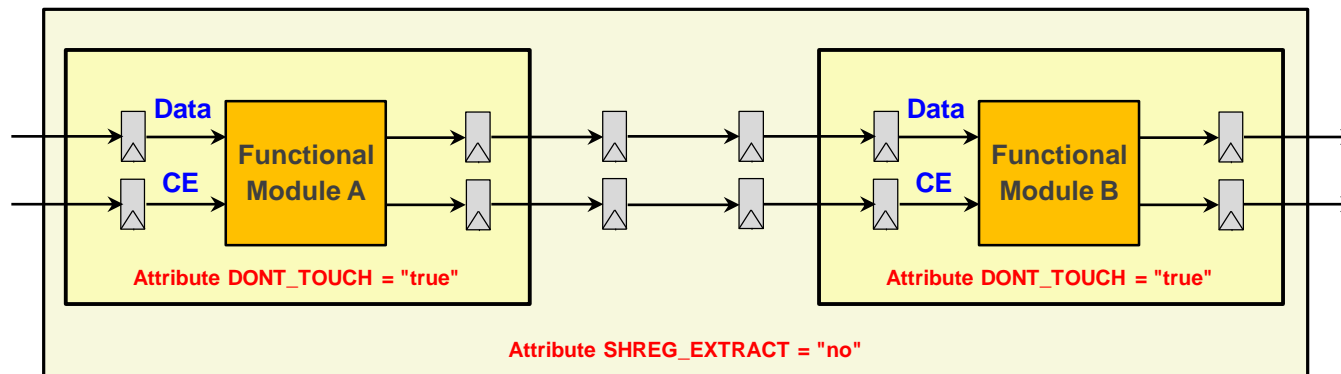
## ➤ UG949 for further details

- "UltraFast™ Design Methodology Guide"



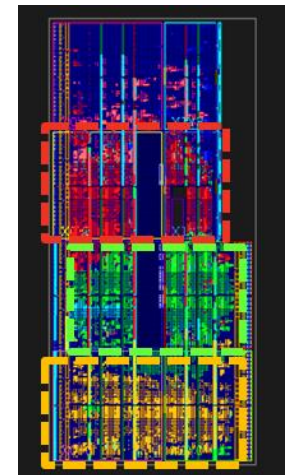
# Design Guidelines - Hierarchy

- Define an appropriate design hierarchy
  - Partitioning into appropriate functional blocks
  - Design hierarchy to gather related logic together
  - More efficient area grouping and logic compression
- Register hierarchical boundaries



- Area grouping
  - Shorter routing delays, better slice packing
  - Define a few "large" area groups
    - Each preferably lying within a single clock region

- Tool flow to preserve hierarchical P&R information

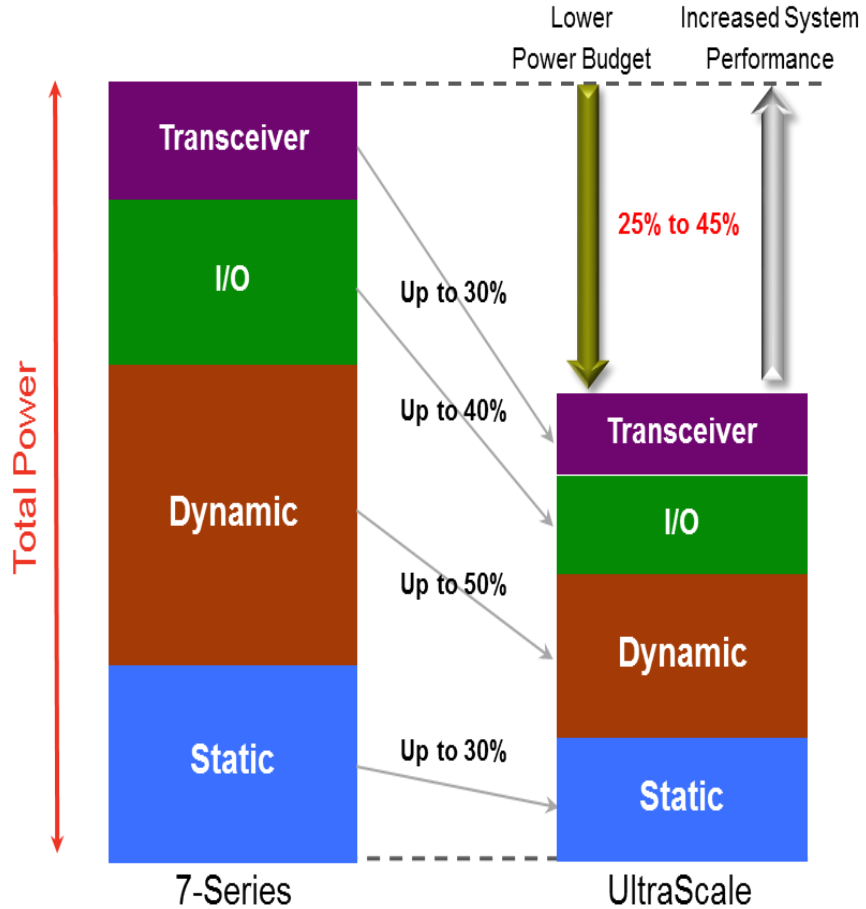


# Benefits of Xilinx UltraScale/UltraScale+ Architecture

## ➤ FPGA Fabric

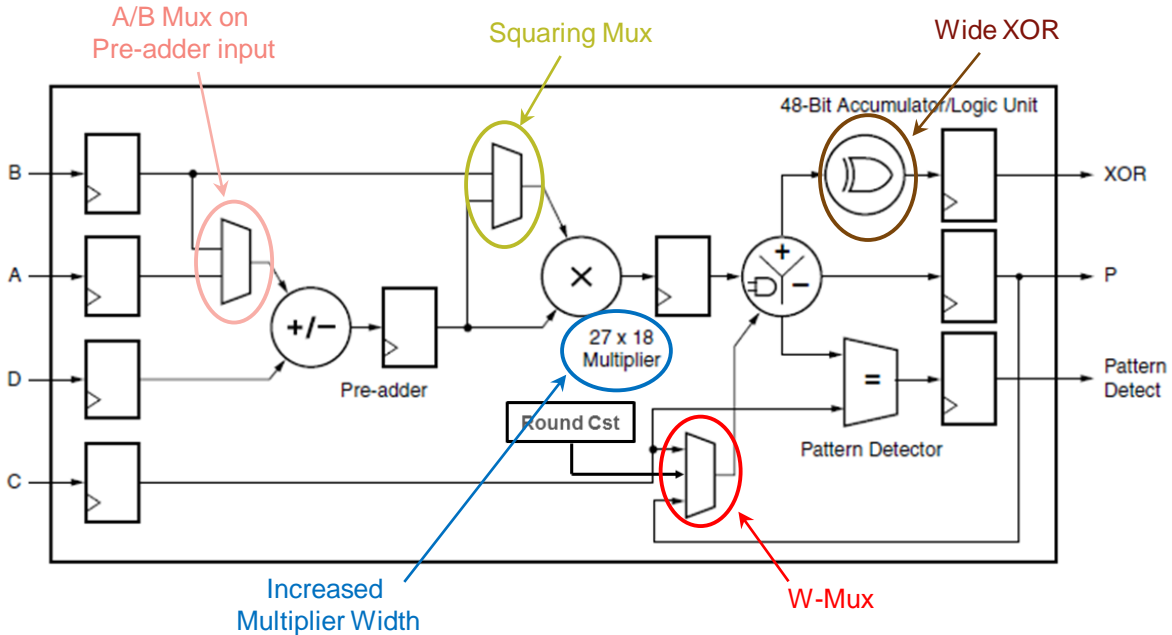
Feature	Benefit
Increased fabric resource	Higher integration Example: 8x8, 60MHz BW DFE: <ul style="list-style-type: none"> <li>• 2x 7K410T on 7 series technology</li> <li>• 1x XCKU60 on UltraScale technology</li> </ul>
DSP48/LUT and BRAM/LUT ratios	Better usage of logic resource for radio applications
Improved fabric performance	Support for +500MHz clock rate in slowest speed grade devices <ul style="list-style-type: none"> <li>• BRAMs still need to be used in specific mode</li> </ul>
Increased routing and control set resource	Reduced routing congestion Better design packing, i.e. higher LUT utilization
Increased SERDES speed	12.5Gb/s support on slowest speed grade

## ➤ Power



# Benefits of Xilinx UltraScale/UltraScale+ Architecture

## ➤ DSP48

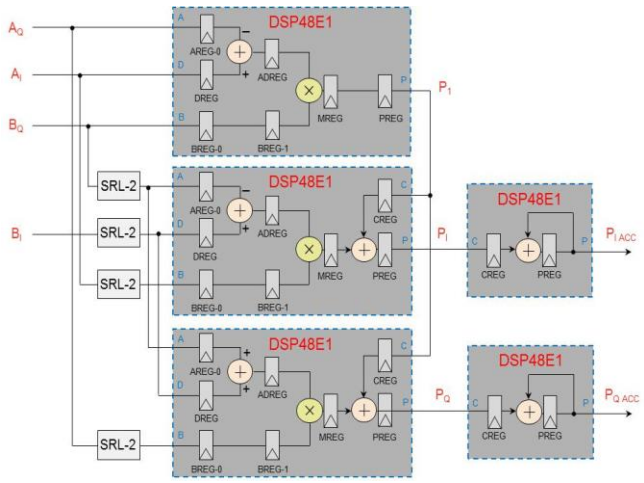


Feature	Benefit
W-Mux (4-input accumulator)	Improved implementation of filters and complex MACs 15-25% DSP48 resource savings in typical Radio designs
Increased Multiplier Width (27x18)	Improved floating point and fused data path support, e.g. HW acceleration for estimation of DPD coefficients
Pre-adder input Mux	Support for symmetric filters with up to 27-bit coefficients (limited to 18-bit on 7 series)
Squaring of pre-adder output	Support for sums of squared error terms
96-bit wide XOR	No use in DFE applications

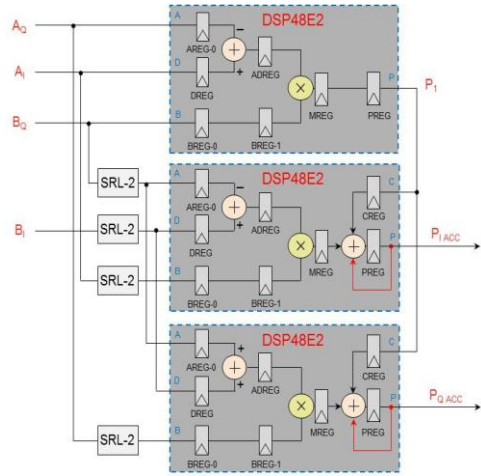
# Benefits of Xilinx UltraScale/UltraScale+ Architecture

## ➤ DSP48: W-Mux Benefits

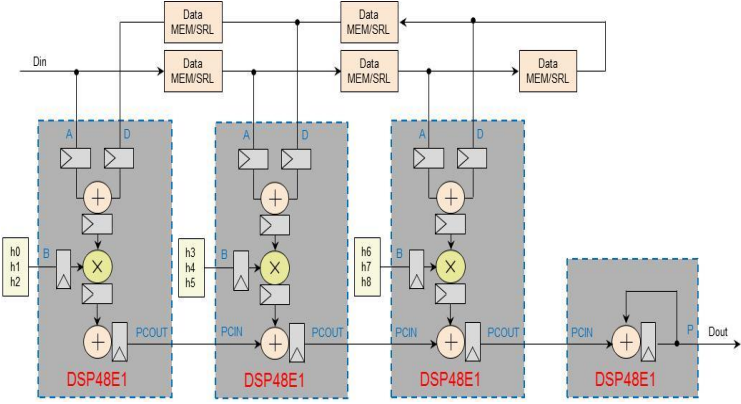
Complex MAC on 7 series



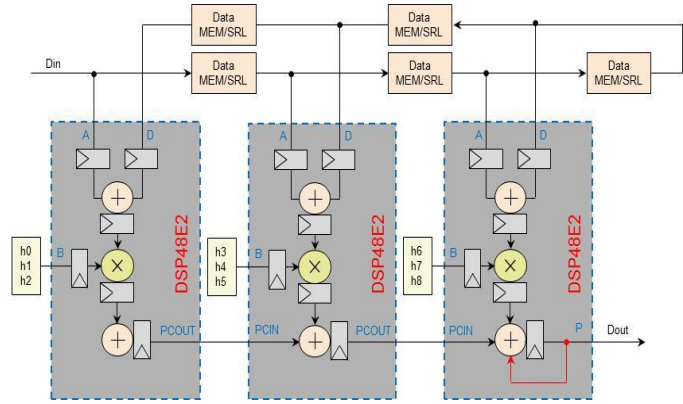
Complex MAC on UltraScale



Semi-parallel filter on 7 series



Semi-parallel filter on UltraScale



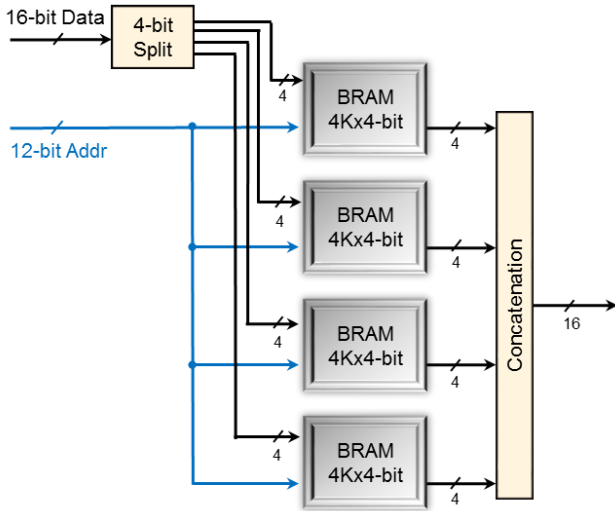
# Benefits of Xilinx UltraScale/UltraScale+ Architecture

## ► BRAM:

- Built-in cascade allows more efficient implementation of large memory blocks
  - Full speed achievable with significant power reduction
- Example: 4K depth x 16-bit memory with 2-cycle latency

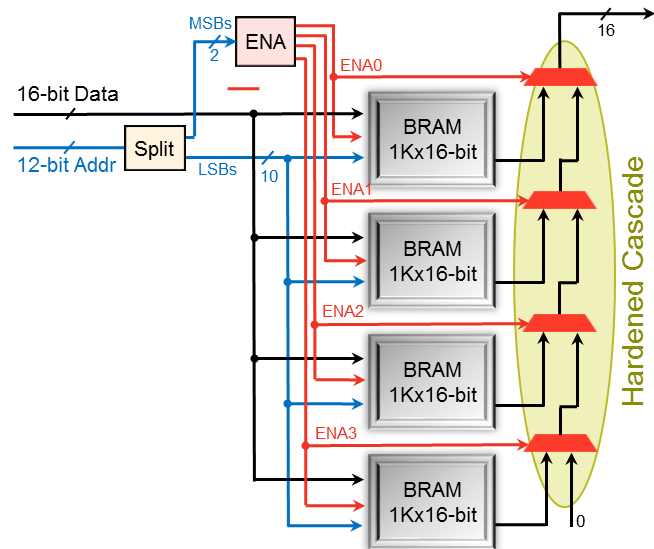
7 series implementation

Full speed but non optimal dynamic power



UltraScale implementation

Full speed and minimal dynamic power



## ► UltraRAM on UltraScale+:

- Dual port 4K x 72bit block RAM
- Efficient for DPD implementation (capture memory): ~60% BRAM savings

# High Clock Rate Design Examples

## ➤ Goal

- Demonstrate 500MHz clock rate Radio design with high utilization ratio

## ➤ Test Designs

- #1: High sample rate data path (sampling rate = clock rate)
- #2: Full transmitter data path Design

## ➤ Implementation

- Target device: 7K160T-2 (mid-speed grade)
  - 25350 slices (101400 LUTs, 202800 FFs), 600 DSP48s, 650 BRAMs 18K
- Clock rate: 1.9ns timing constraint (525 MHz)
- Vivado 2014.4
- VHDL code + System Generator + IP Catalog

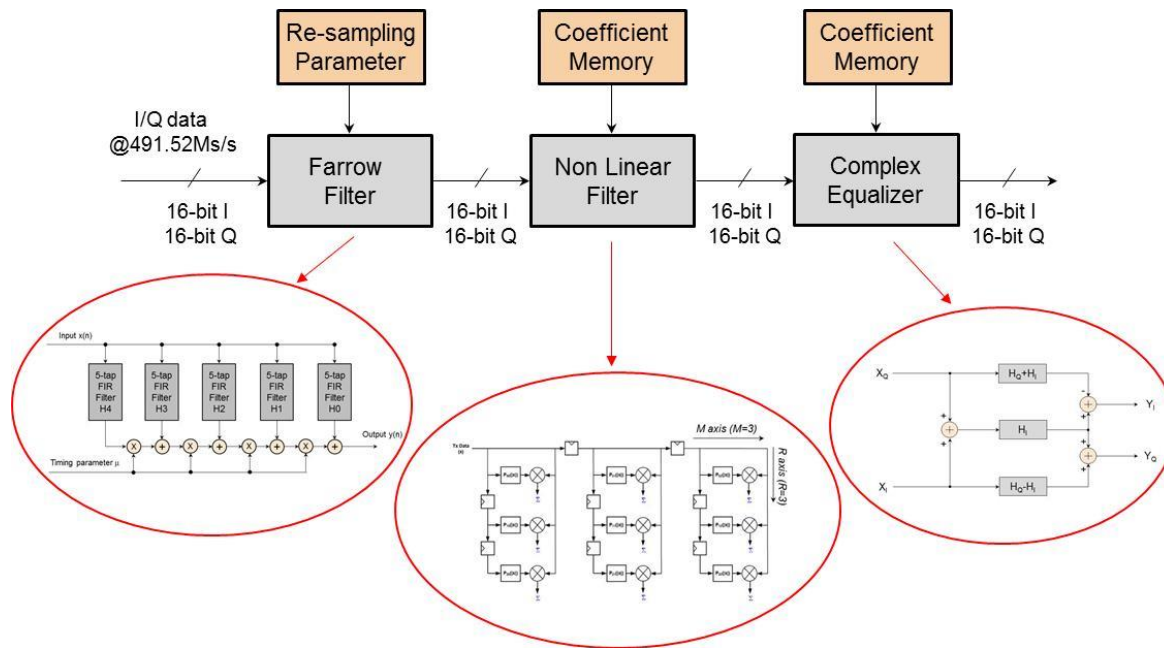
## ➤ WP445 for further details

- "Enabling High-Speed Radio Designs with Xilinx All Programmable FPGAs and SoCs"

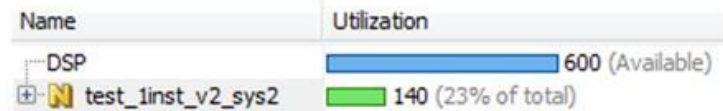
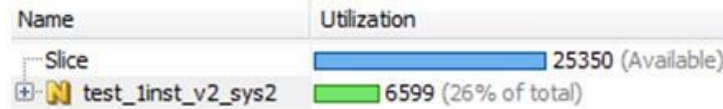
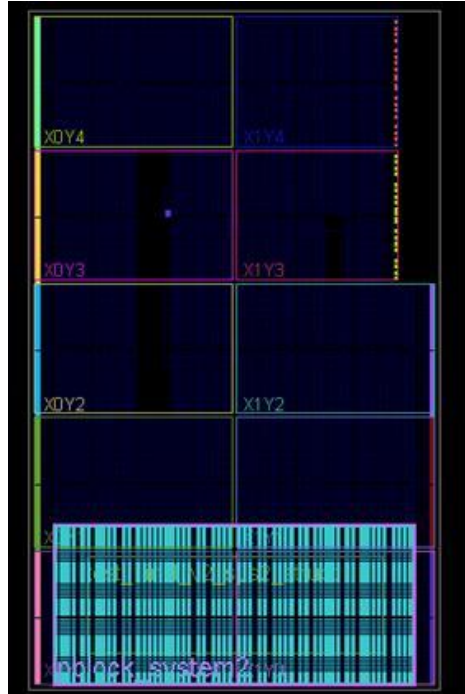
# Test Design #1 - Specifications

## ➤ High Sampling Rate Data Path

- Farrow filter, Non linear filter, Complex equalizer
- 491.52Ms/s sampling rate
- Single clock design
- Logic functionality added to the non-linear filter to achieve appropriate utilization ratios



# Test Design #1 - Results for a Single Instance

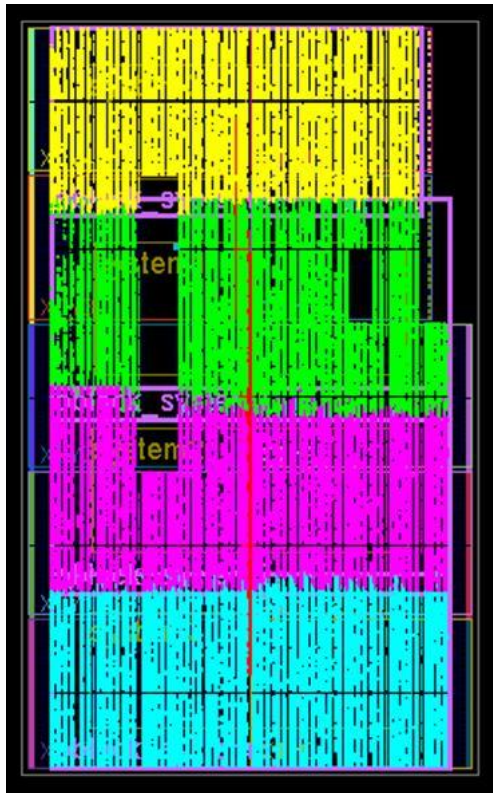


- Can support up to 530MHz
- Same timing performance can be achieved without an Area Group.
- Removing the Area Group constraint does not change the LUT and FF utilization, but the number of occupied slices increases by 48%

Resource	Slice	LUT	FF	DSP48	BRAM (18K)
1-instance design	6599	19740	42421	140	116
Area Group (PBLOCK)	6600	26400	52800	144	168
% of PBLOCK utilization	100%	75%	80%	97%	69%
7K160T device	25350	101400	202800	600	650
% of device utilization	26%	19%	21%	23%	18%

# Test Design #1 - Results for Four Instances

➤ Can support up to 515MHz



Name	Utilization
Slice	25350 (Available)
test_4inst_v2	25149 (99% of total)
test_4inst_v2_struct (test_4inst_v2_struct)	25149 (99% of total)
system2 (system2_a428cbb1eb)	6718 (27% of total)
system3 (system3_5c1b02cbd9)	6672 (26% of total)
system1 (system1_90c81529a0)	6160 (24% of total)
system0 (system0_9d75b0be3c)	6077 (24% of total)

Name	Utilization
DSP	600 (Available)
test_4inst_v2	560 (93% of total)
test_4inst_v2_struct (test_4inst_v2_struct)	560 (93% of total)
system0 (system0_9d75b0be3c)	140 (23% of total)
system1 (system1_90c81529a0)	140 (23% of total)
system2 (system2_a428cbb1eb)	140 (23% of total)
system3 (system3_5c1b02cbd9)	140 (23% of total)

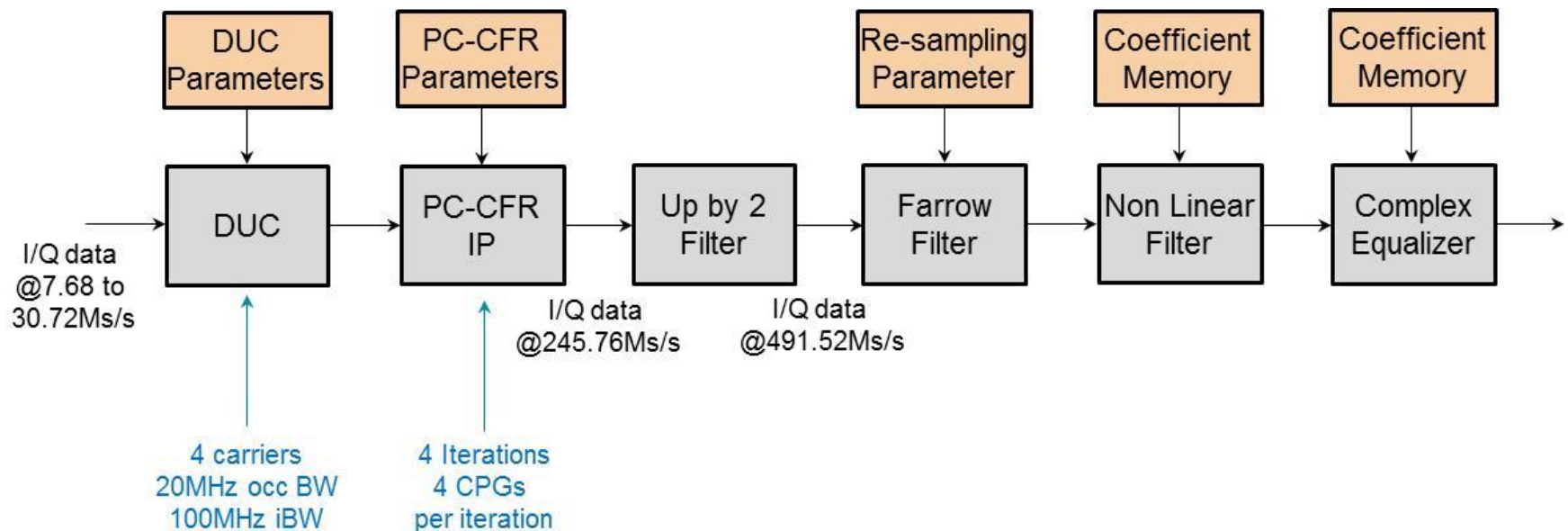
Name	Utilization
RAMB18	650 (Available)
test_4inst_v2	464 (71% of total)
test_4inst_v2_struct (test_4inst_v2_struct)	464 (71% of total)
system0 (system0_9d75b0be3c)	116 (18% of total)
system1 (system1_90c81529a0)	116 (18% of total)
system2 (system2_a428cbb1eb)	116 (18% of total)
system3 (system3_5c1b02cbd9)	116 (18% of total)

Resource	Slice	LUT	FF	DSP48	BRAM (18K)
4-instance design	25149	73682	161207	560	464
7K160T device	25350	101400	202800	600	650
% of device utilization	99%	73%	79%	93%	71%

# Test Design #2 - Specifications

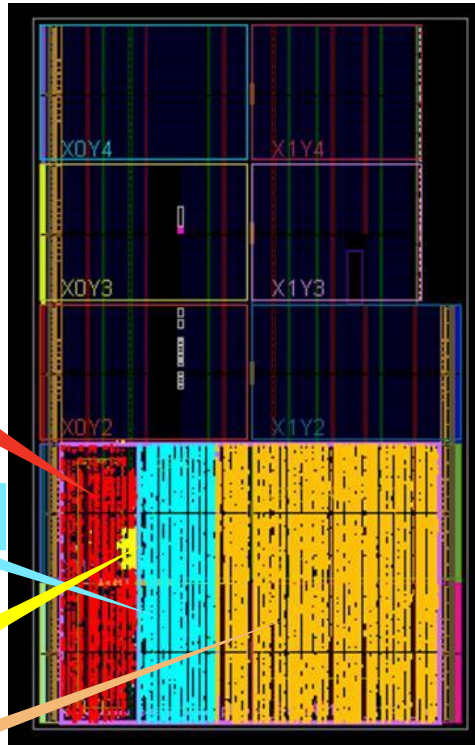
## ➤ Complete Radio Data Path Design

- DUC, CFR, farrow filter, non linear filter, complex equalizer
- Sampling rate ranging from 7.68Ms/s to 491.52Ms/s
- Dual clock design



# Test Design #2 - Results for a Single Instance

➤ Can support up to 505MHz



Name	Utilization
Slice	25350 (Available)
top_inst_0	10567 (42% of total)
proc491_v2_sys2_inst (proc491_v2_sys2_0)	6373 (25% of total)
pc_cfr_inst (pc_cfr_0)	2394 (9% of total)
duc_up245_inst (duc_up245_0)	1723 (7% of total)
duc_245up491_inst (duc_245up491_0)	123 (<1% of total)

Name	Utilization
DSP	600 (Available)
top_inst_0	195 (32% of total)
proc491_v2_sys2_inst (proc491_v2_sys2_0)	98 (16% of total)
duc_up245_inst (duc_up245_0)	51 (9% of total)
pc_cfr_inst (pc_cfr_0)	40 (7% of total)
duc_245up491_inst (duc_245up491_0)	6 (1% of total)

Name	Utilization
RAMB18	650 (Available)
top_inst_0	125 (19% of total)
proc491_v2_sys2_inst (proc491_v2_sys2_0)	116 (18% of total)
pc_cfr_inst (pc_cfr_0)	8 (1% of total)
duc_up245_inst (duc_up245_0)	1 (<1% of total)

Resource	Slice	LUT	FF	DSP48	BRAM (18K)
1-instance design	10567	30051	59890	195	125
Total Area Groups (PBLOCK)	11000	44000	88000	240	280
% of PBLOCK utilization	96%	69%	68%	81%	45%

# Summary

- Complexity of wireless systems keeps growing, requiring flexible radio solutions to support various bandwidth/power-level etc.
- Increased bandwidth and efficiency requirements pushing performance demands on radio applications
- Zynq and UltraScale/UltraScale+ device families offer optimal resource mix and scalability
- Techniques to build efficient radio designs with high clock rate and high device utilization ratios
- Achieving clock speeds of 500Mhz+ with 7 series and UltraScale/UltraScale+ devices

감사합니다.

정웅

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