

Introduction to Arria 10 FPGAs and SoCs

2015

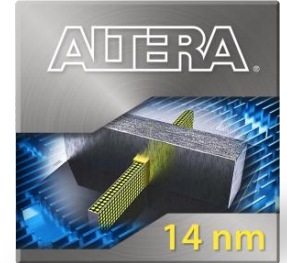


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Agenda

- **Optimized next generation portfolio**
- **Introduction to Altera's expanded 20 nm mid-range FPGA and SoC family**
- **Target applications for Arria 10 devices**
- **Detailed look at Arria 10 features**
- **Summary**



Arria® 10

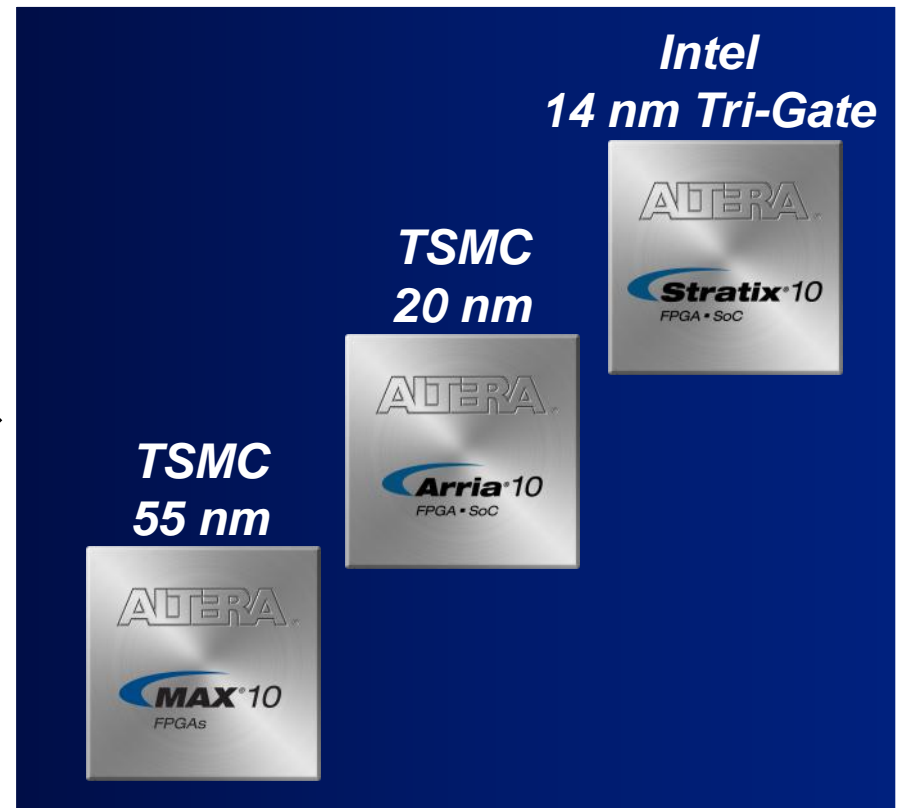
Extending Altera's Tailored Approach With 14 nm

Today's Portfolio



Single Node
28 nm

Generation 10 Portfolio



Multiple Nodes
14 nm, 20 nm, 55 nm

Altera's Next Generation Portfolio Goes to 10



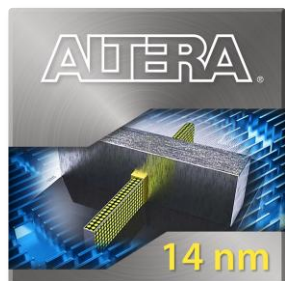
TSMC
20 nm Process

*High-Performance
Midrange
FPGAs & SoCs*

Arria® 10

- 60% faster vs. Arria V FPGAs, A speed grade faster than Stratix V FPGAs
- Up to 40% lower power vs. prior generation FPGAs
- 96 XCVRs, up to 28.3 Gbps

Pin Migration



Intel 14 nm
Tri-Gate Process

*High End
FPGAs
& SoCs*

Stratix® 10

- 2x performance of Stratix V FPGAs
- Up to 70% lower power vs. Stratix V FPGAs
- 4M+ LEs, Up to 56 Gbps XCVRs
- Up to 10 TFLOPs DSP performance

Altera's 10th Generation Portfolio – 2x More

**Up to 1 GHz
Core Performance**

**2x More
Bandwidth**

Bandwidth

Speed

*Arria 10: 28.3 Gbps
Stratix 10: 56 Gbps*

*Arria 10: 1.6x more than Arria V
Stratix 10: 2x more than Stratix V*



SoC

**“All-In” with
ARM for SoC**

*Power Saving
Innovations*

Power


*SoC across Density Range
>2x more Fabric Density*

**40-60%
Lower Power**

A 2x Leap Forward with 10th Generation

	Arria V GX/GT	Arria 10	Advantage
Density	500K LE	1,150K LE	2x
Multipliers	2,312	3,356	1.5x
Core Performance	300 MHz+	500 MHz+	1.6x
Transceiver Max Data Rate	10 Gbps	28.3 Gbps	2.8x
Memory Interface	1333 Mbps	2666 Mbps	2x
Total Power*	1.0	0.6	Up to 40% Lower
Cross Migration	No	Yes to Stratix 10	Yes

Arria 10 to Stratix 10 Migration

 **Arria[®] 10** 1st & Largest Devices

GX 1150

GT 1150

Three F1932 Packages
(NF45, SF45, UF45)

 **Stratix[®] 10**

1st Device

GX 2800

Notes:
Preliminary and subject to change






Applications: 10th Gen Mid-Range and High-End FPGAs

Arria® 10

Stratix® 10

More Power & Cost Sensitive

More Bandwidth Intensive

Applications	Industries	Applications
Up to 100G Line Cards, Nx100G Bridging & Aggregation	 <p>Wireline Communications</p>	200G/400G Line Cards, 200G/400G Bridging & Aggregation
40G/100G Muxponders/Transponders, ODU		200G/400G Muxponders/Transponders, ODU
10G GPON / NGPON		100G TM, Packet Processing, NGPON-2
Remote Radio Heads, Channel & Switch Cards	 <p>Wireless Communications</p>	High BW Remote Radio Heads
Mobile Backhaul		
Electro-Optical/IR	 <p>Defense</p>	Signal Intelligence
Guidance/Control		High-End Radar / Electronic Warfare / Secure Comms
Radar, Electronic Warfare, Secure Comms		
Pro AV / Videoconferencing	 <p>Broadcast</p>	High-End Broadcast Studio / Distribution
Studio Switcher / Server / Transport		Headend Encoder / EdgeQAM / CMAP
Flash Cache & Cloud Computing	 <p>Compute, Storage & Medical</p>	High- End Acceleration & Custom Servers, Diagnostic Imaging
Acceleration, Custom Servers, Diagnostic Imaging		

Arria 10 FPGAs and SoCs: Reinventing the Midrange

■ High performance and bandwidth

- Highest performance 20nm FPGAs
 - A speed grade faster than 20nm competition
- Over 3 Tbps of transceiver bandwidth
 - Up to 28.3G chip-to-chip, 17.4G backplane
- Over 850 Gbps of DDR4 bandwidth
- Over 1.2 Tbps of serial memory bandwidth
- Up to 1.5 TFLOPs floating-point DSP performance

■ Lowest power 20nm FPGAs and SOCs

- Up to 40% lower power than prior generation
- Comprehensive power reduction features

■ Highest level of integration in the midrange

- Up to 1.15 million logic elements and 53 Mb embedded memory
- Up to 96 transceivers
- Over 3.3K 18x19 multipliers
- Dual-core ARM Cortex A9 processor and subsystem

*Highest Performance 20nm FPGAs
Up to 40% Lower Power*



*Highest Performance and Lowest Power
for Midrange Applications*

ALTERA
MEASURABLE ADVANTAGE™

Arria 10 FPGAs and SoCs

Arria[®] 10

Up to 28.3G chip-to-chip, 17.4G backplane transceivers

High-performance logic fabric

M20K embedded memory blocks

Variable-precision DSP blocks

DDR4 Support up to 2666 Mbps

PCI Express[®] (PCIe[®]) Gen1, Gen2, Gen 3

Arria[®] 10 GX

Up to 17.4 Gbps XCVRs
Up to 1.15M LEs
Up to 53 Mbits Block RAM
Up to 768 IO

Arria[®] 10 GT

Up to 28.3 Gbps XCVRs
Up to 1.15M LEs
Up to 53 Mbits Block RAM
Up to 624 IO

Arria[®] 10 SX

Integrated ARM Cortex-A9
Processor
Up to 17.4 Gbps XCVRs
Up to 660K LEs
Up to 42 Mbits Block RAM
Up to 624 IO

NEW
28G-Capable
Family Members

Arria 10 FPGA Family Plan

	Core Resources								Interconnects		PLLs		Hard IP
	Device Name	Logic Elements (KLE)	M20K Blocks	M20K Bits (Mbits)	MLAB Counts	MLAB (Mbits)	18x19 Mults	Peak GFLOPs	Max IOs	Max XCVRs	fPLLs	IO PLLs	PCIe HIPs (x8)
GX	GX 160	160	440	9	1680	1	312	140	288	12	6	6	1
	GX 220	220	588	11	2932	1.8	382	172	288	12	6	6	1
	GX 270	270	750	15	3922	2.4	1660	747	384	24	8	8	2
	GX 320	320	891	17	4582	2.8	1970	887	384	24	8	8	2
	GX 480	480	1438	28	7046	4.3	2736	1231	492	36	12	12	2
	GX 570	570	1800	35	8153	5.0	3046	1371	696	48	16	16	2
	GX 660	660	2131	42	9260	5.7	3376	1519	696	48	16	16	2
	GX 900	900	2423	47	15017	9.2	3036	1366	768	96	32	16	4
	GX 1150	1150	2713	53	20774	12.7	3036	1366	768	96	32	16	4
GT	GT 900	900	2423	47	15017	9.2	3036	1366	624	96	32	16	4
	GT 1150	1150	2713	53	20774	12.7	3036	1366	624	96	32	16	4

Notes:
Preliminary and subject to change

Updated 4/10/2014

Arria 10 SoC Family Plan

	Core Resources								Interconnects		PLLs		Hard IP
	Device Name	Logic Elements (KLE)	M20K Blocks	M20K Bits (Mbits)	MLAB Counts	MLAB (Mbits)	18x19 Mults	Peak GFLOPs	Max IOs	Max XCVRs	fPLLs	IO PLLs	PCIe HIPs (x8)
Arria 10 SX SoC	SX 160	160	440	9	1680	1	312	140	288	12	6	6	1
	SX 220	220	583	11	2227	1.4	384	172	288	12	6	6	1
	SX 270	270	750	15	3537	2.2	1660	747	384	24	8	8	2
	SX 320	320	891	17	4673	2.9	1970	887	384	24	8	8	2
	SX 480	480	1438	28	7137	4.4	2736	1230	492	36	12	12	2
	SX 570	570	1800	35	8241	5.0	3046	1370	588	48	16	16	2
	SX 660	660	2131	42	9345	5.7	3376	1510	588	48	16	16	2

Notes:
Preliminary and subject to change

Updated 4/10/2014

Arria 10 GX and GT Package Plan (1 of 2)

Package Name	U484				F672				F780				F1152				F1152			
Size	19x19mm				27x27mm				29x29mm				35x35mm				35x35mm			
Package Code	U19				F27				F29				F34				F35			
XCVR Code	C (6 XCVRs)				E (12 channels)				E (12 channels)				H (24 channels)				H, K (24, 36 channels)			
GX FPGAs	GP IO	3V IO	LVDS Pairs	XCVR	GP IO	3V IO	LVDS Pairs	XCVR	GP IO	3V IO	LVDS Pairs	XCVR	GP IO	3V IO	LVDS Pairs	XCVR	GP IO	3V IO	LVDS Pairs	XCVR
GX 160	192	48	72	6	240	48	96	12	288	48	120	12								
GX 220	192	48	72	6	240	48	96	12	288	48	120	12								
GX 270					240	48	96	12	360	48	156	12	384	48	168	24	384	48	168	24
GX 320					240	48	96	12	360	48	156	12	384	48	168	24	384	48	168	24
GX 480									360	48	156	12	492	48	222	24	396	48	174	36
GX 570													492	48	222	24	396	48	174	36
GX 660													492	48	222	24	396	48	174	36
GX 900													504	0	252	24				
GX 1150													504	0	252	24				

Notes:

- a) Preliminary and subject to change
- b) GPIO counts include 3V IO and LVDS IO; GPIO that do not support 3V IO can support LVDS
- c) Each LVDS pair can be configured as either a differential input or as a differential output
- d) Up to 48 GPIO pins may be used for programming
- e) All packages are 1.0mm ball pitch except U484 which is 0.8mm ball pitch
- f) Packages of similar footprint (ie, the two F1152 columns shown in table above) may have different package form factors. Please consult package outlines.

 Pin migration across devices within family

Arria 10 GX and GT Package Plan (2 of 2)

Package Name	F1517				F1517				F1517				F1932				F1932				F1932			
Size	40x40mm				40x40mm				40x40mm				45x45mm				45x45mm				45x45mm			
Package Code	F40				F40				F40				F45				F45				F45			
XCVR Code	K (36 channels)				N (48 channels)				R (66 channels)				N (48 channels)				S (72 channels)				U (96 channels)			
GX FPGAs	GP IO	3V IO	LVDS Pairs	XCVR	GP IO	3V IO	LVDS Pairs	XCVR	GP IO	3V IO	LVDS Pairs	XCVR	GP IO	3V IO	LVDS Pairs	XCVR	GP IO	3V IO	LVDS Pairs	XCVR	GP IO	3V IO	LVDS Pairs	XCVR
GX 570	696	96	324	36	588	48	270	48	Pin Migration to Stratix 10 Devices															
GX 660	696	96	324	36	588	48	270	48																
GX 900					600	0	300	48	342	0	154	66	768	0	384	48	624	0	312	72	480	0	240	96
GX 1150					600	0	300	48	342	0	154	66	768	0	384	48	624	0	312	72	480	0	240	96
GT FPGAs																								
GT 900					600	0	300	48						624	0	312	72	480	0	240	96			
GT 1150					600	0	300	48						624	0	312	72	480	0	240	96			

Notes:

- a) Preliminary and subject to change
- b) GPIO counts include 3V IO and LVDS IO; GPIO that do not support 3V IO can support LVDS
- c) Each LVDS pair can be configured as either a differential input or as a differential output
- d) Up to 48 GPIO pins may be used for programming
- e) All packages are 1.0mm ball pitch except U484 which is 0.8mm ball pitch
- f) Packages of similar footprint (ie, the two F1517 columns shown in table above) may have different package form factors. Please consult package outlines.




Arria 10 SoC Package Plan: Small Form Factor (1 of 2)

Package Type and Size	U484				F672				F780			
Size	19x19mm				27x27mm				29x29mm			
Package Code	U19				F27				F29			
XCVR Code	C (6 XCVRs)				E (12 XCVRs)				E (12 XCVRs)			
Device	IO	XCVR	3V	LVDS	IO	XCVR	3V	LVDS	IO	XCVR	3V	LVDS
10AX016	192	6	48	72	240	12	48	96	288	12	48	120
10AX022	192	6	48	72	240	12	48	96	288	12	48	120
10AX027					240	12	48	96	360	12	48	156
10AX032					240	12	48	96	360	12	48	156
10AX048									360	12	48	156

Notes:

- (1) All packages are ball grid arrays with 1.0mm pitch, except for U19 (U484) which is 0.8mm pitch.
- (2) High-Voltage I/O pins are used for 3.3V and 2.5V interfacing.
- (3) Each LVDS pair can be configured either as a differential input, or as a differential output.
- (4) High-Voltage I/O pins and LVDS Pairs are included in the General Purpose I/O count. Transceivers are counted separately.
- (5) Each package column offers pin migration (common circuit board footprint) for all devices in the column.

 Pin migration across devices within family



Arria 10 SoC Package Plan: IO & XCVR OPTIMIZED (2 of 2)

Package Type and Size	F1152				F1152				F1517				F1517			
Size	35x35mm				35x35mm				40x40mm				40x40mm			
Package Code	F34				F35				F40				F40			
XCVR Code	H (24 XCVRs)				H, K (24, 36 XCVRs)				K (36 XCVRs)				N (48 XCVRs)			
Device	IO	XCVR	3V	LVDS	IO	XCVR	3V	LVDS	IO	XCVR	3V	LVDS	IO	XCVR	3V	LVDS
10AX027	384	24	48	168	384	24	48	168								
10AX032	384	24	48	168	384	24	48	168								
10AX048	492	24	48	222	396	36	48	174								
10AX057	492	24	48	222	396	36	48	174	696	36	48	324	588	48	48	270
10AX066	492	24	48	222	396	36	48	174	696	36	48	324	588	48	48	270

Notes:

- (1) All packages are ball grid arrays with 1.0mm pitch, except for U19 (U484) which is 0.8mm pitch.
- (2) High-Voltage I/O pins are used for 3.3V and 2.5V interfacing.
- (3) Each LVDS pair can be configured either as a differential input, or as a differential output.
- (4) High-Voltage I/O pins and LVDS Pairs are included in the General Purpose I/O count. Transceivers are counted separately.
- (5) Each package column offers pin migration (common circuit board footprint) for all devices in the column.
- (6) F40 package with 36 transceivers only supports HPS with 72-bit DDR support, all other packages support HPS with up to 40-bit DDR Support

 Pin migration across devices within family





Select Arria 10 Target Applications



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Arria 10 Applications Example: OTN 100G Transponder

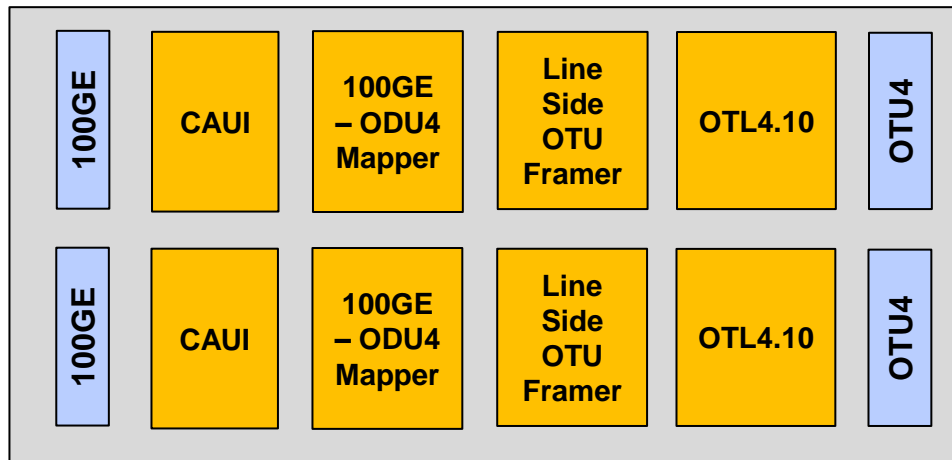
Design Details

FPGA Core

490 KLE 260 MHz main clock
2.6 Mbits RAM

IO Interfaces

20 XCVRs @ 11.18 Gbps
20 XCVRs @ 11.3 Gbps
2 XCVRs @ 2.5 Gbps



Conditions: 100C Max

Arria 10 Product Advantages

- Robust protocol support for OTU4, GE
- Low power transceivers
- XCVR support up to 28.3 Gbps
- Comprehensive power reduction feature set

	Stratix V	Arria 10	Improvement
Power	31.4W	18.9W	40%

Arria 10 FPGA Delivers 40% Power Reduction vs. Prior Generation

Arria 10 Applications Example: Mobile Backhaul

Design Details

FPGA Core

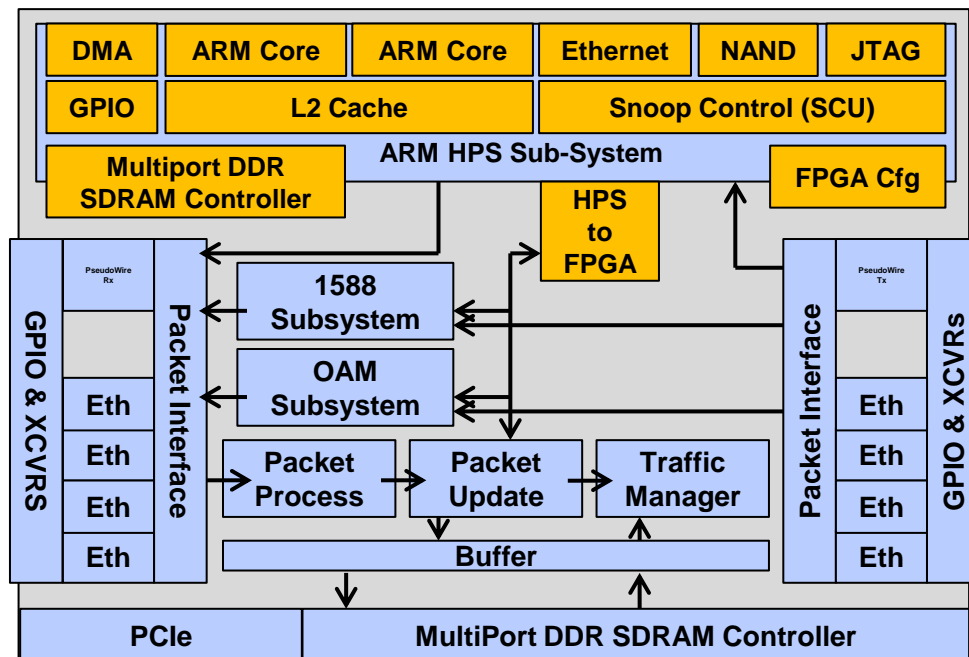
400 KLE	500 18x18 mults
12.3 Mbits RAM	250 Mhz main clock

IO Interfaces

8 XCVRs @ 10.3 Gbps
3x DDR3 x32 @533 Mhz

Arria 10 Product Advantages

- Flexibility vs. ASSP solutions
- Single-chip integration of processor and external switch to reduce power and space
- In-field upgradability
- Comprehensive power reduction feature set



Conditions: 100C Max

	Arria V + CPU + Switch	Arria 10 SoC	Improvement
Power	26.2W	13.7W	47.7%

Lowest Power Single-Chip Implementation Supporting In-Field Hardware Upgrades

Arria 10 Applications Example: Broadcast UDX

Design Details

FPGA Core

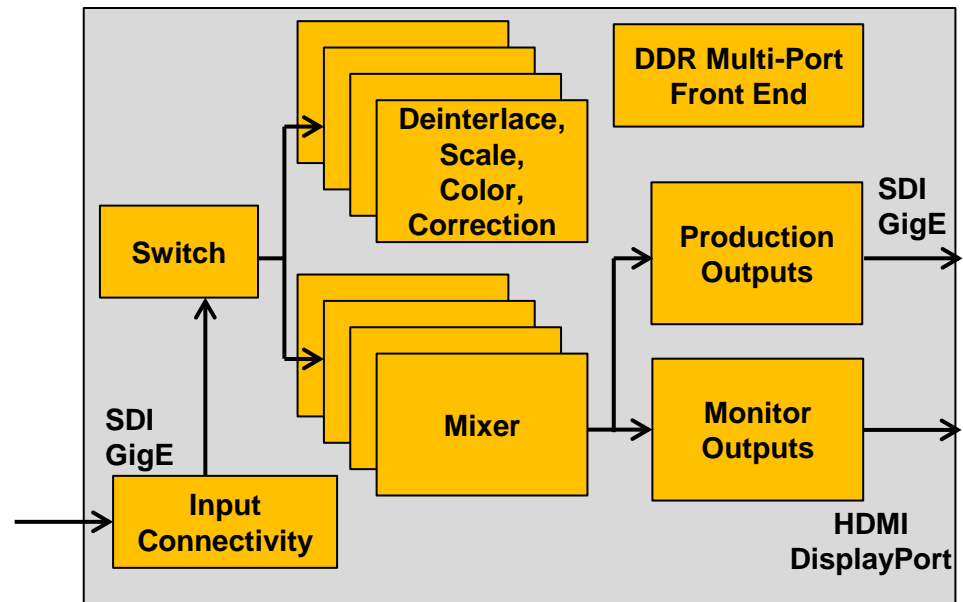
250 KLE	60 18x18 mults
14.7 Mbits RAM	200 Mhz main clock

IO Interfaces

8 XCVRs @ 3 Gbps
4 XCVRs @ 5.4 Gbps
2x DDR3x72 @533 Mhz

Arria 10 Product Advantages

- DDR4 support up to 2.6 Gbps
- Protocol support for SDI, DisplayPort, HDMI & GE
- RAM widths optimized for video data
- Up to 96 XCVR channels for scalable switching



Conditions: 100C Max

	Stratix V	Arria 10	Improvement
Power	14.2W	8.5W	40%

Lowest Power Single-Chip Implementation for Wide Variety Of Switching Applications



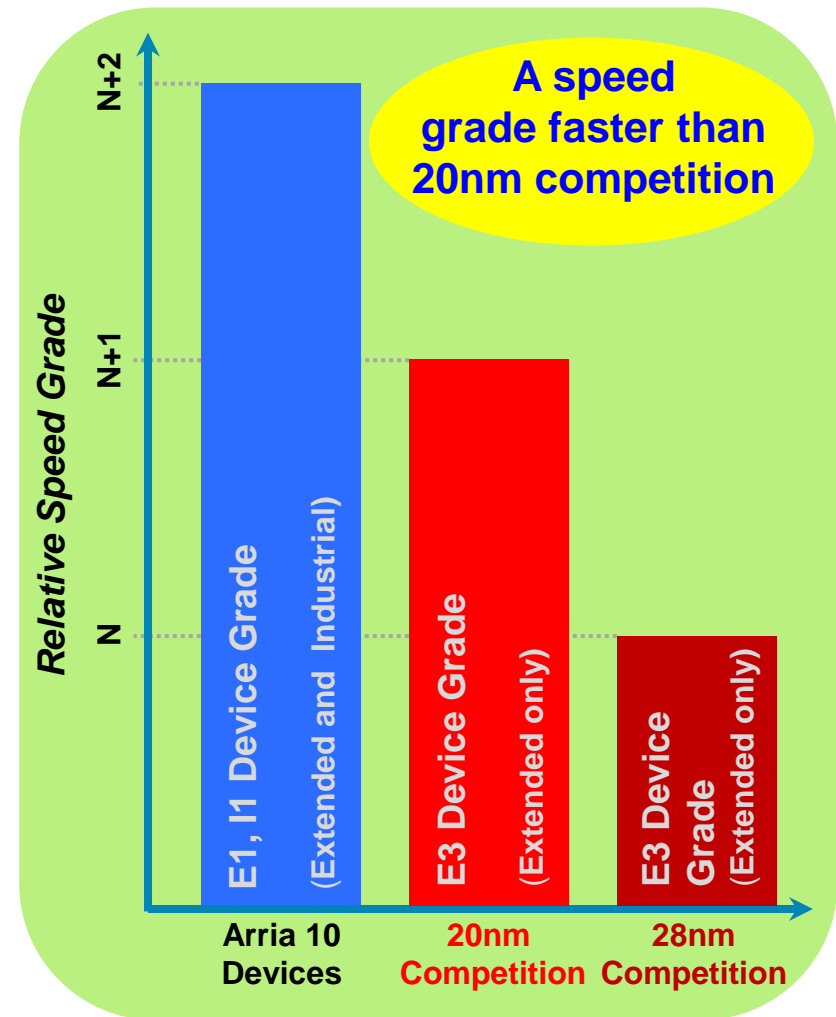
Arria 10 Performance and Power



Arria 10 Devices: Highest Performance 20nm FPGAs/SoCs

- A speed grade faster than competitive 20nm FPGAs
- Industry leading performance levels:
 - Fastest DDR interface
2.6 Gbps / 1.3 GHz DDR4
 - Highest performance SoC
1.5 GHz
 - Only hard floating point DSP
Up to 1.5 TFLOPS
 - Highest XCVR count and bandwidth in a monolithic FPGA
96 XCVRs delivering over 3.3 Tbps
- Only 20nm FPGA with fastest grade in industrial temperature (up to 500 MHz)

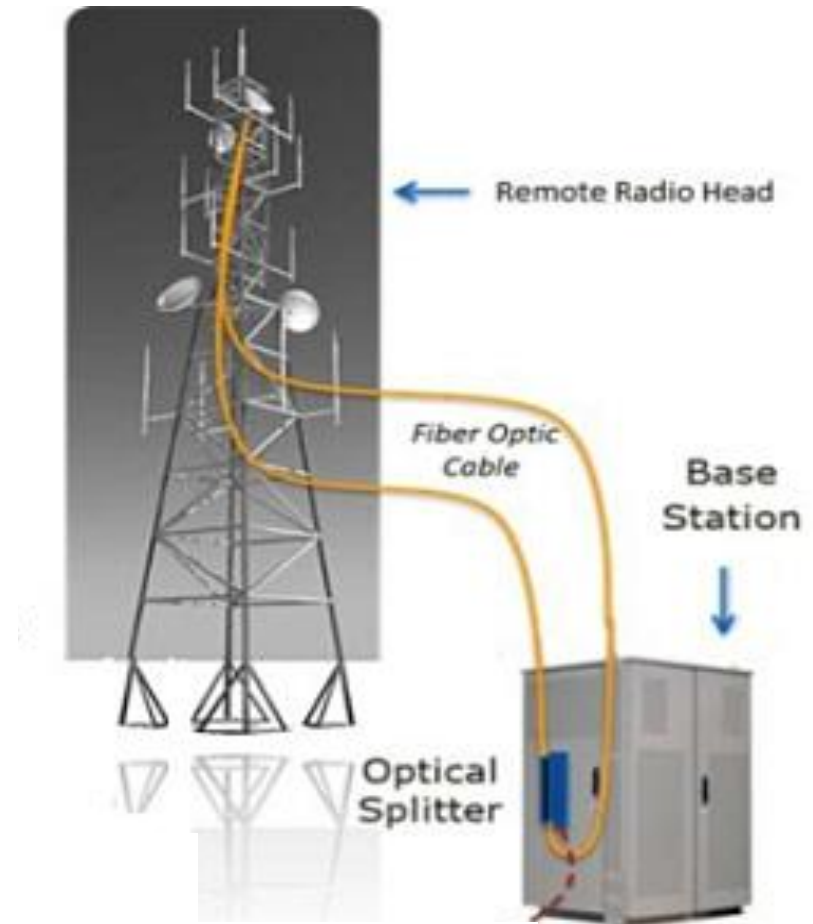
*Arria 10 FPGAs & SoCs:
Built for Performance*



(Average result from benchmark suite)

Arria 10 500MHz Benchmark Design – Remote Radio Head

- **Wireless infrastructure application**
 - Requires high performance, low power in harsh environmental conditions (I-temp)
- **Altera remote radio head (RRH) benchmark design emulates 8TX, 8RX**
- **Each TX/RX can support 2 LTE 5/10/20MHz carriers**
 - Total system bandwidth targeted for 40 MHz
- **Performance target: 491MHz**



Remote Radio Head Benchmark Design – Arria 10 Results

■ Benchmark design details

- Includes digital front end (DUC, CFR, DPD, DDC) clocked at 491MHz

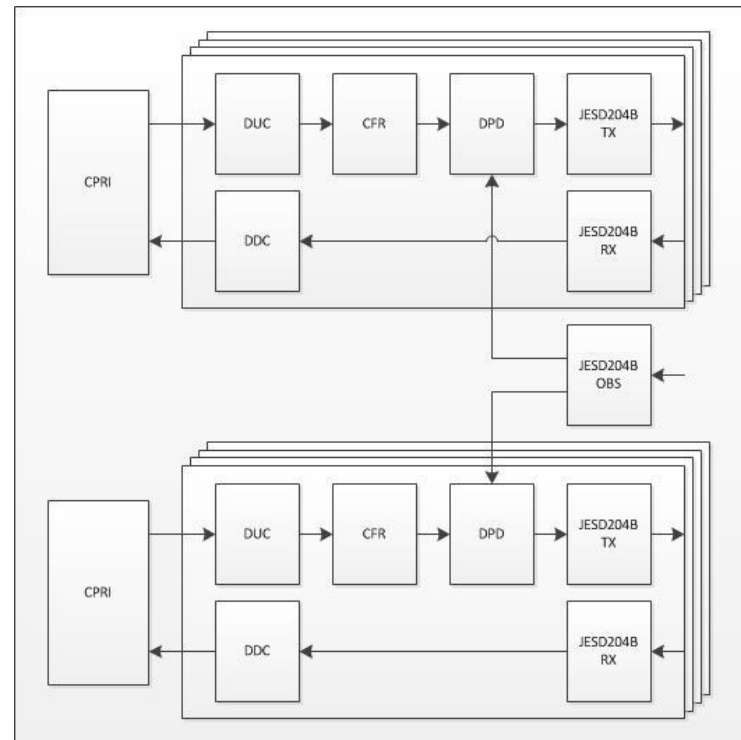
■ Resource utilization

(targeting Arria 10 GX 660, -1 speed grade)

- 160K ALMs
- 19K MLABs
- 195K FFs
- 1080 DSP blocks
- 376 M20Ks

■ Performance target: 491MHz

■ Performance achieved: 508MHz at Industrial Temp



Altera RRH Benchmark Design

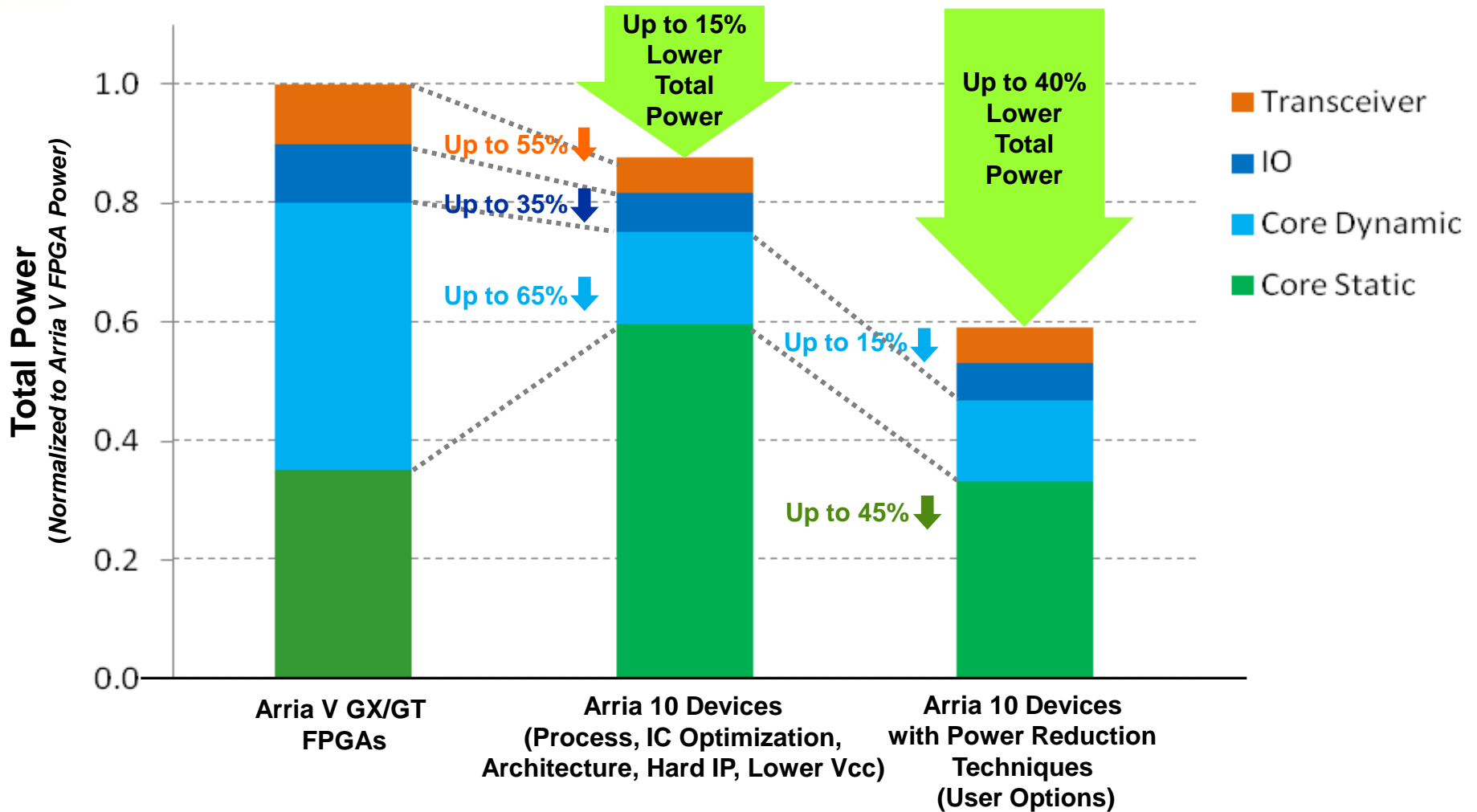
Arria 10 FPGAs & SoCs: Lowest Power @ 20 nm



- Advanced 20 nm process
- Comprehensive power reduction features
- Lowest transceiver power in class
- Reduced static power options
- Most power-efficient embedded processor
- Extensive use of hard IP

Up to 40% Lower Power than Prior Generation Midrange FPGAs

Power Reduction in Arria 10 vs. Arria V



Up to 40% Total Power Reduction Compared to Arria V GX/GT FPGAs

Arria 10 Power Saving Innovations

SmartVoltage ID

Enables device to run at lower than nominal Vcc while retaining same performance level reducing static and dynamic power

Programmable Power Technology

Enables lower power transistors for non-performance critical paths to reduce static power

Vcc PowerManager

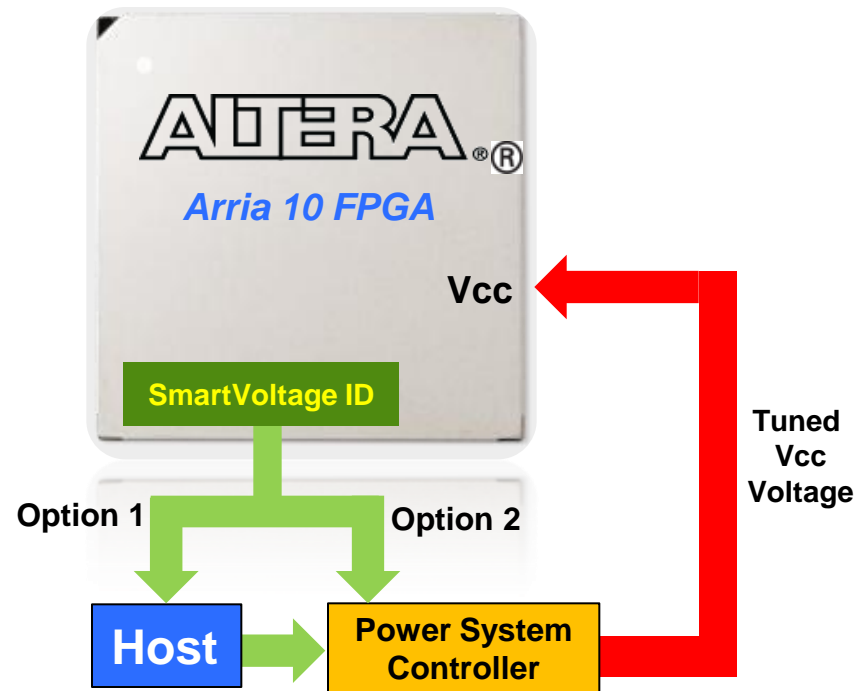
Lower operating Vcc to trade off performance to achieve lower total power

Low Static Power Speed Grades

Devices tested to lower static power and designated -L (low static power)


SmartVoltage ID Power Reduction

- **Allows FPGA to be operated at lower core Vcc while retaining same performance**
- **Reduces static power**
 - Lowers worst-case static power
 - Shown in Early Power Estimator
- **Also reduces average dynamic power consumption across distribution of devices**
 - Lower OpEx
- **Requires power system controller that can support tuned voltage**



Reduce Static Power by 40%+

SmartVID in Early Power Estimator



Visit the [Online Power Management Resource Center](#)

PowerPlay Early Power Estimator
Arria® 10

Input Parameters		Thermal Power (W)	
Family	Arria 10	Logic	1.178
Device	10AX048	RAM	0.211
Device Grade	Industrial -2	DSP	0.077
Package	F29	Clock	1.867
Transceiver Grade	E2	PLL	0.120
Power Characteristics	Maximum	I/O	0.350
V _{CC} Voltage (mV)	900	XCVR	0.572
SmartVoltage ID	On	HPS	0.000
Power Model Status	PRELIMINARY	P _{STATIC}	8.645
Junction Temp, T _J (°C)	User Entered	TOTAL (W)	13.020
Junction Temp, T _J (°C)	100	SmartVID Power Savings	3.389
Cooling Solution	N/A	TOTAL After SmartVID (W)	9.631

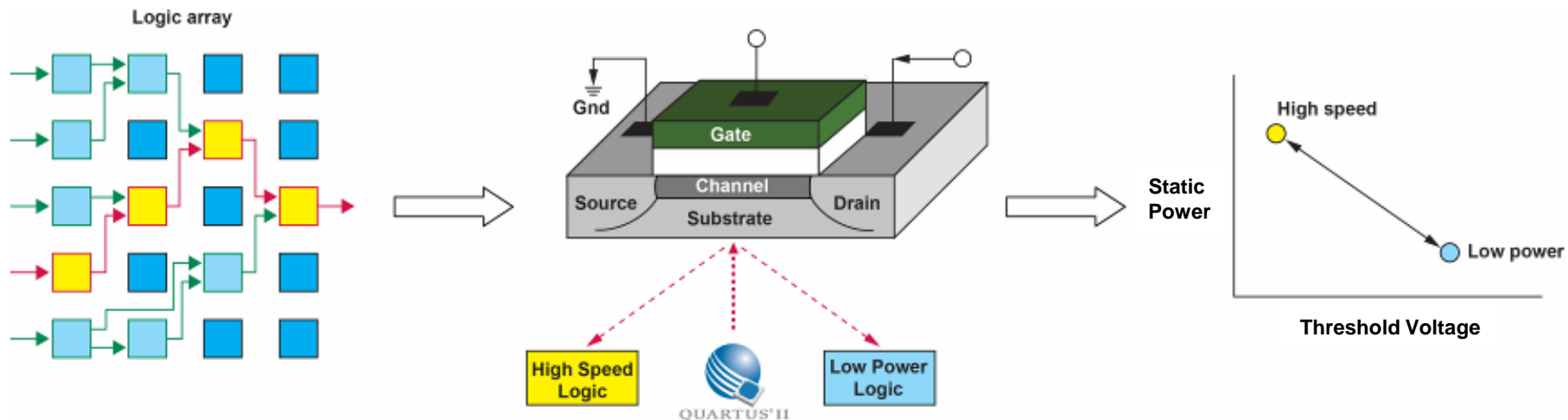
Total Power without SmartVID Benefit

SmartVID Power Reduction Benefit

Total *Worst-Case Power* After Applying SmartVID

Early Power Estimator Shows Worst-Case Total Power Including SmartVID Benefit

Programmable Power Technology



Accelerate speed-critical paths while reducing power on non-speed critical paths

Quartus II optimizes your design automatically, enabling high-speed logic only where needed

Get performance where you need it, and reduced power everywhere else

Patented Altera Technology Reduces Core Static Power by Up to 20%

Vcc PowerManager in Arria 10 FPGAs

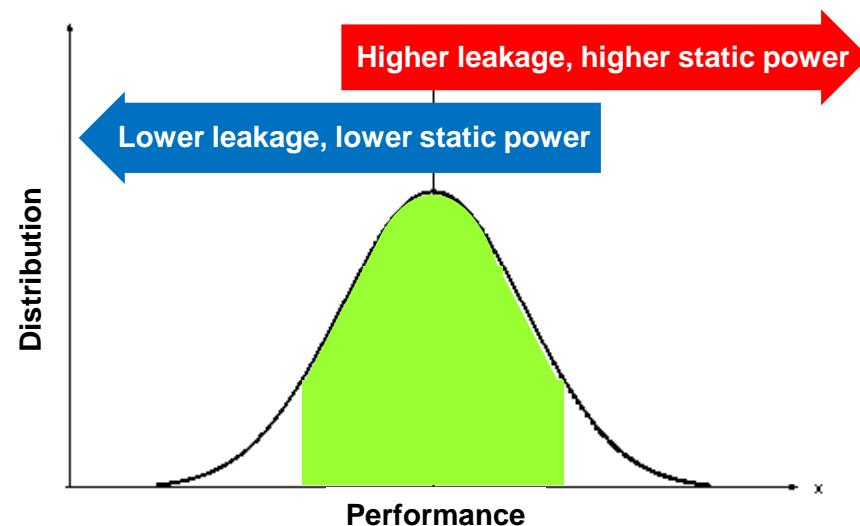
- Use lower Vcc to achieve lower power by trading off performance
- When lower Vcc applied, Fast speed grade devices operate at slower speed
- Requires timing closure at slower core speed

	Device Speed Grade		
Applied Vcc Level	Fast	Mid	Slow
Standard Vcc	<i>Fast core speed</i>	<i>Mid core speed</i>	<i>Slow core speed</i>
Lower Vcc	<i>Slow core speed</i>	NA	

Reduces Total Power by Up to 35%

Lower Static Power Speed Grades

- Takes advantage of process variation to offer lower static power devices (-L)
- Offered for both Extended (0°C – 100°C) and Industrial (-40°C – 100°C) versions



Distribution of Semiconductor Devices

Reduce Static Power by Up to 25%

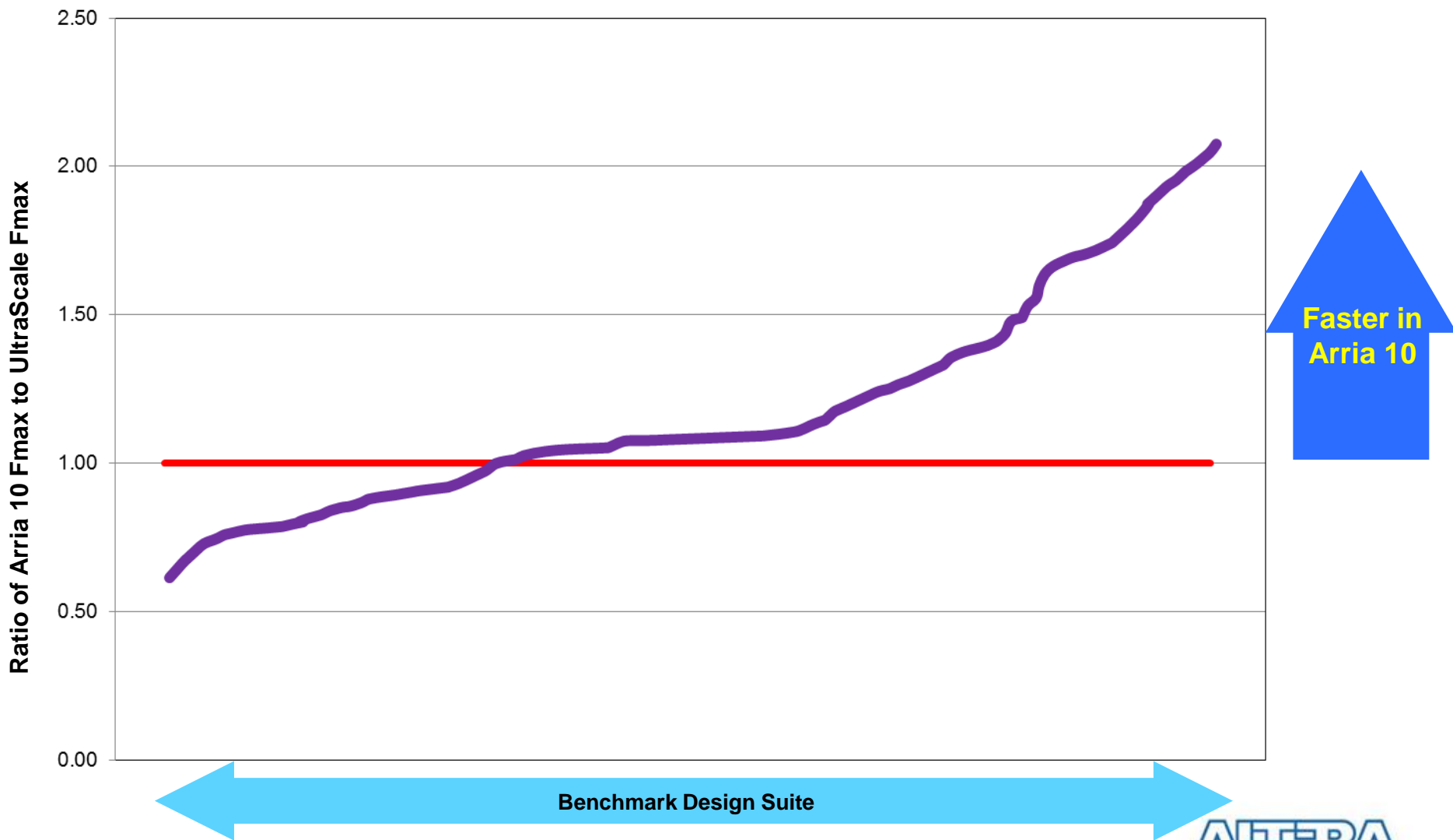
Arria 10 Performance Benchmarks



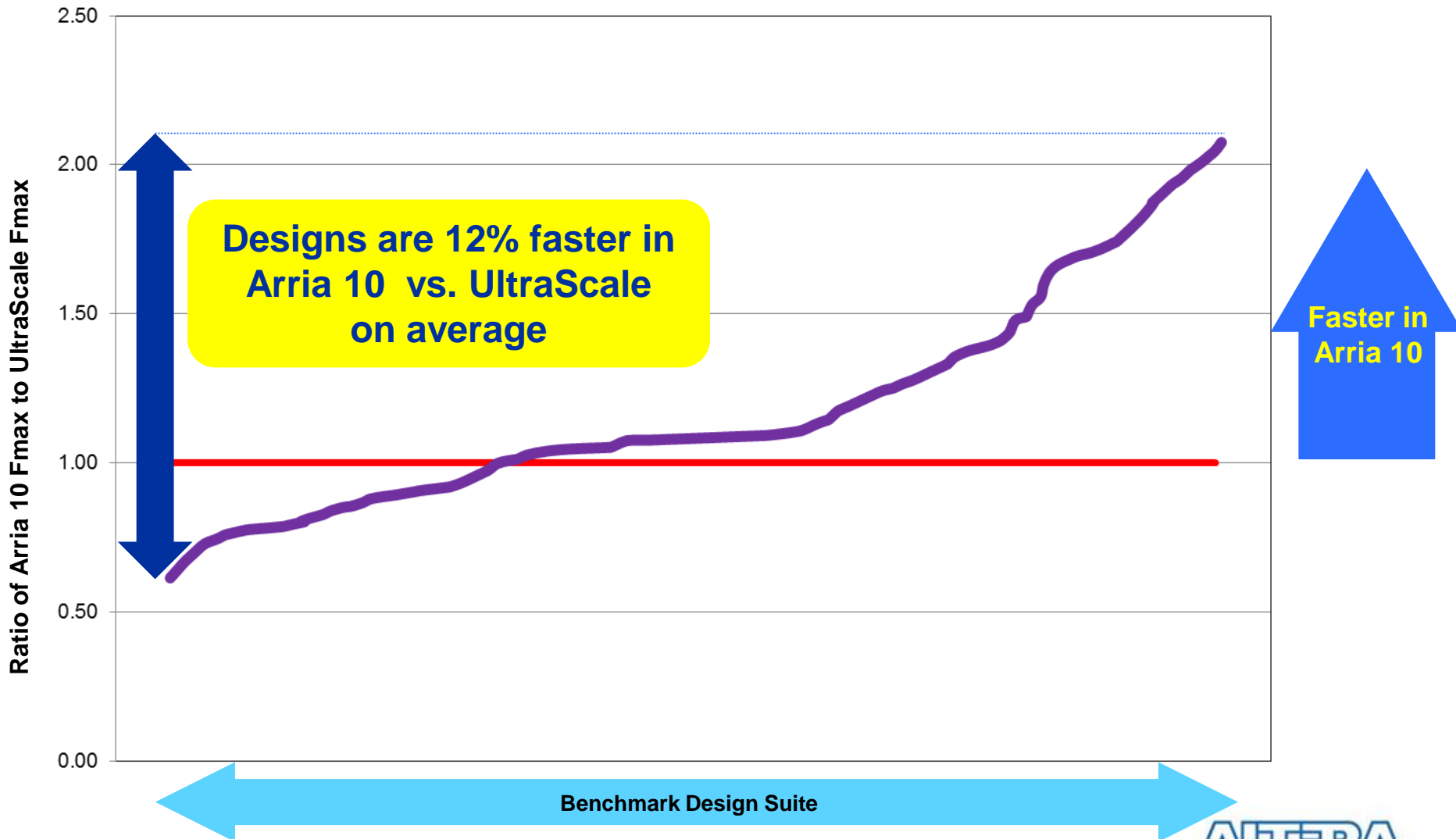
Arria 10 vs. UltraScale Benchmark

- **Benchmark suite includes range of designs**
 - Including device utilization over 95%
- **Fastest speed grade of each device family compared**
- **Compilation detail:**
 - Quartus II 14.0 public release version
 - Vivado 2014.2
 - Five seeds

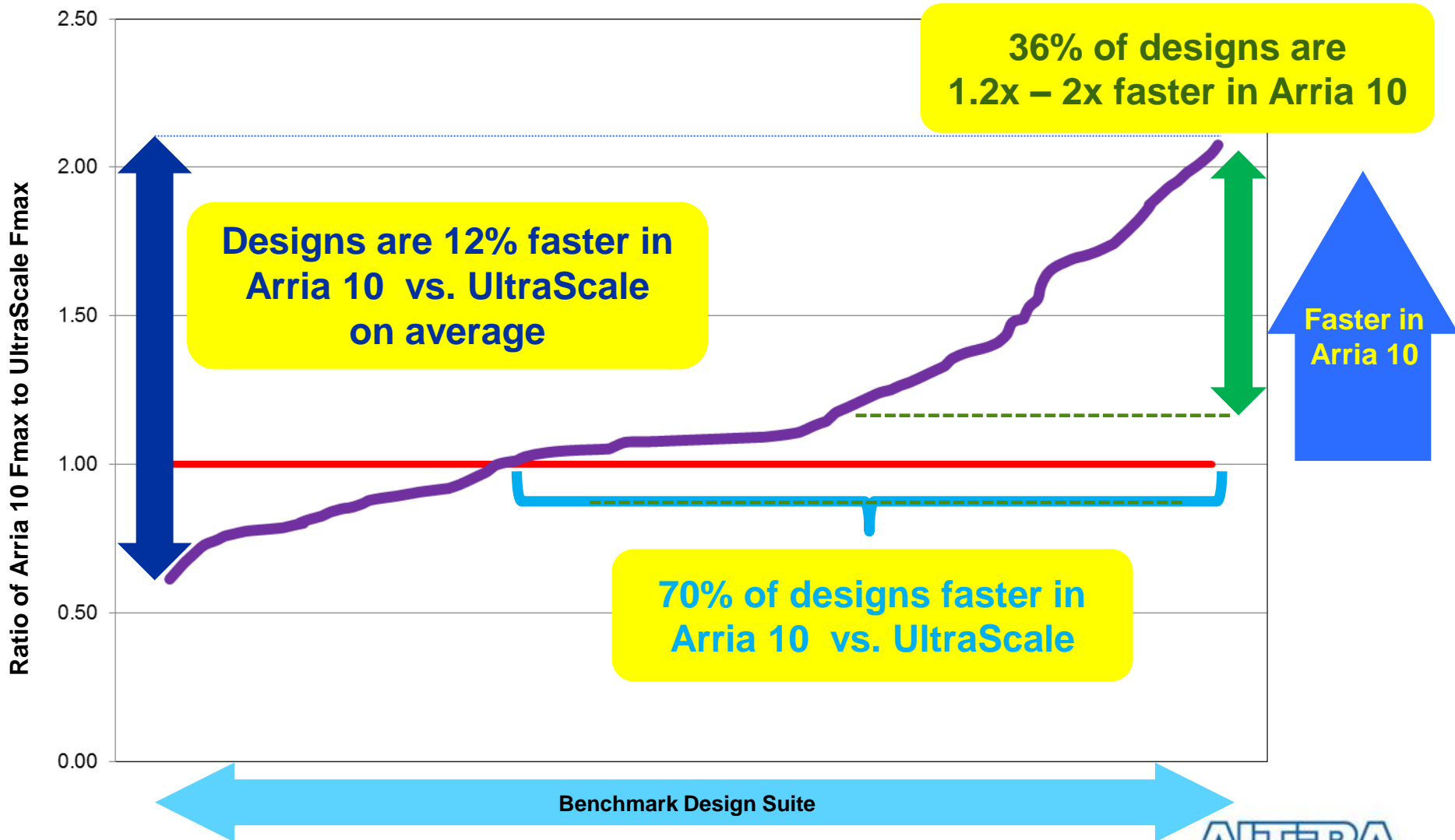
Arria 10 vs. UltraScale Fmax Benchmark Results



Arria 10 vs. UltraScale Fmax Benchmark Results



Arria 10 vs. UltraScale Fmax Benchmark Results





Arria 10 Transceivers



Arria 10 Transceivers

■ Highest bandwidth in a midrange FPGA

- Over 3 Tbps of transceiver bandwidth
- Up to 96 XCVRs
 - Up to 28.3G chip-to-chip/chip-to-module
 - Backplane support up to @17.4G
- First midrange FPGAs with >12G backplane support
- Hard Nios II processor for individual transceiver tuning and better signal integrity
- Hard IP for 10G/40GBase-KR FEC

■ Industry's strongest transceiver pedigree

- Comprehensive transceiver IP portfolio developed over a decade
- Across ten product generations
- Overseen by the same core development team
- Leveraging over 100 man years of field-tested expertise



Planned Protocol Support	
10G-Base R/KR	PCI Express Gen 3
CEI-6G/10G	Infiniband
CPRI	QPI
DisplayPort	SATA / SAS
FibreChannel	SDI – SD/HD/3G/10G
GPON	Serial RapidIO
Gigabit Ethernet (GbE)	SFP + / XFP
Higig+	SFI – 4.2 / 5.2
IEEE 802.3ba 40G / 100G	SGMII
Interlaken	SONET OC-192
JESD204B	XAUI
OTU – 2/3/4	Custom protocols supported using “Native PHY” mode

Arria 10 Protocol Support

Market Segment	Standards	Protocol / Data rate
Wireline	IEEE	GbE (1.25Gbps) XAUI, HiGig (>3.75G) 10GBase-R, 10GBase-KR, 40GBase-KR4, 40GE, 100GE XLAUI (4x10G), CAUI (10x10G) CAUI-4, CPPI-4 1588, SyncE, low latency
	Interlaken	6.25/10.3125/11.3/28G
	OIF	CEI 6G-SR/LR, 11G-SR/LR, 25G-SR/VSR, 28G-SR/VSR SFI-S 10G/28G, SFI-5.1/5.2 (17x3.125G, 4x10G)
	ITU	SONET OC-3/12/48/192/768 (0.155, 0.622, 2.488, 9.95, 4x10G) OTU-1/2/3 (2.66, 10.7, 4x10.7G, 4x25G) OTL 3.4/4.4/4.10/5.16 (4x10G, 4x25G, 10x10G, 16x25G)
	GPON/EPON	1.25/2.5/10G
Military/Wireless	JEDEC	JESD204B (3, 6.25, 12.5G)
	SRIO	1.25/2.5/3.125/6/10G
Wireless	CPRI	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144, 9.83, 10.13, 12.67, 20G

Arria 10 Protocol Support (continued)

Market Segment	Standards	Protocol / Data rate
Video/Broadcast	SDI	SD/HD/3G/10G
	DisplayPort	1.6/2.7/5.4G
	HDMI 1.3/1.4	3.4G
Computing/Storage	QPI	4, 4.8, 6.4, 8 , 9.6, 12G
	Fibre Channel	FC1/2/4/8/10/16G
	Infiniband	2.5/5/10/25.8G
	SATA/SAS	1.5/3/6/12G
General	PCI Express	Gen 1/2/3 (2.5, 5, 8G)
	Altera	SerialLite III (up to 25G)
	HMC Consortium	HMC2
	MoSys	GCI (10.3G)
	MSA	SFP+, XFP, QSF, CFP, CFP2, CFP4 (4x25G)

Comprehensive Set of Industry Standards



Arria 10 Transceiver Enhancements

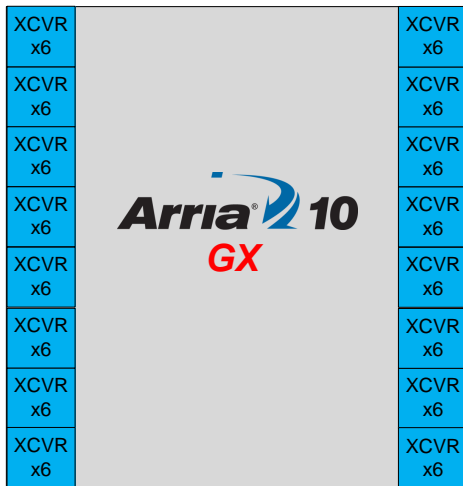
Feature	Arria V GX/GT	Arria V GZ	Arria 10 Devices
Technology	28 nm	28 nm	20 nm
Transceivers	32	36	96
Data Rate	6.5Gbps /10.3125Gbps	12.5Gbps chip-to-chip 12.5Gbps backplane	28.3 Gbps chip-to-chip 17.4Gbps backplane
Transmit Pre-emphasis	Yes	Yes	Yes
Adaptive CTLE (Continuous Time Linear Equalizer)	Yes	Yes	Yes
Adaptive DFE (Decision Feedback Equalizer)	No	Yes	Yes
Backplane Total Equalization Gain	No	25dB	>30dB

**Arria 10 Delivers High-End
Transceiver Performance**

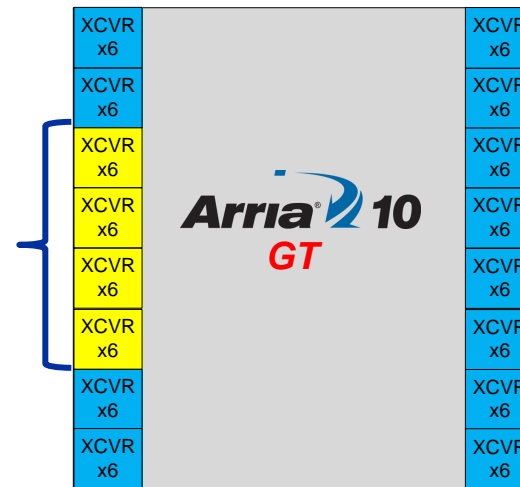


Arria 10 Transceiver Overview

	Arria 10 GX	Arria 10 GT
Transceiver Count	Up to 96	Up to 96
Max Data Rate	17.4 Gbps	28.3 Gbps
Number of 28G Channels	0	16
Max Backplane Data Rate	16 Gbps	17.4 Gbps



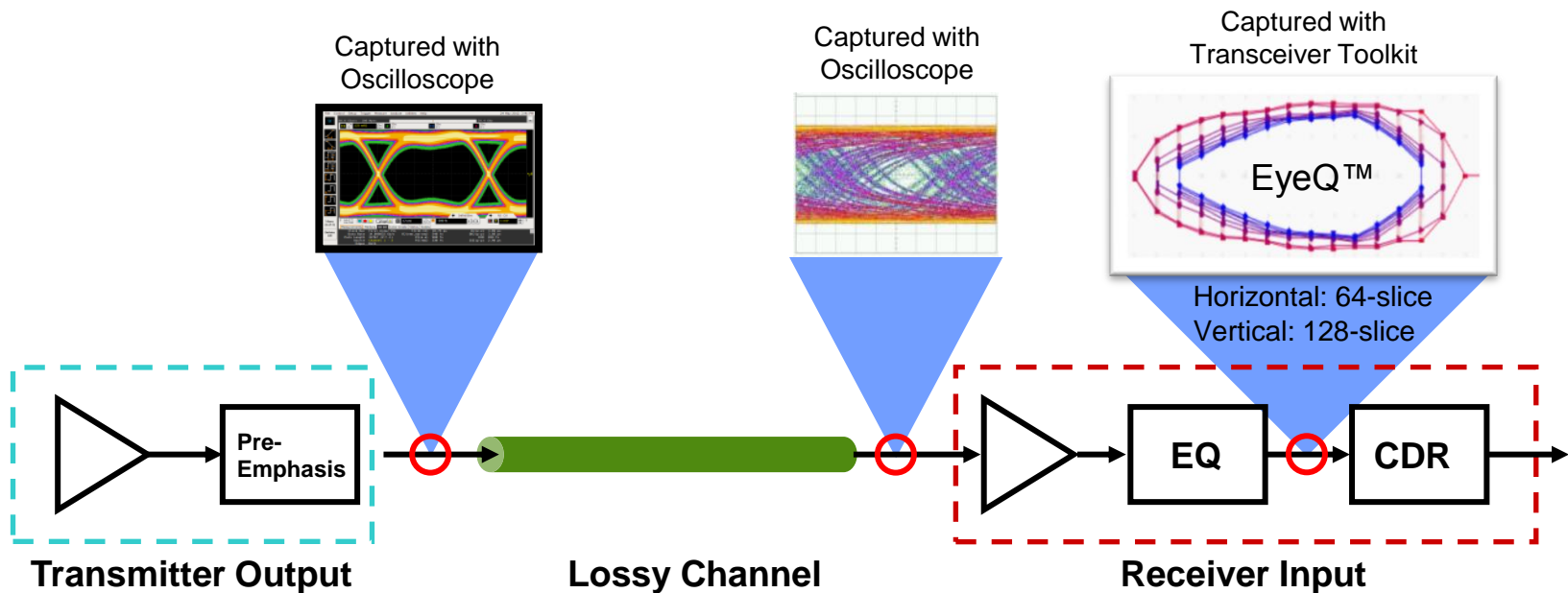
**28.3Gbps
Capable
Channels**



High Port Count and High Bandwidth Applications in a Mid-range platform

Arria 10 FPGA On-Die Instrumentation

- **View eye-opening at CDR input, inside receiver**
 - Complete X and Y reconstruction of post-equalized eye opening
- **Evaluate effectiveness of signal-conditioning techniques**
 - Verify optimal pre-emphasis, CTLE, and DFE settings for largest eye opening
- **2X horizontal and 2X vertical resolution compared to Arria V GZ**



*Minimize Board Bring up / Debug Time
With EyeQ*

Arria 10 Industry-Leading PCI Express Support

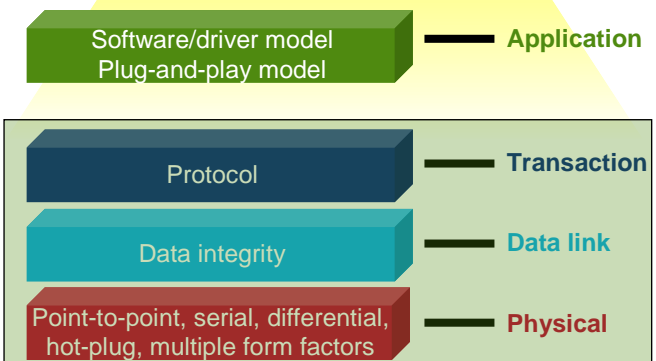
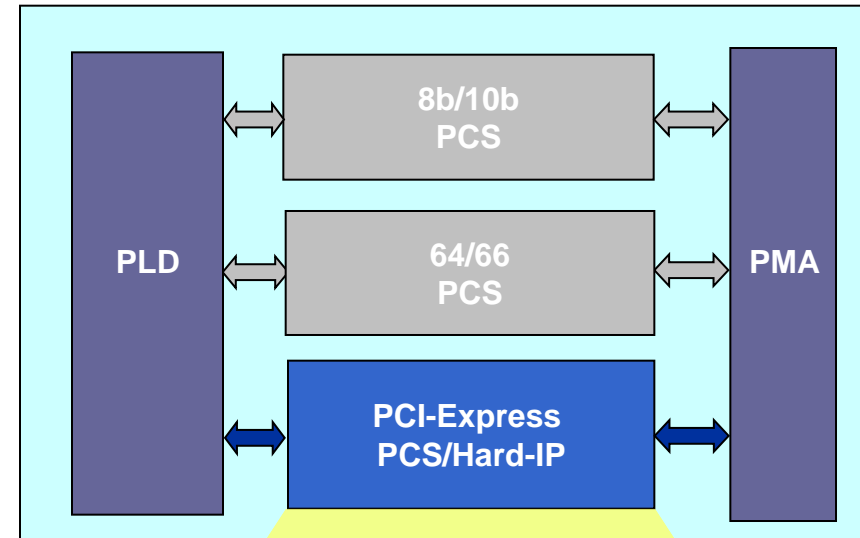
■ PCIe Gen 3/2/1 hard IP block with 256-bit architecture

- Provides built-in timing closure
- Reduces costs, power, and design time
- Live link within 100ms
- Supports root port and end point

■ Supports Configuration via Protocol (CvP) with PCIe

Altera Industry Leadership in PCI Express

- ✓ First to offer hard PCIe Gen2 block
- ✓ First to offer hard PCIe Gen3 block
- ✓ First to demonstrate PCIe Gen3 interop



*Industry's Most Mature and Trusted PCIe IP
Comes to 20 nm*

Arria 10 Parallel and Serial Memory Interfaces



Arria 10 Hard Memory Controller & PHY

■ Hard memory controller- high-performance interface with built-in timing closure

- Shortens engineering cycles
- Saves logic and memory resources
 - 5K LEs and 29 M20K blocks per x72 DDR3 IF
- Up to x144 support
- Up to 4x72 DDR3 interfaces in a single device

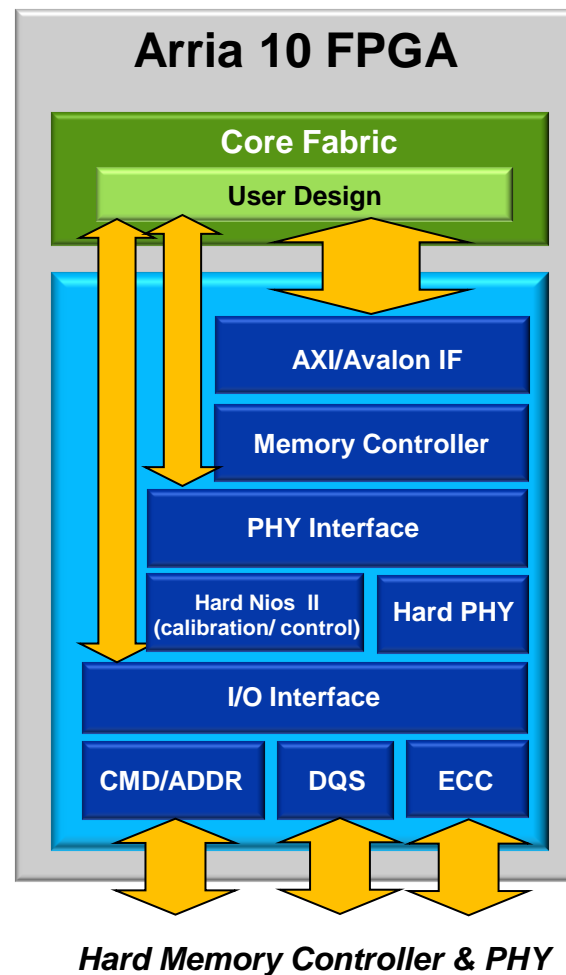
■ Hard memory controller supports

- DDR4, DDR3, LPDDR3
- Hard controller and PHY bypassable for flexibility to support emerging and legacy standards

■ Additional support (soft controller)

- RLDRAM 3, RLDRAM 2
- QDR IV, QDR II+, QDR II+ Xtreme

■ Intelligent calibration and skew control via Hard Nios II processor



**DDR4 Support
Up to 2666 Mbps**

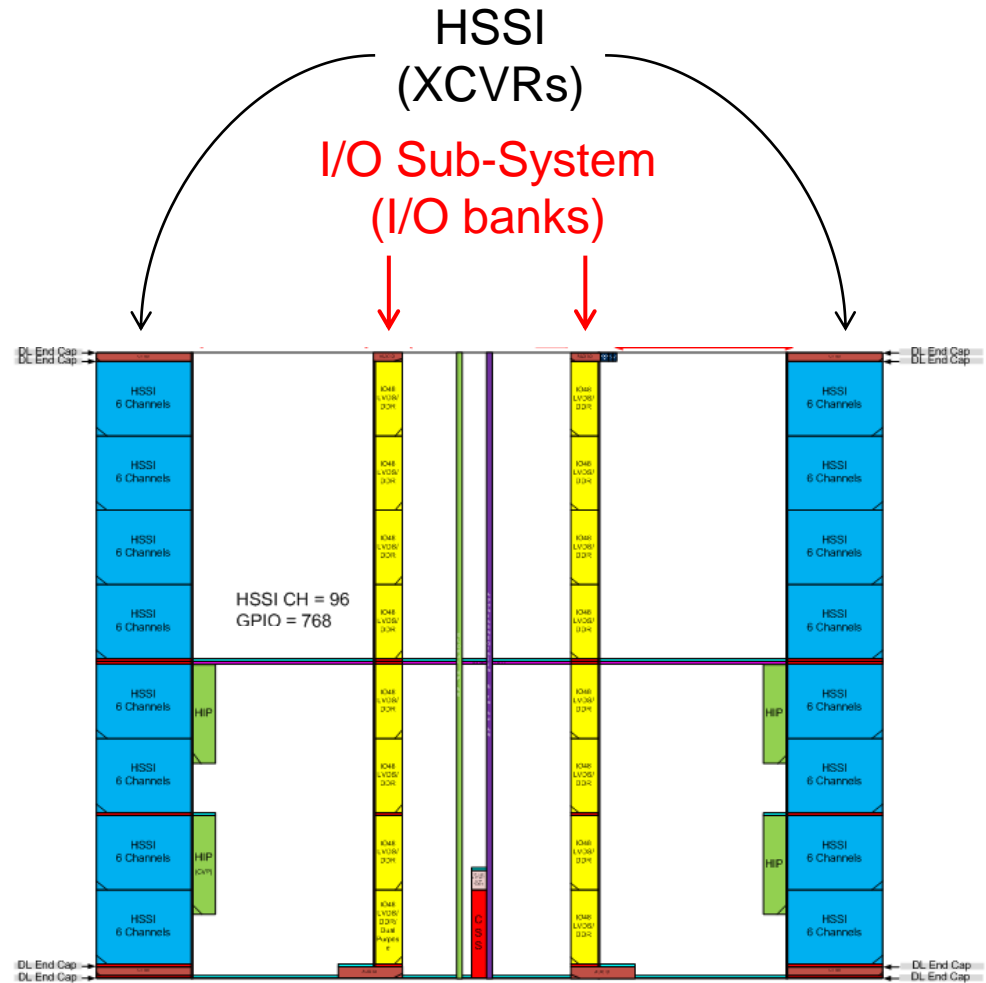
Arria 10 I/O Sub-System

■ Supports

- General Purpose I/Os (GPIO)
 - I/O Registers & I/O Buffers
- PLLs
 - IOPLL for EMIF and user logic
- External Memory Interfaces (EMIF)
 - Hard Memory Controller
 - Hard PHY
 - Hard Nios / Calibration sequencer
 - DLL
- LVDS
- On-chip Termination Control (OCT)

■ Organized in columns of

- I/O banks (groups of 48 I/Os)



Arria 10 I/O Bank (48 General Purpose I/Os)

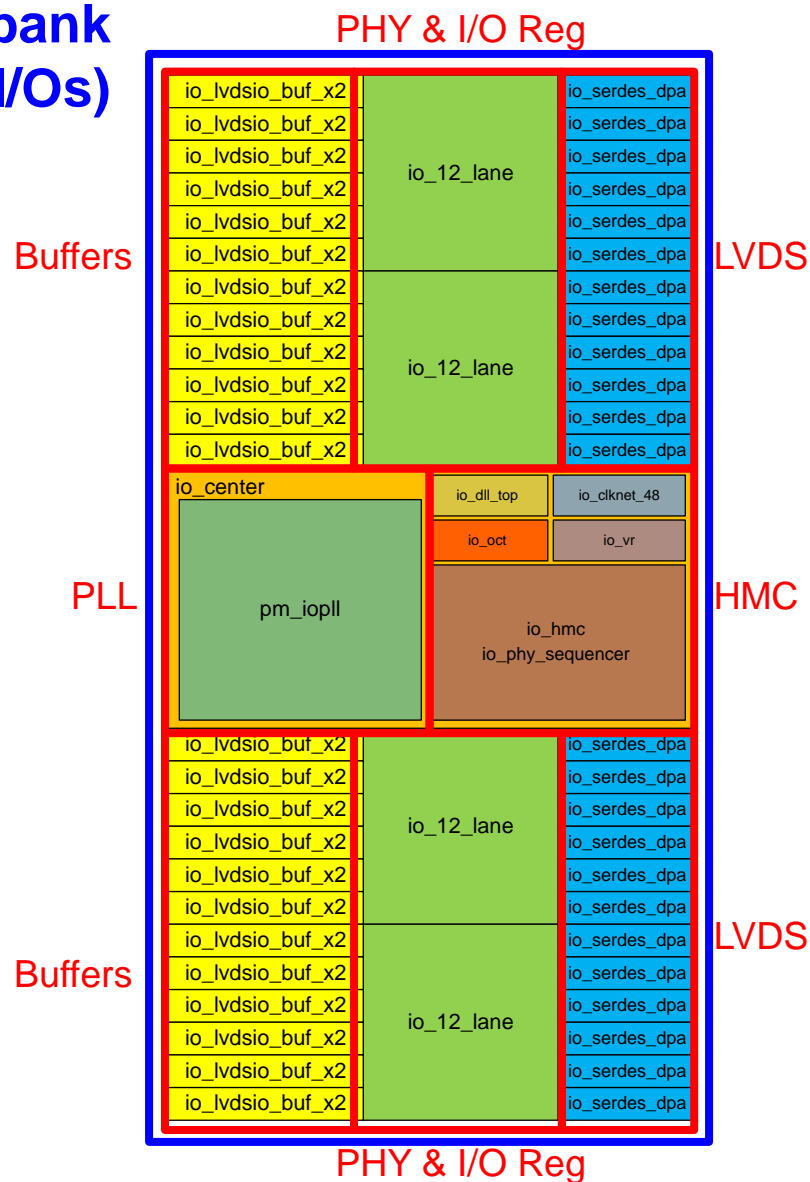
■ Supports

- General Purpose I/Os (GPIO)
 - I/O Registers & I/O Buffers
- PLLs
 - IOPLL for EMIF and user logic
- External Memory Interfaces (EMIF)
 - Hard Memory Controller
 - Hard PHY
 - Hard Nios / Calibration sequencer
 - DLL
- LVDS
- On-chip Termination Control (OCT)

■ Organized in columns of

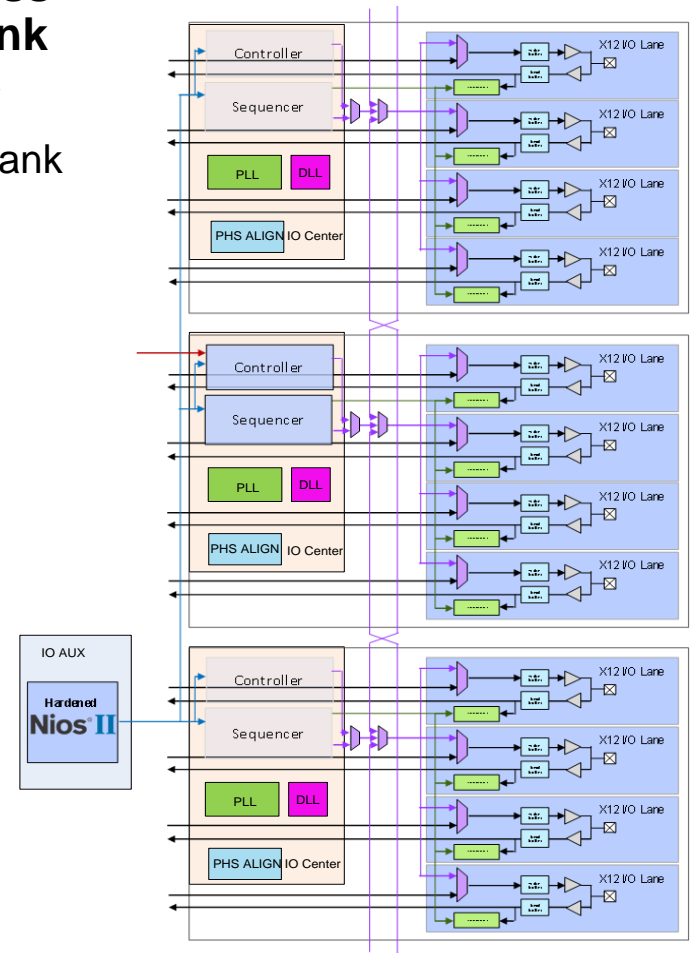
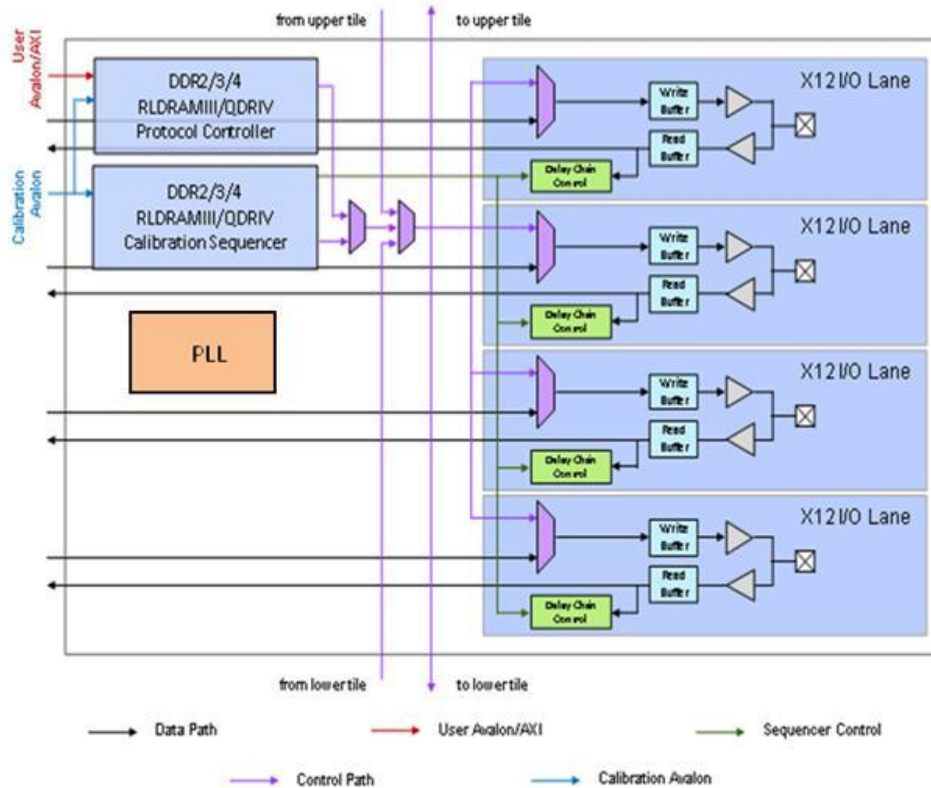
- I/O banks (groups of 48 I/Os)

I/O bank (48 I/Os)

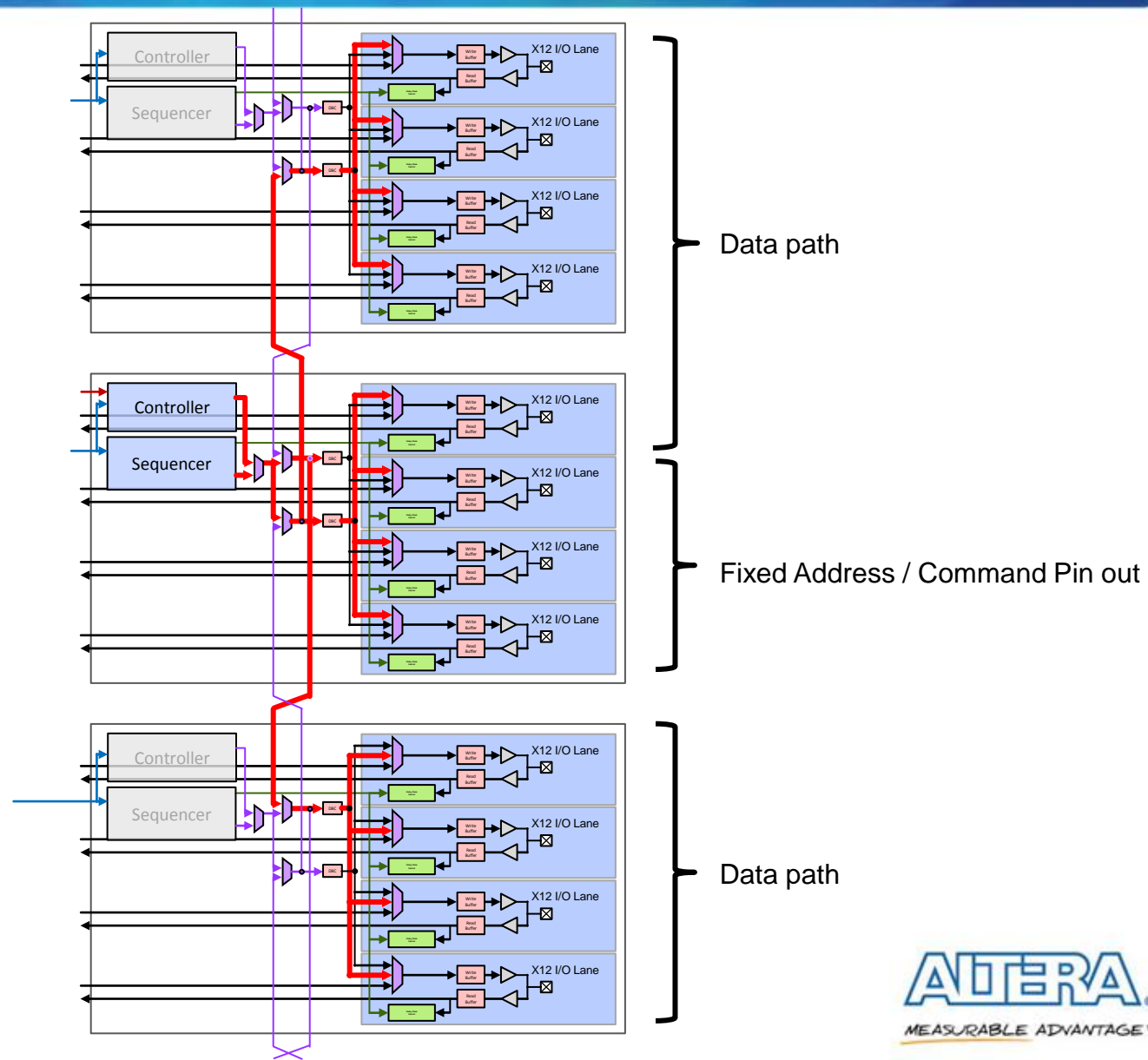


Arria 10 EMIF Architecture

- **Controller and Sequencer can only drive Address and Command lines to I/O lanes in same I/O bank**
 - But can drive data groups to banks above and below
 - Address/Command pins have fixed locations in I/O bank
 - Similar to hard interface in Arria V & Cyclone V



Arria 10 EMIF Example, 72-bit Interface (3 I/O Banks)

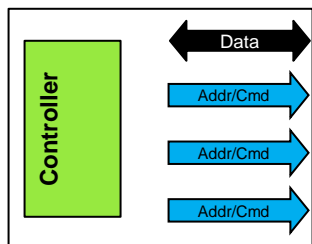


Arria 10 EMIF, Other Examples

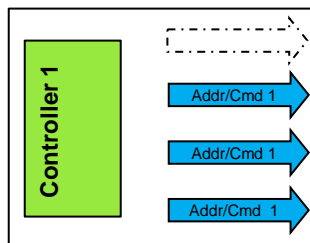
1 x 144 pin
(6 banks)



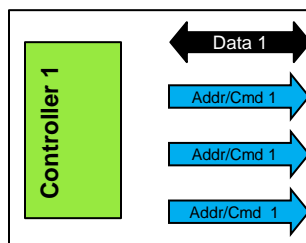
1 x 8 pin
(1 bank)



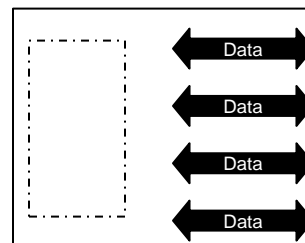
2 x 16 pin
(3 banks)



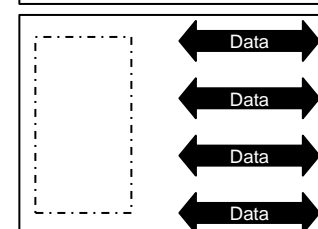
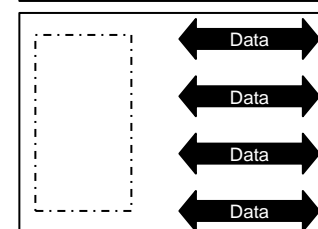
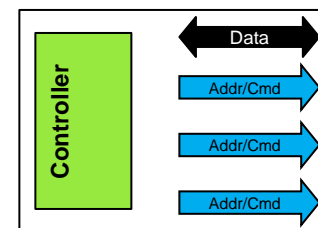
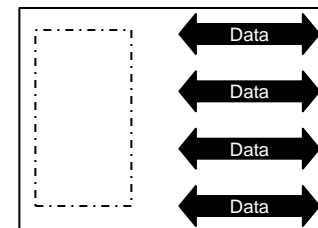
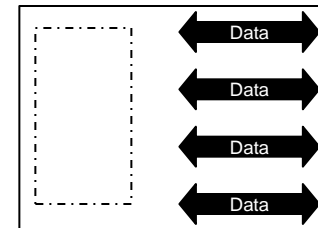
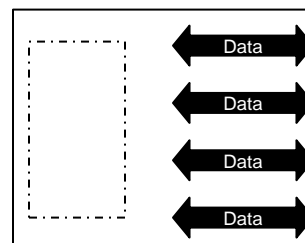
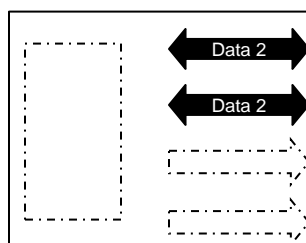
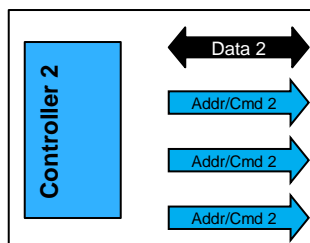
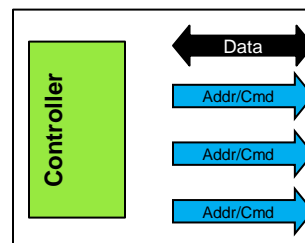
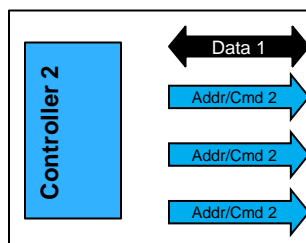
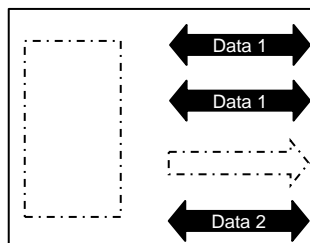
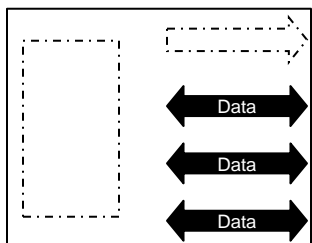
2 x 16 pin
(3 banks)



1 x 72 pin
(3 banks)



1 x 32 pin
(2 banks)



Arria 10 Hard Memory Controller Enhancements

Feature	Arria V GX/GT	Arria 10
Interfaces Supported	DDR3, DDR2	DDR4, DDR3 LPDDR3
Maximum Interface Width	x64	x144
Maximum Interface Rate	1066 Mbps (DDR3)	2133 Mbps (DDR3) 2666 Mbps (DDR4)
Maximum x32 I/F per Device	4	7
DIMM Support	None	DDR4, DDR3

*Higher Performance and Greater Capability
Compared to Prior Generation*

Arria 10 Memory Interface Support by Speed Grade

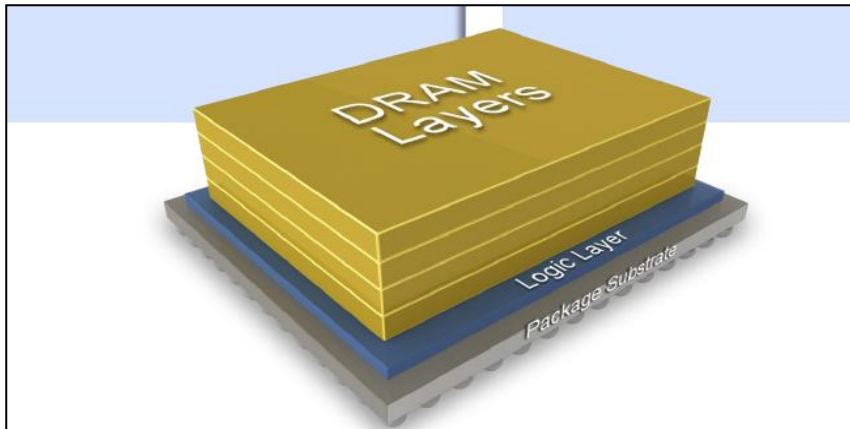
Memory Standards	-1 Grade		-2 Grade		-3 Grade	
	Parallel Memory					
	1 Rank / CS	2 Rank / CS	1 Rank / CS	2 Rank / CS	1 Rank / CS	2 Rank / CS
DDR4 UDIMM/RDIMM/Comp	2666	2400	2132	1866	1866	1600
DDR4 LRDIMM	2666	2666	2132	2132	1866	1866
DDR3 / 3L	2133	1866	2133	1866	1866	1600
LPDDR3	1600		1600		1334	
Parallel Memory						
QDR IV	2133		2133		1866	
QDR II+Xtreme	1266		1100		1000	
QDR II+	1100		1000		900	
QDR II	700		700		700	
RLDRAM 3	2400	2132	2132	1866	1866	1600
Serial Memory						
Hybrid Memory Cube (HMC)	16x15 Gbps per link, up to 4 links					

Full Support for Key Parallel and Serial Memory Interfaces

Hybrid Memory Cube (HMC) Technology

■ HMC technology basics

- Ultra high performance, multi-bank DRAM memory
- DRAM die stacked using state-of-the-art 3D process
- Built-in memory controller with logic base die



Parameters	Specification
Link	4
Speed	10,12.5,15 Gbps
Density	2GB, 4GB
Vaults	16
Banks	128, 256
DRAM B/W	160 GB/s (1.2 Tbps)
Vault B/W	10 GB/s (80 Gb/s)

■ Unparalleled gains with HMC

- Maximum DRAM bandwidth of up to 160 GB/s
- Four links running at 15 Gbps offering nearly 1 T bps raw interface bandwidth
- Up to 4GB density (storage) capacity, low PHY power (pj/bit)
- Best in class RAS feature set

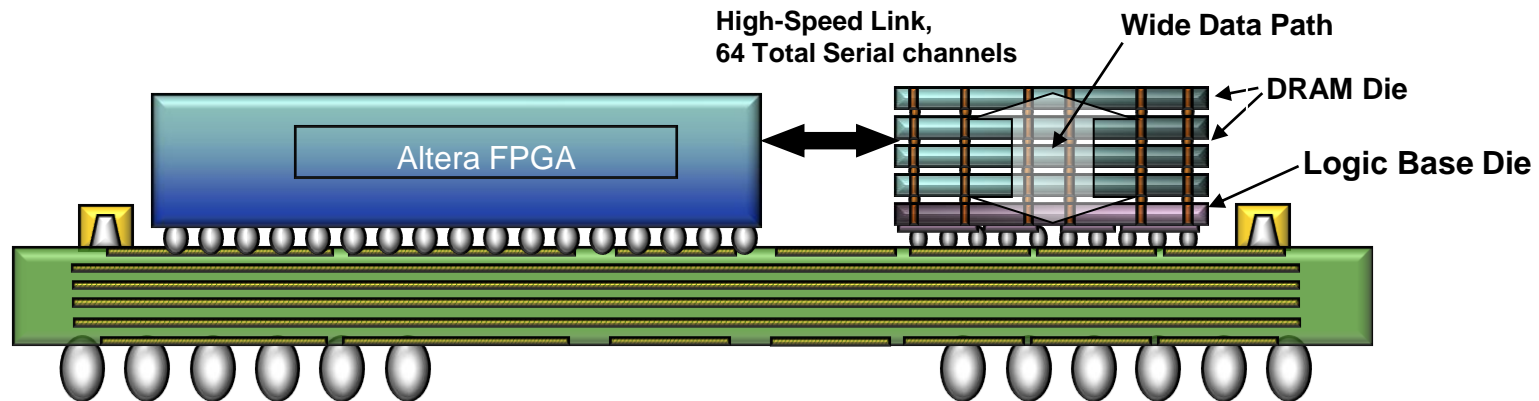
Altera Technology Leadership in HMC

■ HMC interoperability demo planned mid 2013

- First interoperability with HMC
- Lead development platform to fully test and validate Altera HMC performance

■ Altera support for HMC technology

- Arria 10 and Stratix 10 FPGAs and SoCs
 - Up to 4 links (16 lanes per link) @ 10G ,12.5G, 15G



Industry's First Support for HMC



Arria 10 DSP Capabilities



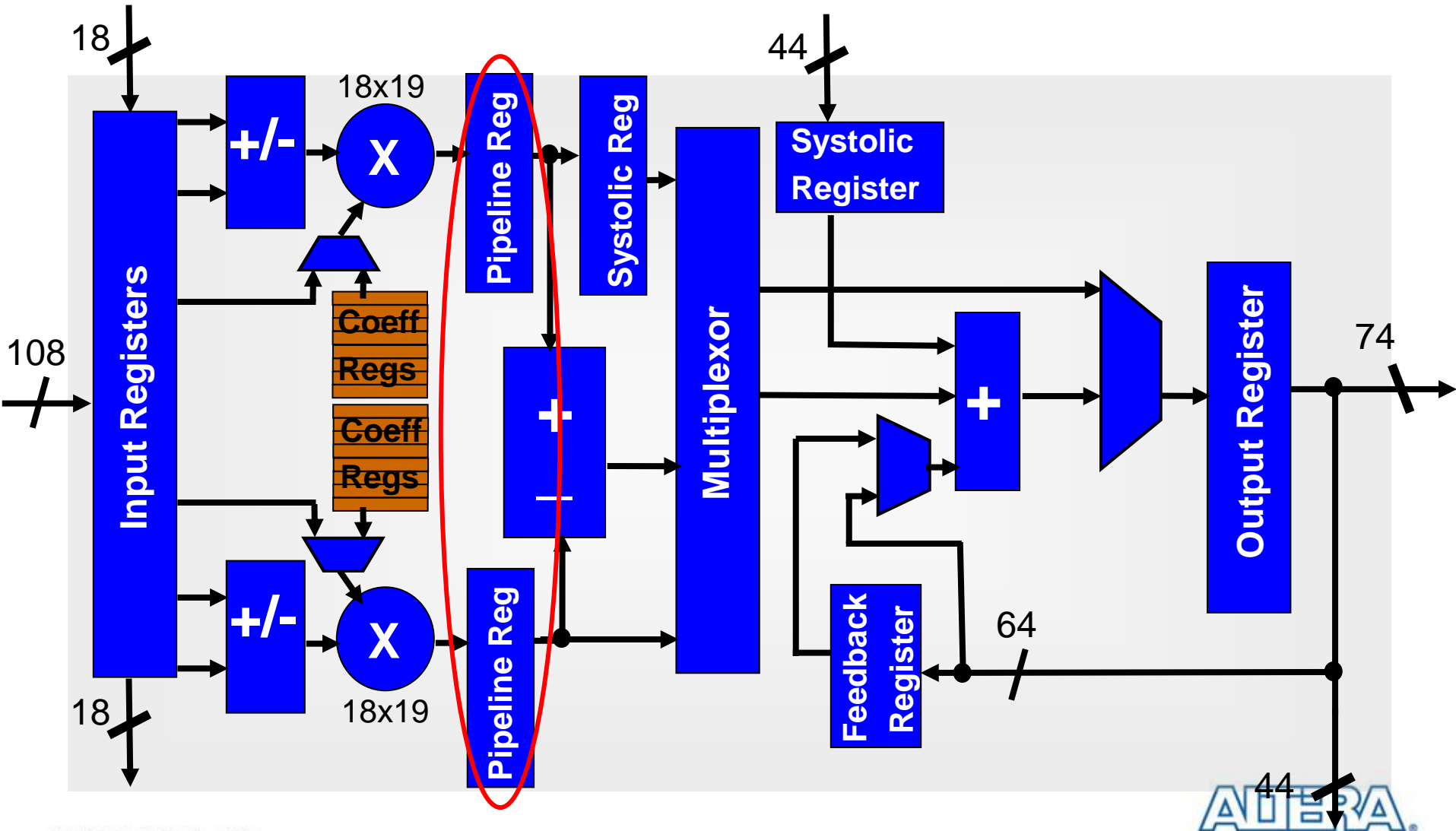
Arria 10: First Floating-Point FPGAs

- **The floating-point enhancements planned for Stratix 10 devices will be available in Arria 10 devices**
 - First floating-point FPGAs available a product generation sooner
- **Industry's only DSP architecture with hard single-precision IEEE 754 floating-point**
 - Higher efficiency implementation (eliminates 80% of logic)
 - Floating point with same performance, throughput and ease-of-use as fixed point
- **Delivers floating-point capabilities competitive with high-end GPUs**

Arria 10 DSP Block Versus Stratix V and Arria V

Relative to Stratix V DSP block	Additions	1) Increased I/O: 72 → 108 inputs, 64 → 74 outputs
		2) No pre-adder restrictions with external coefficients
		3) Fully Independent 18x19 multiplier outputs
		4) Dual accumulator registers, for simultaneous I/Q accumulation
		5) Pipeline register added to Arria 10 DSP block
Subtractions	Subtractions	1) 36x36, 18x36 multipliers now require some external logic support
		2) 9x9 multiplier size no longer supported in DSP block
		3) 18x25 complex mode removed
Relative to Arria V DSP block	Additions	1) Much higher DSP block Fmax (500-600 MHz depending upon characterization)
		2) Pipeline register added to Arria 10 DSP block
	Subtractions	Subtractions

Arria 10, 18-bit Fixed Point Mode



Arria 10 Core Fabric & Configuration

- [Embedded Memory (M20K, MLAB)]
- [Core PLLs]
- [Configuration Device]



Arria 10 M20K Block Feature Summary

Feature		Arria V	Arria 10
Maximum Performance		380 MHz	730 MHz
Total RAM Bits per Block		10,240	20,480
Total M20K Memory Bits (Mb) per Device		8-24	13-54
Port Width Configurations		8K x1, 4K x2 2K x 4, 5 1K x 8, 10 512 x 16, 20 256 x 32, 40	16K x 1, 8K x 2 4K x 4, 5 2K x 8, 10 1K x 16, 20 512 x 32, 40
Parity		✓	✓
Byte Enable		✓	✓
Packed Mode		✓	✓
Address Clock Enable		✓	✓
Mixed Clock		✓	✓
Mixed Width (for Dual Port modes)		✓	✓
ECC Support		Soft	Hard
Memory Modes	Single Port	✓	✓
	Simple & True Dual-Port	✓	✓
	Shift Register, ROM, FIFO	✓	✓

*Higher Performance, More Port Configurations,
and Hard ECC*



Arria 10 MLAB Feature Summary

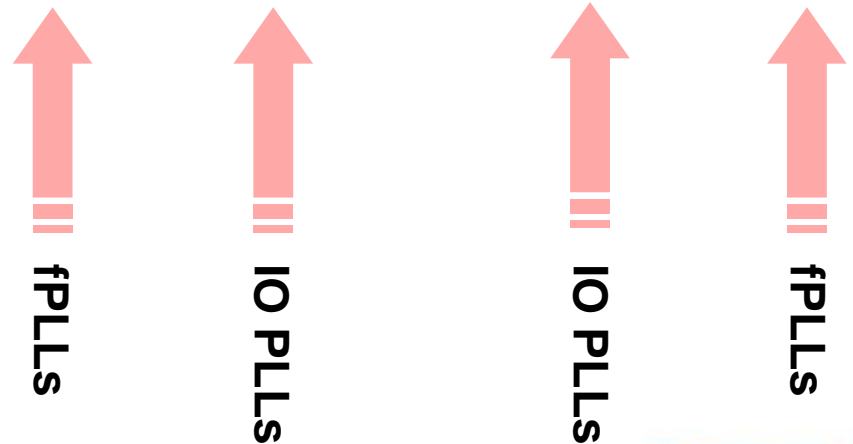
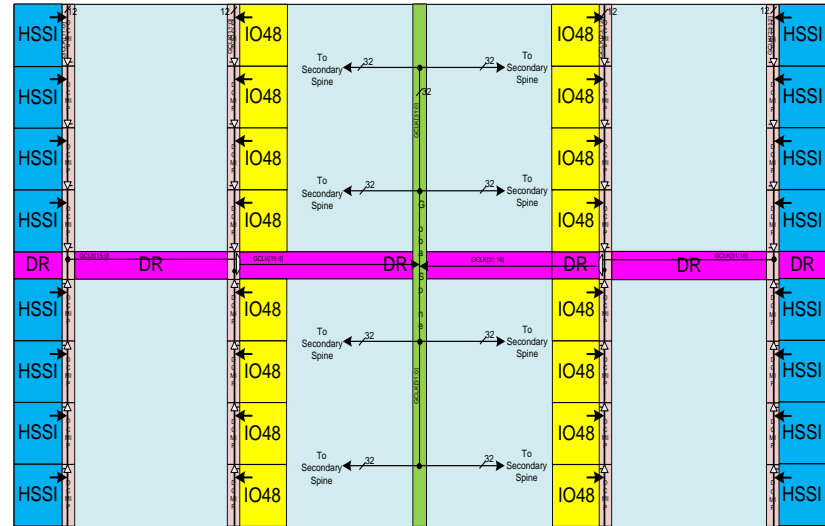
Feature		Arria V	Arria 10
Maximum Performance		300 MHz	700 MHz
Total RAM Bits per Block		640	640
Total Memory Bits (Mb) per Device		0.4 – 2.9	2-13
Port Width Configurations		32 x 16 32 x 18 32 x 20	x 64 deep mode supported in emulation mode 32 x 16 32 x 18 32 x 20
Parity		✓	✓
Byte Enable		✓	✓
Address Clock Enable		✓	✓
Mixed Clock		✓	✓
Mixed Width (for Dual Port modes)		✓	✓
ECC Support		✓	✓
Memory Modes	Single Port*	✓	✓
	Simple Dual-Port	✓	✓
	Shift Register, ROM, FIFO	✓	✓

Over 2X Performance Increase Compared to Prior Generation



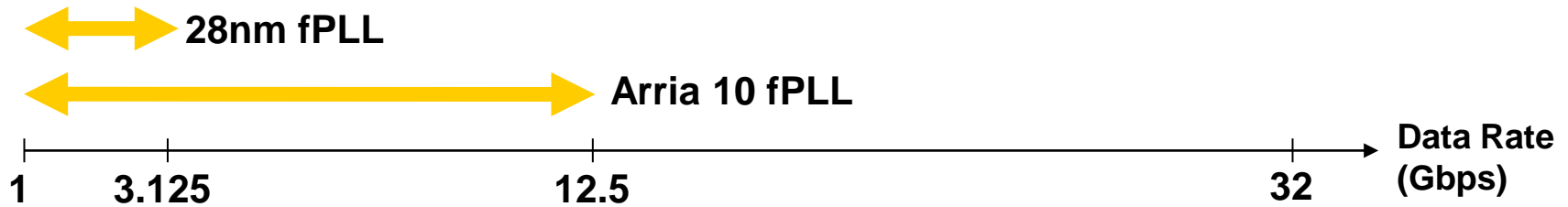
Arria 10 Core PLLs Introduction

- **Arria 10 devices have two different types of core PLL**
- **fPLL**
 - Fractional synthesis, integer modes
 - Located in every XCVR bank
 - 1 for every 3 XCVRs
 - General purpose use in core
 - Also used with XCVRs
- **IO PLL**
 - Integer mode only
 - Located in every IO bank
 - 1 for every 48 IOs
 - Primary use, EMIF, LVDS
 - Also general purpose use in core
- **Removed from architecture**
 - Corner PLLs
 - Top/bottom edge PLLs



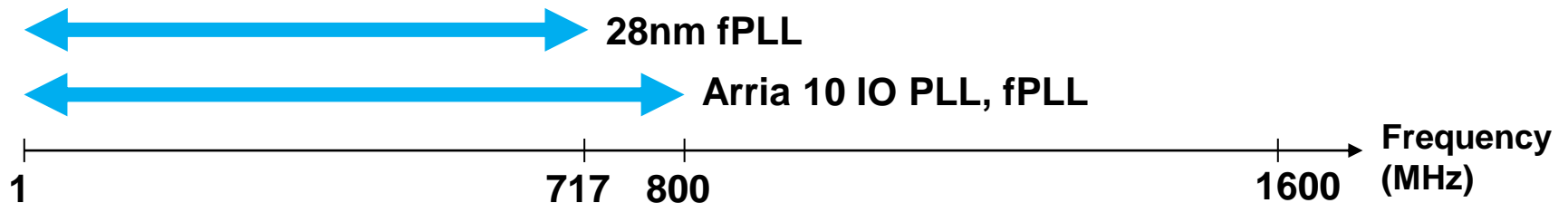
Arria 10 Core PLL Performance

■ fPLL used as transceiver TX PLL (integer mode)



- Jitter performance improved over 28nm
- Improvement not quantified yet
- Topic needs to be revisited when numbers are available

■ fPLL or IO PLL used as general purpose core PLL



Improved f_{MAX} and jitter performance

EPCQ-L Configuration Devices for Arria 10 Devices

EPCQ-L Configuration Devices

Supported Products	Arria 10 Devices Stratix 10 Devices
Data Interface	Active Serial x4/x1 @ 1.8V
Supply Voltage	1.8V
Package	24 pin Fineline BGA, 1.0 mm ball pitch, 6 mm x 8 mm Lead-Free (RoHS 6)
Shipping Media	Tray
Densities Available	256,512,1024 Mbit

EPCQ-L Selection Guide

Density (kLE)	Arria 10 GT FPGAs	Arria 10 GX FPGAs	Arria 10 SX SoCs
160	-	EPCQL256	
220	-		
270	-		
320	-	EPCQL512	
480	-		
570	-		
660	-		
900	EPCQL1024		-
1150	EPCQL1024		-

Assumes two uncompressed FPGA/SoC images

Use next smaller device for single FPGA image

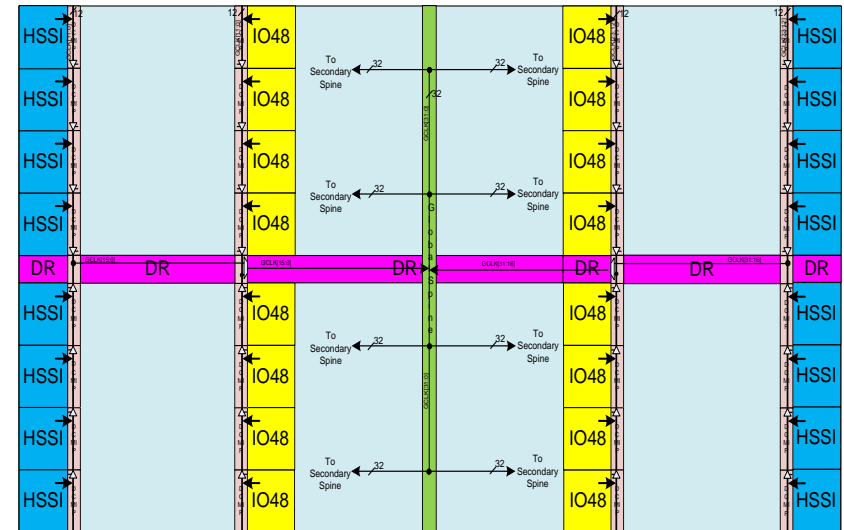
Images sizes are preliminary

Arria 10 Core Clocking



Arria 10 Core Clocking Introduction

- **Hierarchical architecture**
 - Low skew, balanced H-tree network
- **Target performance, 800MHz**
 - To meet high-speed application needs
- **Increased flexibility**
 - “Small” PCLK and “Large” PCLK
 - Reach of regional RCLKs redefined
 - More clock spine regions
 - PLL compensation support for > 50% of general purpose PLLs



High-performance, 800MHz target

Arria 10 Core Clocking Network Hierarchy

■ 1st level clock

- GCLK network
- RCLK network
- PCLK network (SPCLK, LPCLK)
- PLL feedback clocks

■ 2nd level clock

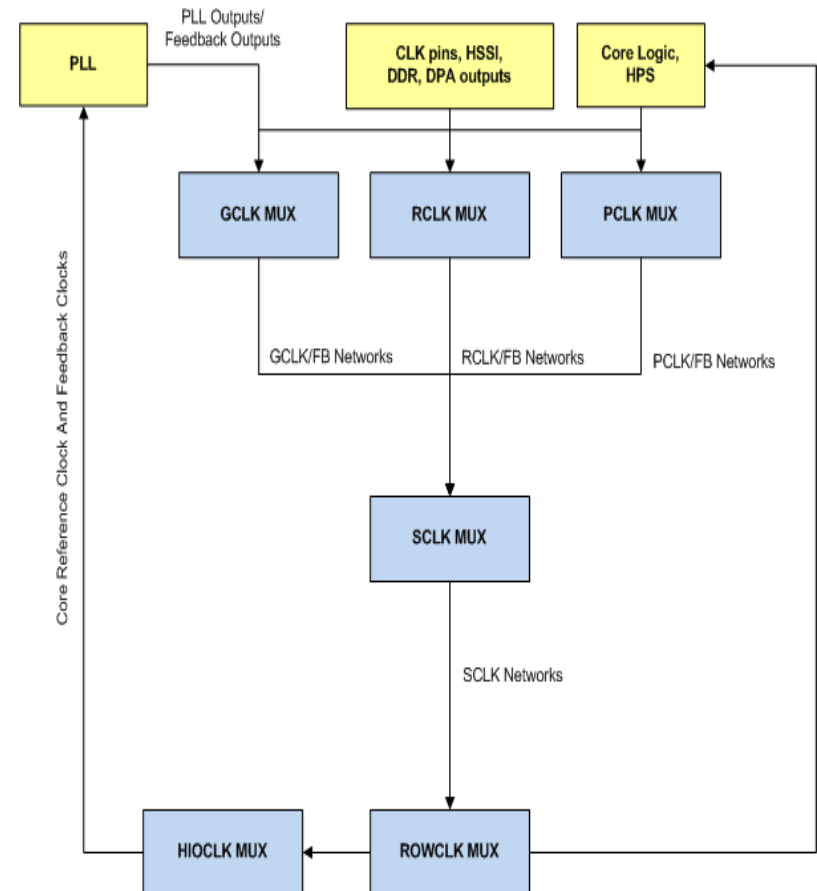
- SCLK network

■ 3rd level clock

- ROWCLKs
- HIOCLKs (but no VIOCLKs)
- Reference clocks back to PLLs
 - CoreREFCLK

■ Compared to Stratix IV, Stratix V

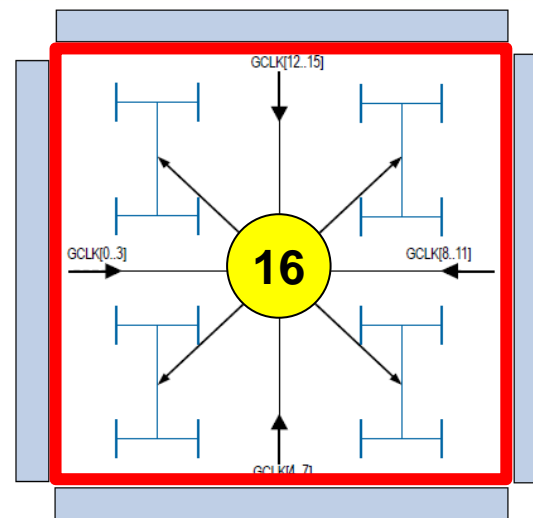
- Same balanced H-tree approach
- Same levels of hierarchy
- Different numbers of clock lines



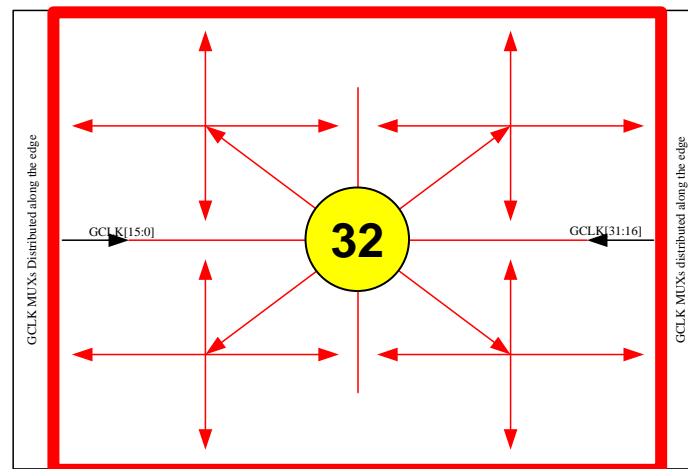
Arria 10 Core Clocking: GCLK Networks

- **32 GCLK versus 16 in Stratix V**
- **PLL compensation tracks shared with GCLK tracks**
 - No dedicated PLL compensation tracks
- **GCLK sources**
 - Dedicated clock pins
 - Core logic
 - PLL / Feedback outputs
 - DPA outputs from LVDS
 - HSSI Outputs
 - HPS Outputs
 - Switch_over_clk

Stratix V



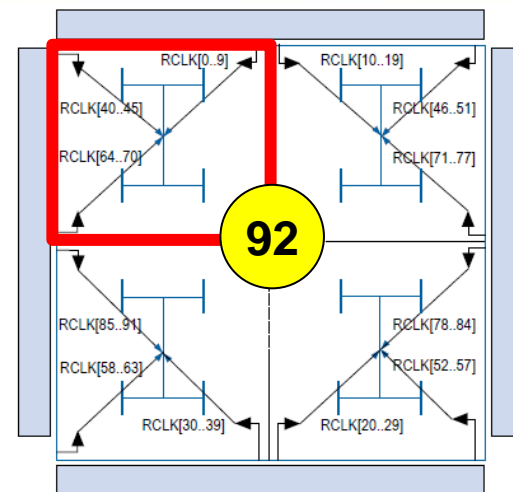
20nm



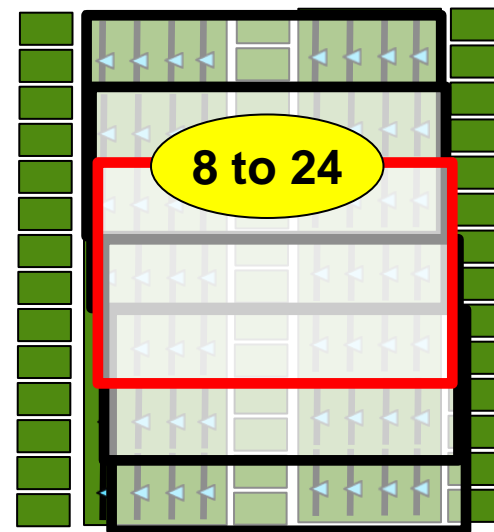
Arria 10 Core Clocking: RCLK Networks

- Replaces “quadrant” style RCLK used in Stratix IV, Stratix V
- Runs entire chip width horizontally, 4 or 6 IO banks vertically
- Staggered overlapping pattern (starts every 2 IO banks), provides support for HSSI channel bonding and DDR interfaces
- 4 RCLK lines per group of 6 IO bank
- RCLK sources similar to GCLK
- Does not include dedicated compensation tracks

Stratix V



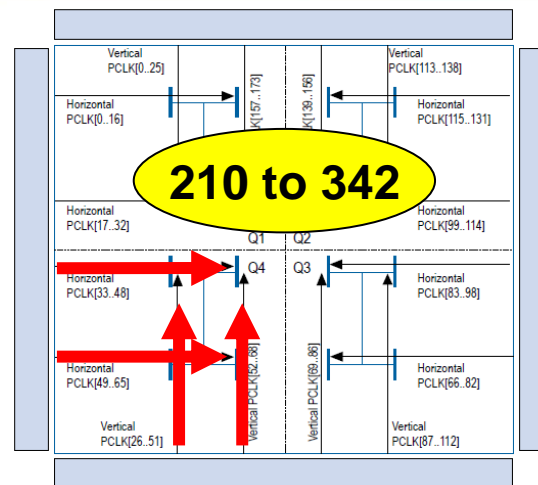
20nm



Arria 10 Core Clocking: PCLK Networks

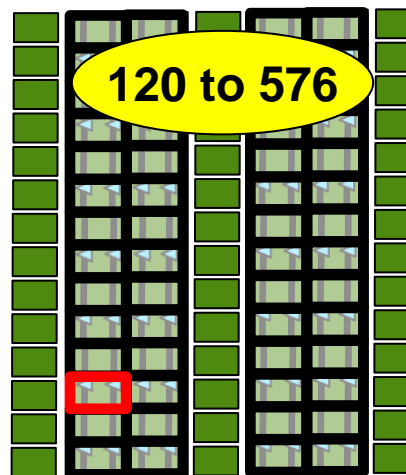
- **Periphery clock network**
- **Driven directly from the IOs to facilitate high-speed interfaces**
- **PCLK sources**
 - HSSI or DPA outputs
 - IO pins
 - Core signals
 - Power tie-off

Stratix V

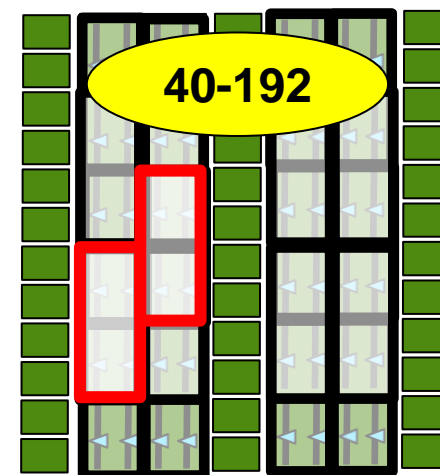


SPCLK (small)	LPCLK (large)
12 SPCLKs per IO and HSSI bank, cover 1 IO bank region	4 LPCLKs per IO and HSSI bank, cover 4 IO bank regions
Tiled	Staggered/overlap
Soft CDR and HSSI TX/RX clocks	HSSI channel bonding (e.g. PCIe x8, ILKN x12) and wide DDR interfaces (e.g. 72-bit)

SPCLK (small)



LPCLK (large)



Arria 10



Arria 10 Core Clocking Summary

Clock Resource	Stratix V	Arria 10
f_{MAX}	717 MHz	800 MHz
Clock pins	48	36-144
GCLK networks	16	32
RCLK networks	92	8-24
SPCLK networks LPCLK networks	210-342	120-576 40-192
SCLK per spine segment	33	33
ROWCLK per LAB row	6	6
HIOCLK per LAB row	21	16
VIOCLK per VIO bank	9	N/A

Clock network resources optimized for high-performance applications

Arria 10 SoC introduction



Arria 10 SoCs: **Faster, Lower Power, Secure and SW Compatible**

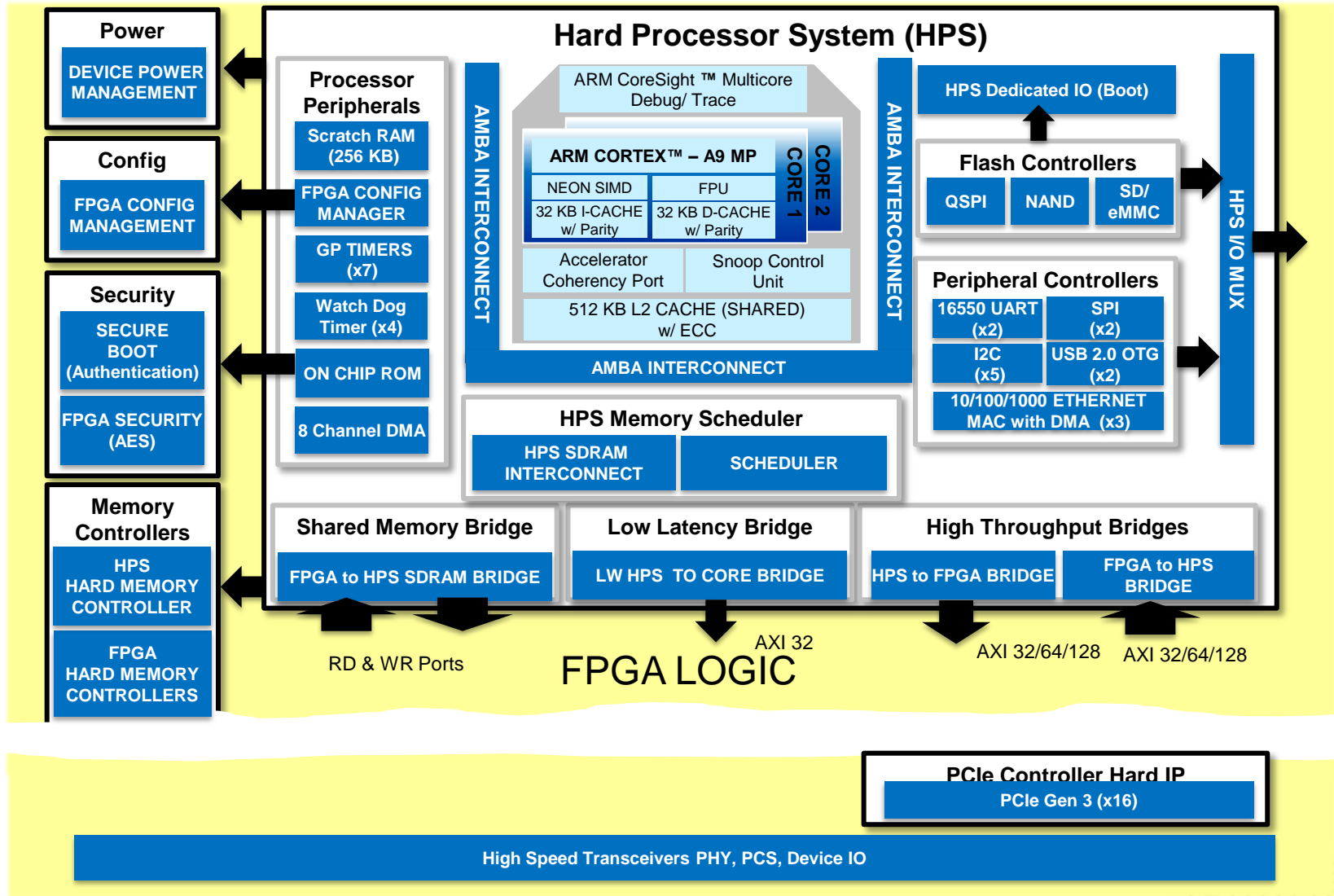
- **Arria 10 SoCs feature a 1.5 GHz Dual Core ARM Processor for**
 - communications processing, acceleration, host offload, deeply embedded processing and FPGA management
- **Faster**
 - Up to 1.5 GHz per core, total 7500 MIPS
- **Lower power**
 - Up to 40% lower device power
- **More Secure**
 - Secure Boot with EC DSA Authentication
 - Root of Trust Support (Certification Authority)
 - Anti-Tamper, Resistance to DPA and other attacks
- **Software Compatible**
 - Extensive of software, OS/BSP, tools reuse

*50% Faster Processor
40% Lower Power
Secure Boot
Software compatible*



Arria 10 SoCs are faster, lower power, more secure and software compatible with 28nm SoCs

Arria 10 HPS Block Diagram



Arria 10 HPS Peripheral Feature Summary

EXTERNAL MEMORY CONTROLLERS

- **Hard Memory Controller (HMC) with support for external memory devices:** **NEW**
 - DDR4/3, LPDDR2/3
 - Most packages support up to 40-Bit DDR4, select packages with up to 72-bit DDR4 also available
 - Multiport Front End (MPFE) Scheduler interface to HMC sharable with logic core
- **QSPI flash controller with SIO, DIO, QIO SPI Flash support**
- **NAND flash controller (ONFI 1.0 or later) with DMA and ECC support** **UPDATED**
 - Updated to support 8 and 16-bit Flash devices
- **SD/SDIO/MMC controller 4.5 with DMA with CE-ATA digital command support** **UPDATED**
 - Updated to eMMC

COMMUNICATION CONTROLLERS

- **3 x 10/100/1000 Ethernet media access control (MAC) with DMA** **NEW**
- **2x USB On-The-Go (OTG) controller with DMA**
- **2x UART 16550 controller**
- **5x I²C controller**
 - 3 can be used by EMAC for MIO to external PHY
- **4x serial peripheral interface (SPI)**
 - 2 Master, 2 Slaves

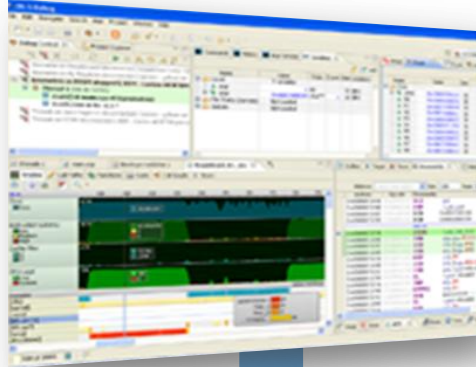
SECURITY & PERIPHERALS

- **Anti-tamper, Secure Boot, POF Encryption (AES) and Authentication (SHA) and Root of Trust Support** **NEW**
- **54 Programmable general-purpose I/O (GPIO)**
- **7x general-purpose timers**
- **4x watchdog timers**

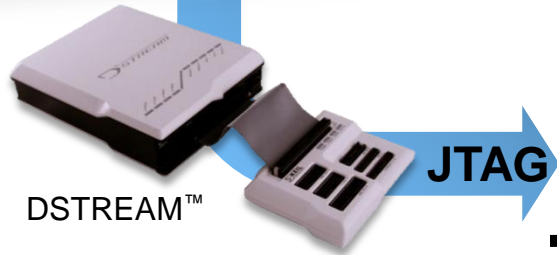
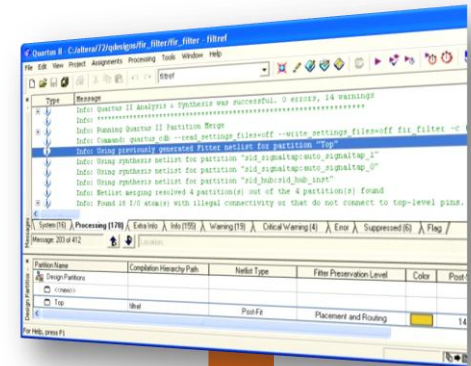
One Device, Two Debugging Tools?



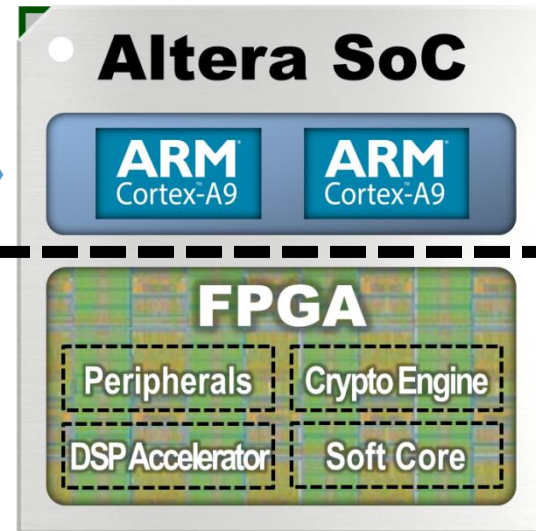
ARM® DS-5™ Toolkit



Altera Quartus™ II Software



- Dedicated JTAG connection
- Visualize & control CPU subsystem



- Dedicated JTAG connection
- Visualize & control FPGA



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START

DOCUMENTATION
Find information on boards, flows, and open hardware and software

CODE
Access the latest SoC Linux code from our git repositories

PROJECTS
Check out projects submitted by the community to get inspired

MAIL LISTS
Stay updated with latest news, features, questions and feedback

FORUM
Jump into the forum to get help and offer help

BOARDS
Explore the latest hardware



Arria 10 Summary



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Arria 10 Summary

■ Highest performance, lowest power 20nm FPGAs and SoCs

- A speed grade faster than competitive 20nm FPGAs
- Up to 40% lower power compared to prior generation

■ Key features for midrange applications

- Up to 1.15M logic elements and 53 Mbits embedded block RAM
- Up to 96 transceivers up to 28.3G chip-to-chip, up to 17.4G backplane
- Footprint-compatible dual-core ARM Cortex A9 SoC options
- Over 850 Gbps DDR4 bandwidth
- Up to 1.5 TFLOPs of floating-point DSP performance

■ Maximum productivity

- Quartus II support rolled out in half the time compared to prior generation
- OpenCL support for system acceleration



Arria 10 FPGAs and SoCs Reinvent the Midrange!



Thank You



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